LM2412

LM2412 Monolithic Triple 2.8 ns CRT Driver

Literature Number: SNOS511A

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National Semiconductor

LM2412
Monolithic Triple 2.8 ns CRT Driver

General Description

The LM2412 is an integrated high voltage CRT driver circuit designed for use in high resolution color monitor applications. The IC contains three high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to −14 and can drive CRT capacitive loads as well as resistive loads presented by other applications, limited only by the package's power dissipation. The LM2412 is a low power alternative of the LM2402

The IC is packaged in an industry standard 11 lead TO-220 molded plastic power package. See thermal considerations section for heat sinking requirements.

Features

- Rise/fall times typically 2.8 ns with 8 pF load at 40 V_{PP}
- Lower power than LM2402 with the same bandwidth
- Well matched with LM2202 video preamps
- Output swing capability: 50 V_{PP} for V_{CC} = 80V
- 1V to 5V input range
- Stable with 0-20 pF capacitive loads and inductive peaking networks
- Convenient TO-220 staggered lead package style
- Standard LM240X family pinout which is designed for easy PCB layout

Applications

- CRT driver for color monitors with display resolutions up to 1600 x 1200 with 85 Hz refresh rate
- Pixel clock frequency up to 200 MHz

Schematic and Connection Diagrams

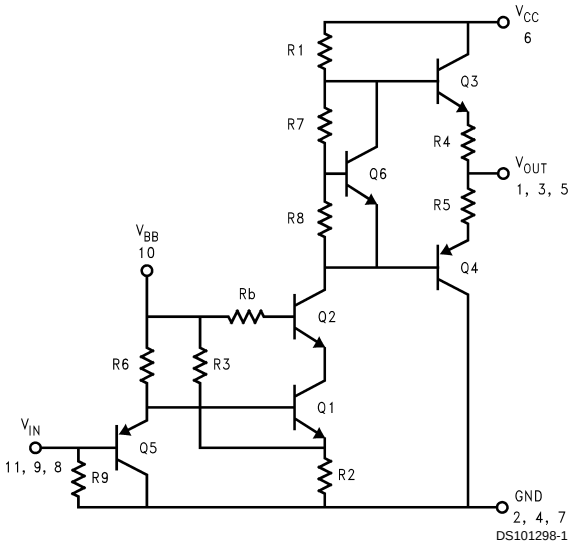
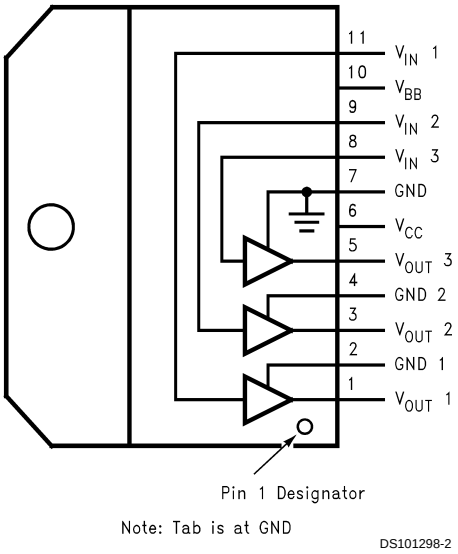


FIGURE 1. Simplified Schematic Diagram (One Channel)



Top View
Order Number LM2412T
See NS package Number

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	+90V
Bias Voltage, V_{BB}	+16V
Input Voltage, V_{IN}	0V to 6V
Storage Temperature Range, T_{STG}	−65˚C to +150˚C
Lead Temperature (Soldering, <10 sec.)	300˚C
ESD Tolerance	
Human Body Model	2 kV
Machine Model	250V

Operating Ranges (Note 3)

V_{CC}	+60V to +85V
V_{BB}	+8V to +15V
V_{IN}	+1V to +5V
V_{OUT} (V_{CC} = 80V, V_{BB} = 12V)	+15V to +75V
Case Temperature	−20˚C to +100˚C

Do not operate the part without a heat sink.

Electrical Characteristics

(See *Figure 2* for Test Circuit)

Unless otherwise noted: V_{CC} = +80V, V_{BB} = +12V, V_{IN} = +3.3 V_{DC}, C_L = 8 pF, T_C = 60˚C, no AC input.

Symbol	Parameter	Conditions	LM2412			Units
			Min	Typ	Max	
I_{CC}	Supply Current	Per Channel, No Output Load	16	21	26	mA
I_{BB}	Bias Current	All Three Channels	27	42	57	mA
V_{OUT}	DC Output Voltage	V_{IN} = 1.9V	62	65	68	V_{DC}
A_V	DC Voltage Gain		−12	−14	−16	
ΔA_V	Gain Matching	(Note 4)		1.0		dB
LE	Linearity Error	(Notes 4, 5)		3.5		%
t_r	Rise Time (Notes 6, 7)	10% to 90%, 40 V_{PP} Output (1 MHz)		2.8	3.5	ns
t_f	Fall Time (Notes 6, 7)	10% to 90%, 40 V_{PP} Output (1 MHz)		2.8	3.5	ns
OS	Overshoot	40 V_{PP} Output (1 MHz)		5		%

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 4: Calculated value from voltage gain test on each channel.

Note 5: Linearity error is the variation in DC gain from V_{IN} = 1.6V to V_{IN} = 5.0V.

Note 6: Input from signal generator: t_r, t_f < 1 ns.

Note 7: 100% tested in production. These limits are not used to calculate outgoing quality levels.

AC Test Circuit

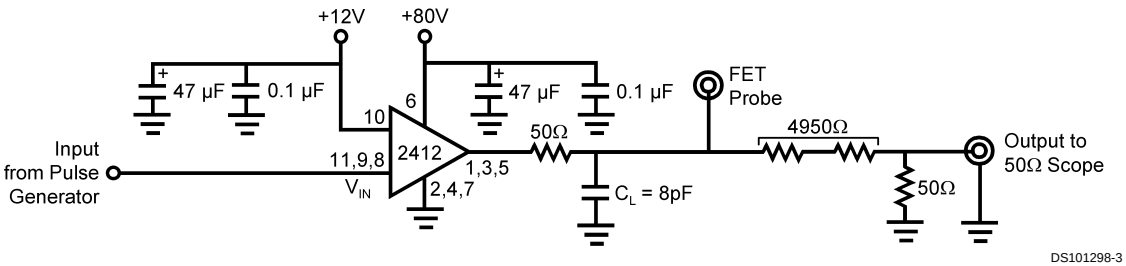


FIGURE 2. Test Circuit (One Channel)

Figure 2 shows a typical test circuit for evaluation of the LM2412. This circuit is designed to allow testing of the LM2412 in a 50Ω environment without the use of an expensive FET probe. The combined resitors of 4950Ω at the output form a 200:1 voltage divider when connected to a 50Ω load. The test board supplied by NSC also offers the option to test theLM2412 with a FET probe. C_L is the total capacitance at the LM2412 output, including the board capacitance.

Typical Performance Characteristics

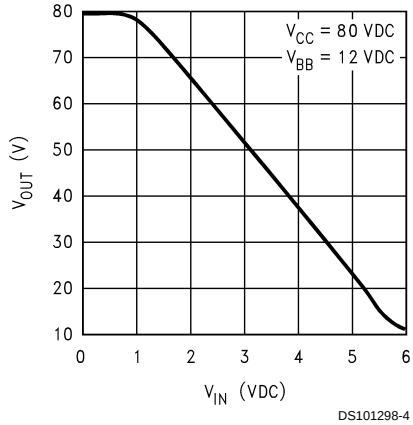


FIGURE 3. V_{IN} vs V_{OUT}

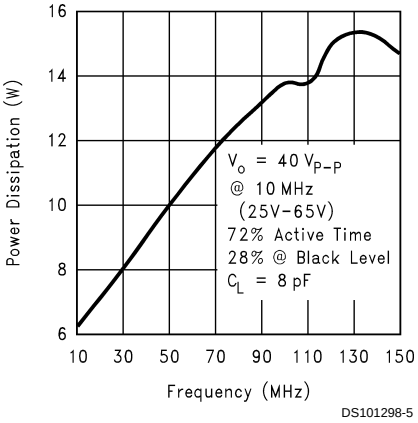


FIGURE 6. Power Dissipation vs Frequency

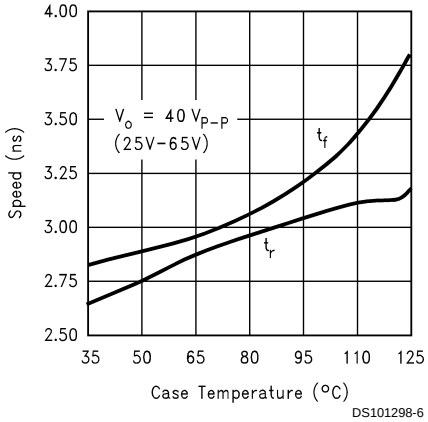


FIGURE 4. Speed vs Temp.

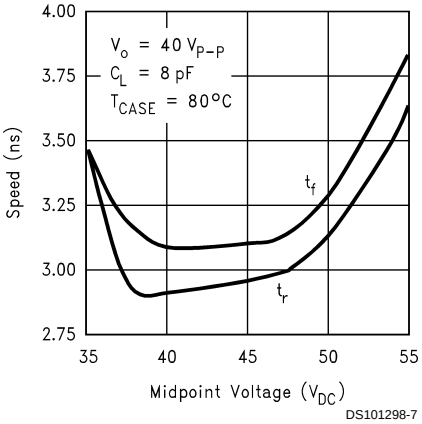


FIGURE 7. Speed vs Offset

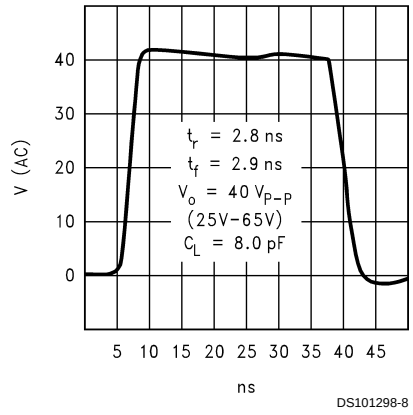


FIGURE 5. Rise/Fall Time

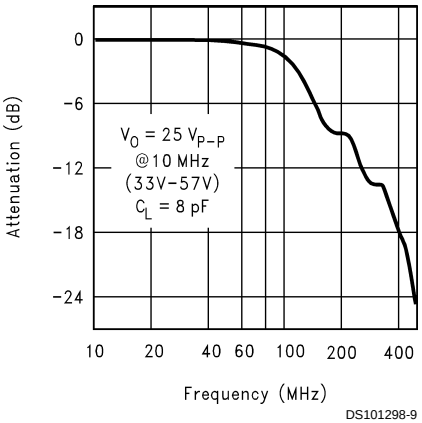


FIGURE 8. Bandwidth

Theory of Operation

The LM2412 is a high voltage monolithic three channel CRT driver suitable for very high resolution display applications, up to 1600 x 1200 at 85 Hz refresh rate. The LM2412 operates using 80V and 12V power supplies. The part is housed in the industry standard 11-lead TO-220 molded plastic power package.

The simplified circuit diagram of one channel of the LM2412 is shown in *Figure 1*. A PNP emitter follower, Q5, provides input buffering. This minimizes the current loading of the video pre-amp. R9 is used to turn on Q5 when there is no input. With Q5 turned on, Q1 will be almost completely off, minimizing the current flow through Q1 and Q2. This will drive the output stage near the V_{CC} rail, minimizing the power dissipation with no inputs. R6 is a pull-up resistor for Q5 and also limits the current flow through Q5. R3 and R2 are used to set the current flow through Q1 and Q2. The ratio of R1 to R2 is used to set the gain of the LM2412. R1, R2 and R3 are all related when calculating the output voltage of the CRT driver. R_b limits the current through the base of Q2. Q1 and Q2 are in a cascode configuration. Q1 is a low voltage and very fast transistor. Q2 is a higher voltage transistor. The cascode configuration gives the equivalent of a very fast and high voltage transistor. The two output transistors, Q3 and Q4, form a class B amplifier output stage. R4 and R5 are used to limit the current through the output stage and set the output impedance of the LM2412. Q6, along with R7 and R8 set the bias current through Q3 and Q4 when there is no change in the signal level. This bias current minimizes the crossover distortion of the output stage. With this bias current the output stage now becomes a class AB amplifier with a crossover distortion much lower than a class B amplifier.

Figure 2 shows a typical test circuit for evaluation of the LM2412. Due to the very wide bandwidth of the LM2412, it is highly recommended that the stand alone board suplied by NSC be used for the evaluation of the CRT driver's performance. The 50Ω resistor is used to duplicate the required series resistor in the actual application. This resistor would be part of the arc-over protection circuit. The input signal from the generator is AC coupled to the input of the CRT driver.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to providing application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

POWER SUPPLY BYPASS

Since the LM2412 is a very high bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing and oscillation. A 0.1 µF capacitor should be connected from the supply pin, V_{CC}, to ground, as close to the supply and ground pins as is practical. Additionally, a 10 µF to 100 µF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should also be placed reasonably close to the LM2412's supply and ground pins. A 0.1 µF capacitor should be connected from the bias pin, V_{BB}, to ground, as close as is practical to the part.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 200V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2412. This fast, high voltage, high energy pulse can damage the LM2412 output stage. The application circuit shown in *Figure 9* is designed to help clamp the voltage at the output of the LM2412 to a safe level. The clamp diodes should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor. The ground connection of the diode and the decoupling capacitor should be very close to the LM2412 ground. This will significantly reduce the high frequency voltage transients that the LM2412 would be subjected to during an arc-over condition. Resistor R2 limits the arc-over current that is seen by the diodes while R1 limits the current into the LM2412 as well as the voltage stress at the outputs of the device. R2 should be a ½W solid carbon type resistor. R1 can be a ¼W metal or carbon film type resistor. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2412 would be subjected to during an arc-over. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. The inductor will not only help protect the device but it will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 9*. The values of L1 and R1 may need to be adjusted for a particular application. The recommended minimum value for R1 is 75Ω, with L1 = .049 µH.

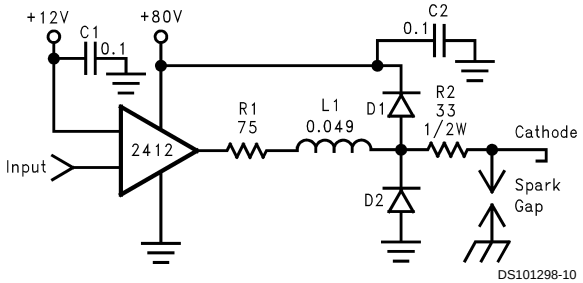


FIGURE 9. One Channel of the LM2412 with the Recommended Arc Protection Circuit.

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 9*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1

Application Hints (Continued)

and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Air core inductors from J.W. Miller Magnetics (part #75F518MPC) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 9* can be used as a good starting point for the evaluation of the LM2412.

Effect of Load Capacitance

The output rise and fall times as well as overshoot will vary as the load capacitance varies. The values of the output circuit (R1, R2 and L1 in *Figure 9*) should be chosen based on the nominal load capacitance. Once this is done the performance of the design can be checked by varying the load based on what the expected variation will be during production.

Effect of Offset

Figure 7 shows the variation in rise and fall times when the output offset of the device is varied from 35 to 55 V_{DC}. The rise and fall times show about the same overall variation. The slightly slower fall time is fastest near the center point of 45V, making this the optimum operating point. At the low and high output offset range, the characteristic of rise/fall time is slower due to the saturation of Q3 and Q4. The recovery time of the output transistors takes longer coming out of saturation thus slows down the rise and fall times.

THERMAL CONSIDERATIONS

Figure 4 shows the performance of the LM2412 in the test circuit shown in *Figure 2* as a function of case temperature. *Figure 4* shows that both the rise and fall times of the LM2412 become slightly longer as the case temperature increases from 40˚C to 125˚C. In addition to exceeding the safe operating temperature, the rise and fall times will typically exceed 3 nsec. Please note that the LM2412 is **never to be operated over a case temperature of 100˚C.** In addition to exceeding the safe operating temperature, the rise and fall times will typically exceed 3 nsec.

Figure 6 shows the total power dissipation of the LM2412 vs. Frequency when all three channels of the device are driving an 8 pF load. Typically the active time is about 72% of the total time for one frame. Worst case power dissipation is when a one on, one off pixel is displayed over the active time of the video input. This is the condition used to measure the total power disspation of the LM2412 at different input frequencies. *Figure 6* gives all the information a monitor designer normally needs for worst case power dissipation. However, if the designer wants to calculate the power dissipation for an active time different from 72%, this can be done using the information in *Figure 14*. The recommended input black level voltage is 1.9V. From *Figure 14*, if a 1.9V input is used for the black level, then power dissipation during the inactive video time is 2.7W. This includes both the 80V and 12V supplies.

If the monitor designer chooses to calculate the power dissipation for the LM2412 using an active video time different from 72%, then he needs to use the following steps when using a 1.9V input black level:

1. Multiply the black level power dissipation, 2.7W, by 0.28, the result is 0.8W.
2. Choose the maximum frequency to be used. A typical application would use 100 MHz, or a 200 MHz pixel clock. The power dissipation is 13.8W.
3. Subtract the 0.8W from the power dissipation from *Figure 6*. For 100 MHz this would be 13.8 – 0.8 = 13.0W.
4. Divide the result from step 3 by 0.72. For 100 MHz, the result is 18.1W.
5. Multiply the result in 4 by the new active time percentage.
6. Multiply 2.7W by the new inactive time.
7. Add together the results of steps 5 and 6. This is the expected power dissipation for the LM2412 in the designer's application.

The LM2412 case temperature must be maintained below 100˚C. If the maximum expected ambient temperature is 70˚C and the maximum power dissipation is 13.8W (from Figure 6. 100MHz) then a maximum heat sink thermal resistance can be calculated:

$$TH = \frac{100°C - 70°C}{13.8W} = 2.2°C/W$$

TYPICAL APPLICATION

A typical application of the LM2412 is shown in *Figure 10*. Used in conjunction with three LM2202s, a complete video channel from monitor input to CRT cathode can be achieved. Performance is excellent for resolutions up to 1600 x 1200 and pixel clock frequencies at 200 MHz. *Figure 10* is the schematic for the NSC demonstration board that can be used to evaluate the LM2202/LM2412 combination in a monitor.

PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2412 and from the LM2412 to the CRT cathode should be as short as possible. The red video trace from the buffer transistor to the LM2412 input is about the absolute maximum length one should consider on a PCB layout. If possible the traces should actually be shorter than the red video trace. The following references are recommended for video board designers:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Guide to CRT Video Design", National Semiconductor Application Note 861.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

NSC Demonstration Board

Figures 11, 12 show routing and component placement on the NSC LM2202/2412 demonstration board. The schematic of the board is shown in *Figure 10*. This board provides a

Application Hints (Continued)

good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- *C47* - V_{CC} bypass capacitor, located very close to pin 6 and ground pins. (*Figure 12*)
- *C49* - V_{BB} bypass capacitor, located close to pin 10 and ground. (*Figure 12*)
- *C46 and C77* - V_{CC} bypass capacitors, near LM2412 and V_{CC} clamp diodes. Very important for arc protection. (*Figure 11*)

The routing of the LM2412 outputs to the CRT is very critical to achieving optimum performance. *Figure 13* shows the routing and component placement from pin 1 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2412 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. The direct video path is shown in by a dark gray line through the components and the PCB traces. Note also that D24, D25, R58 and D19 are placed to keep the size of the video nodes to a minimum (R58 is located under D19). This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The traces in the video nodes to these components are shown by the white line. The anode of protection diode D25 is connected directly to the ground plane giving a short and direct path to the LM2412 ground pins. The cathode of D24 is connected to V_{CC} very close to decoupling capacitor C78 (*Figure 13*) which is connected to the same section of the ground plane as D25. The diode placement and routing is very important for minimizing the voltage stress on the LM2412 during an arc-over event. Lastly, notice that S3 is placed very close to the blue cathode and is tied directly to CRT ground.

Application Hints (Continued)

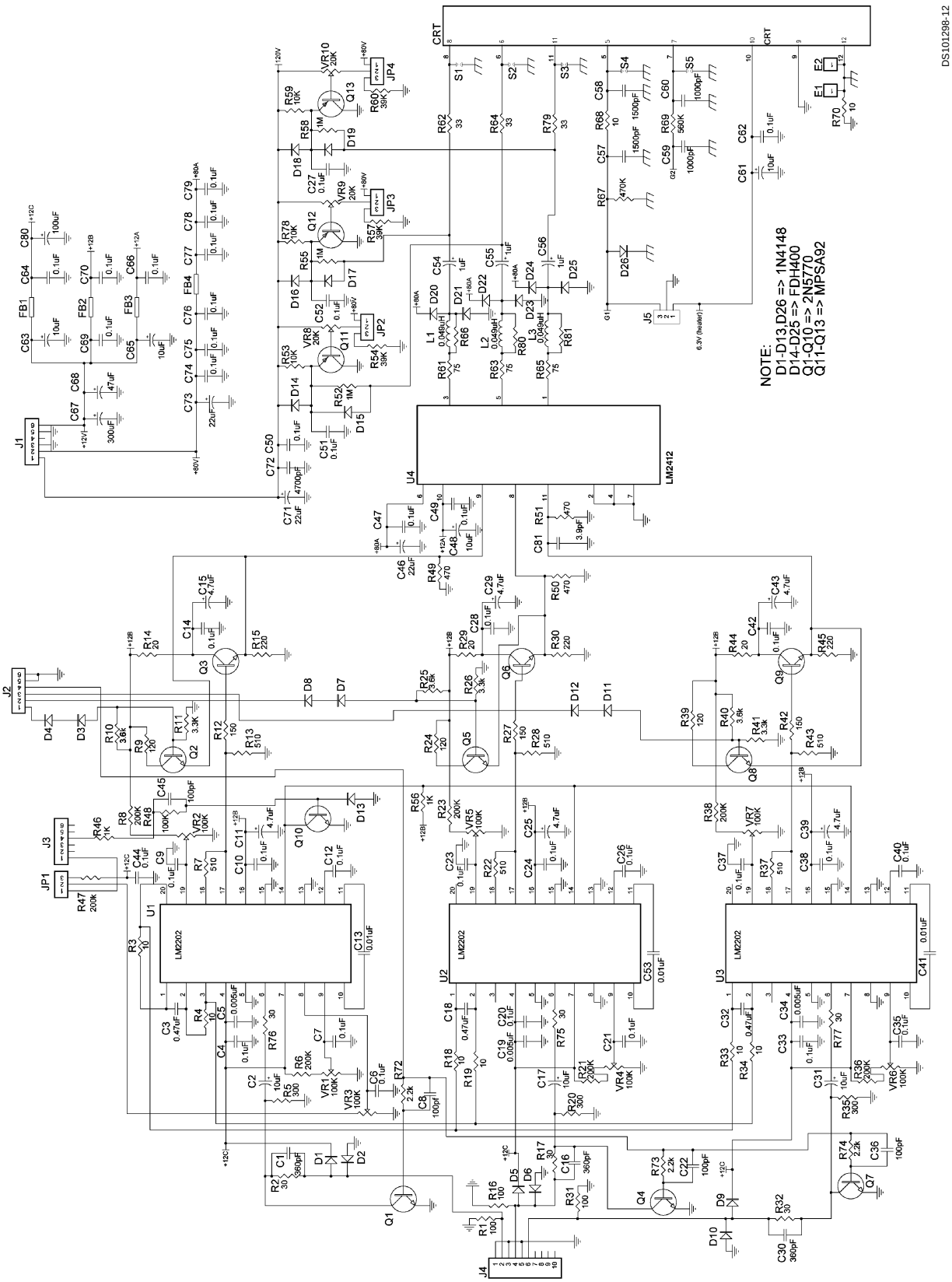
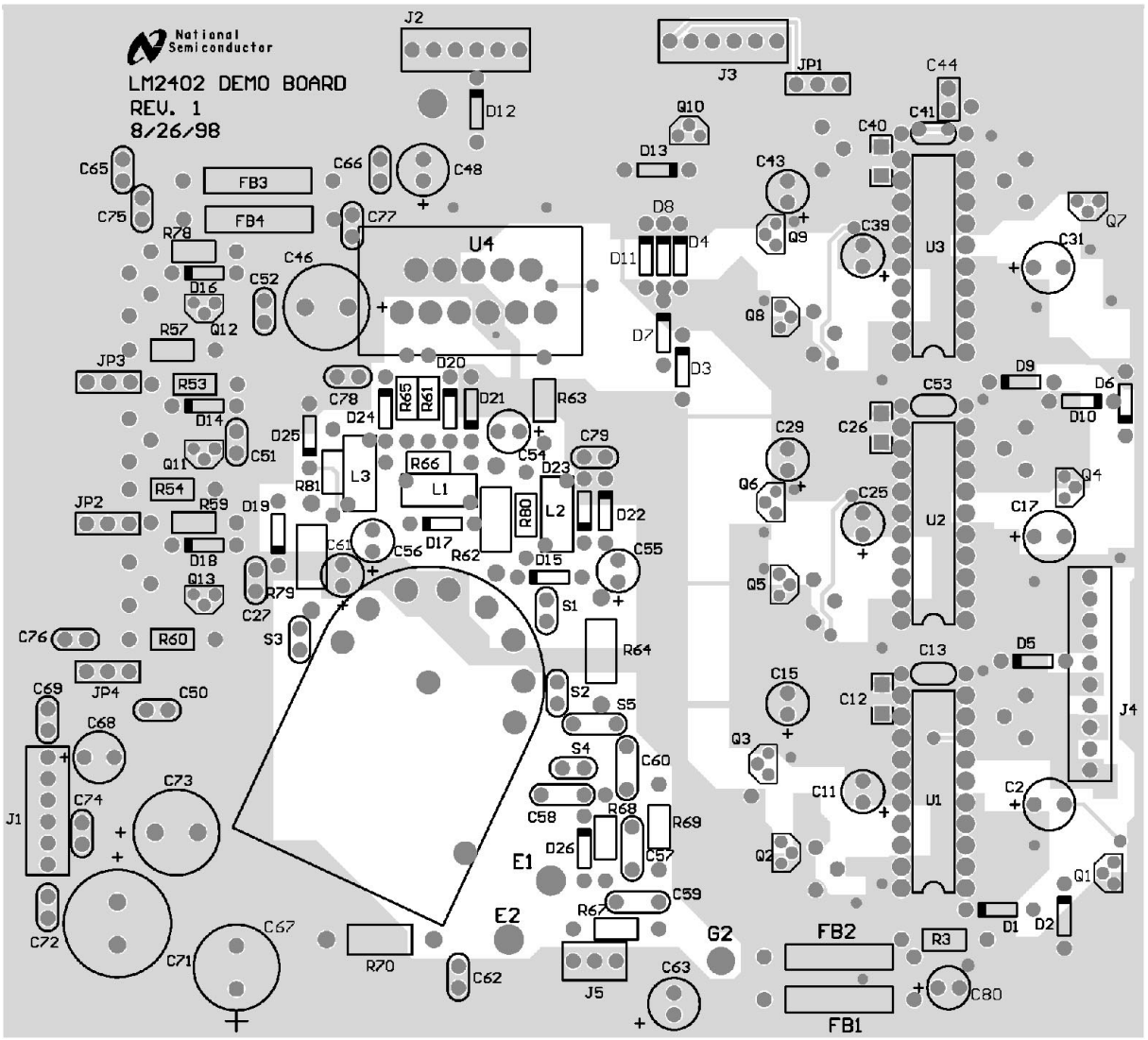


FIGURE 10. Demo Board Schematic

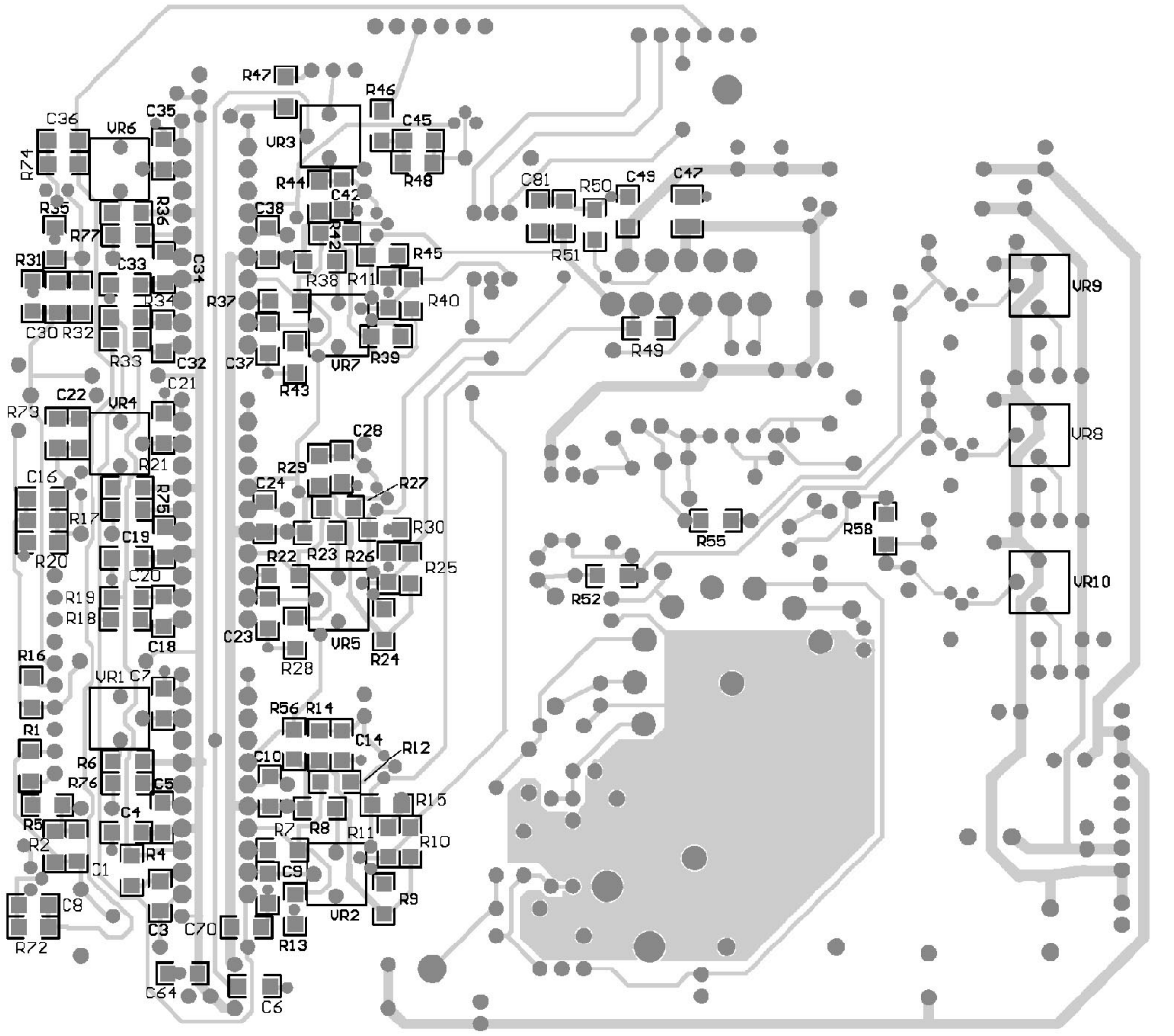
Application Hints (Continued)



DS101298-13

FIGURE 11. PCB Top Layer

Application Hints (Continued)



DS101298-14

FIGURE 12. PCB Bottom Layer

Application Hints (Continued)

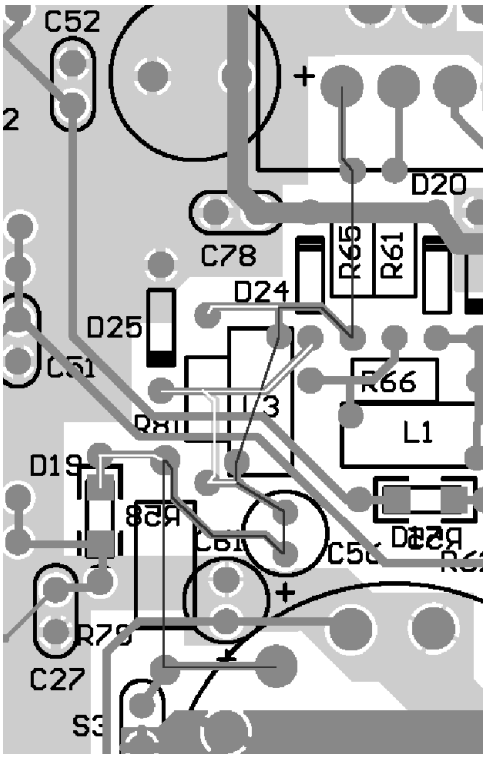


FIGURE 13. PCB CRT Driver, Blue Channel Output

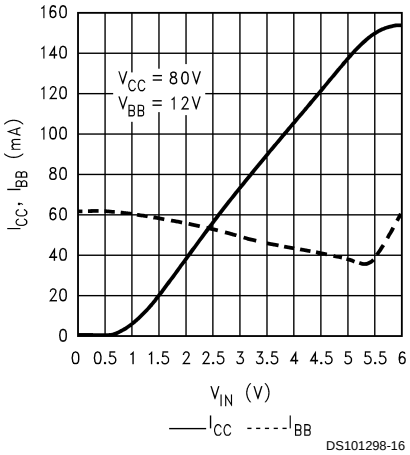
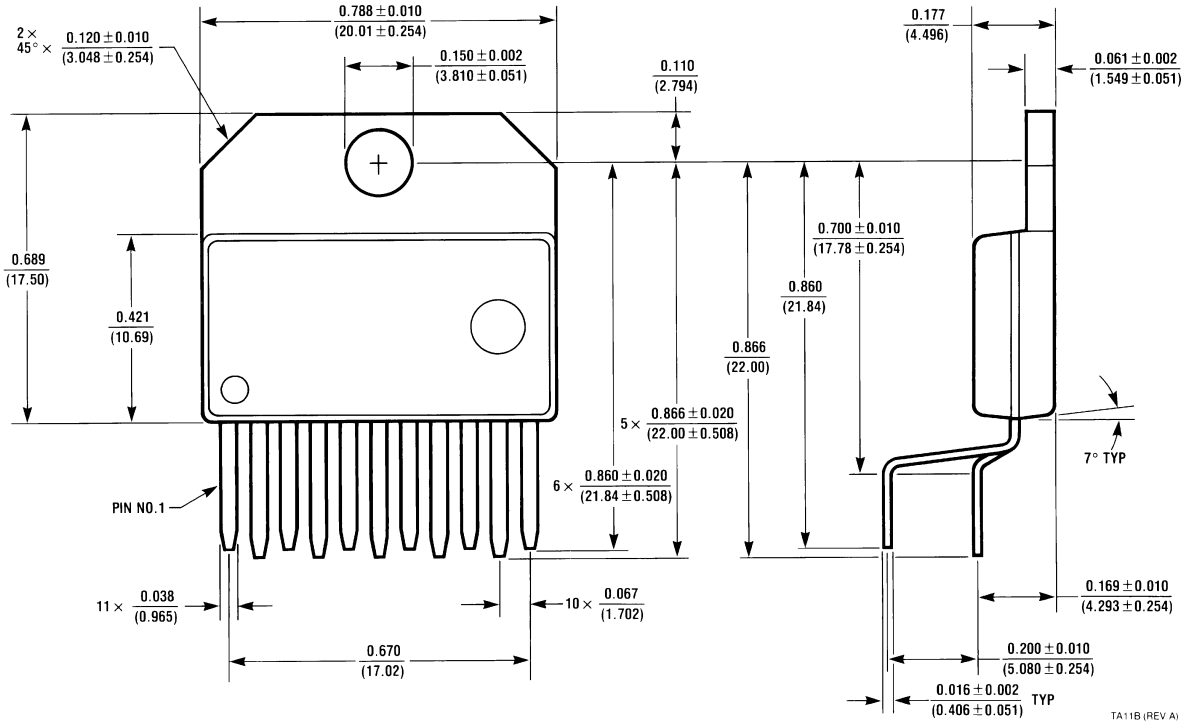


FIGURE 14. I_{CC} and I_{BB} vs V_{IN}

Physical Dimensions inches (millimeters) unless otherwise noted



11 Lead Molded TO-220
NS Package Number TA11B
Order Number LM2412T

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