



PCA85276

Automotive 40 x 4 LCD driver

Rev. 4 — 29 September 2021

Product data sheet

1 General description

The PCA85276 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)¹ with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. It can be easily cascaded for larger LCD applications. The PCA85276 is compatible with most microcontrollers and communicates via the two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing, and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see [Table 23](#).

2 Features and benefits

- AEC-Q100 grade 2 compliant for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
 - Up to 20 7-segment numeric characters
 - Up to 10 14-segment alphanumeric characters
 - Any graphics of up to 160 segments/elements
- 40 × 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
 - From 2.5 V for low-threshold LCDs
 - Up to 8.0 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- Extended temperature range up to 105 °C
- 400 kHz I²C-bus interface
- May be cascaded for large LCD applications (up to 1 280 segments/elements possible)
- No external components required

¹ The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 21](#).



3 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA85276ATT/A	PCA85276TT	TSSOP56	plastic thin shrink small outline package, 56 leads; body width 6.1 mm with 0.5 mm pitch	SOT364-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method ^[1]	Minimum order quantity	Temperature
PCA85276ATT/A	PCA85276ATT/AJ ^[2]	TSSOP56	reel 13 inch q1 non dry pack	2000	T _{amb} = -40 °C to +105 °C
	PCA85276ATT/AY	TSSOP56	reel 13 inch q1 dry pack	2000	T _{amb} = -40 °C to +105 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/

[2] Discontinuation notice 202107021DN - drop-in replacement is PCA85276ATT/AY - this is documented in PCN202102010F01.

4 Block diagram

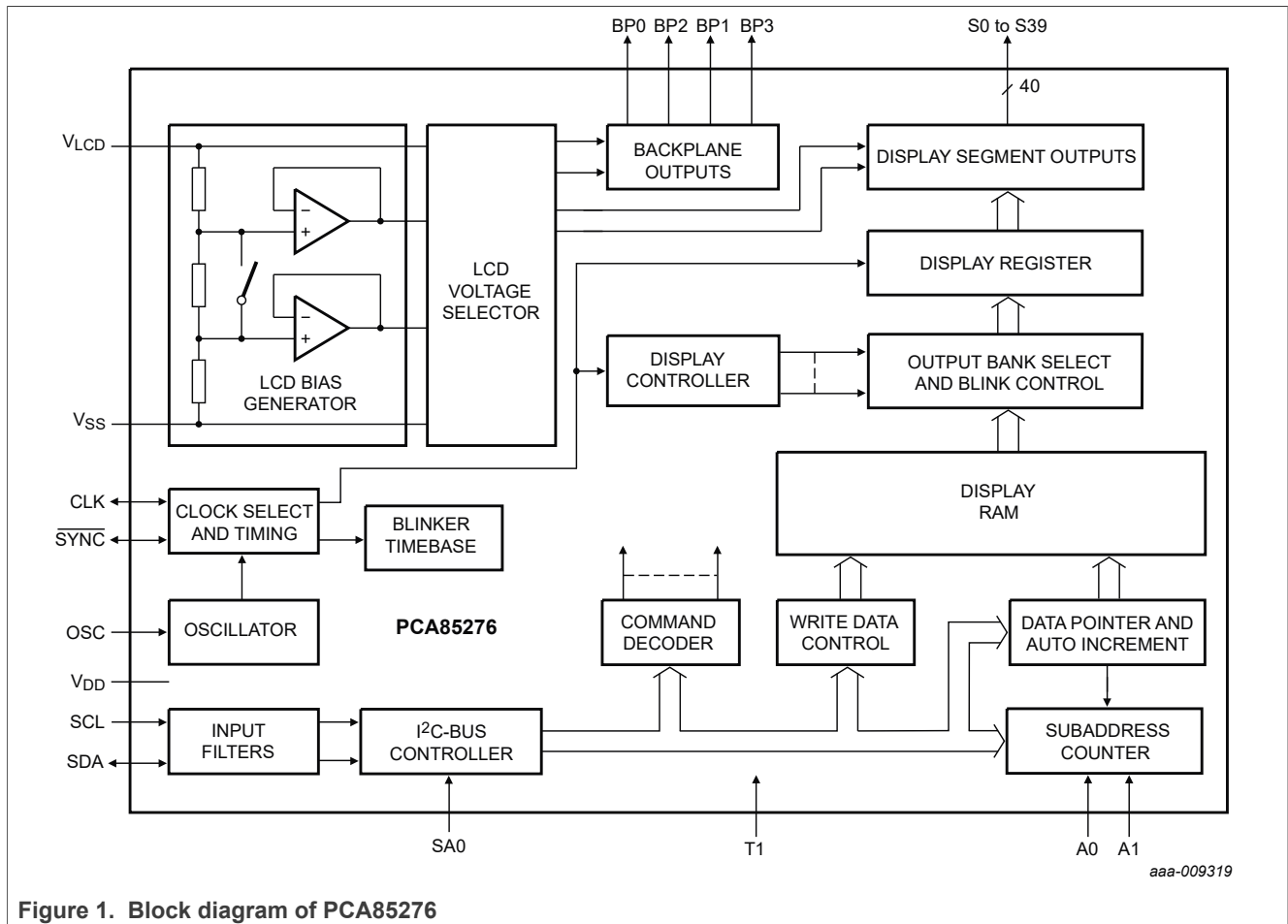
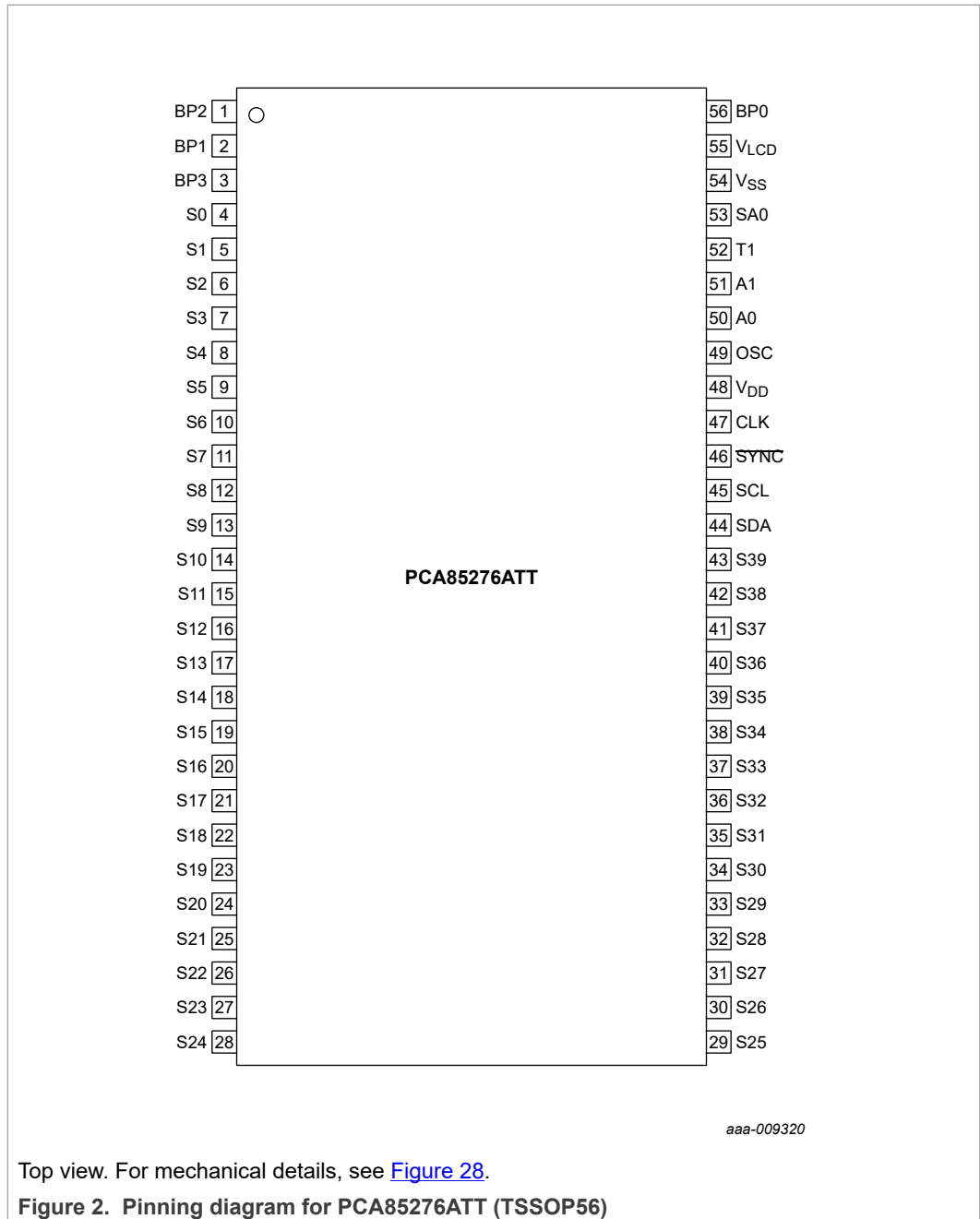


Figure 1. Block diagram of PCA85276

5 Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description of PCA85276ATT (TSSOP56)

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
	PCA85276ATT		
SDA	44	input/output	I ² C-bus serial data line
SCL	45	input	I ² C-bus serial clock
CLK	47	input/output	clock line
V _{DD}	48	supply	supply voltage
SYNC	46	input/output	cascade synchronization; if not used it must be left open
OSC	49	input	internal oscillator enable
A0, A1	50, 51	input	subaddress inputs
T1	52	input	dedicated testing pin; to be tied to V _{SS} in application mode
SA0	53	input	I ² C-bus address input
V _{SS}	54	supply	ground supply voltage
V _{LCD}	55	supply	LCD supply voltage
BP0, BP2, BP1, BP3	56, 1, 2, 3	output	LCD backplane outputs
S0 to S39	4 to 43	output	LCD segment outputs

6 Functional description

The PCA85276 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot-matrix displays. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

6.1 Commands of PCA85276

The commands available to the PCA85276 are defined in [Table 4](#).

Table 4. Definition of the PCA85276 commands

Bit position labeled as - is not used.

Command	Operation Code								Reference	
	7	6	5	4	3	2	1	0		
mode-set	C	1	0	-	E	B	M[1:0]		Table 6	
load-data-pointer	C	0	P[5:0]							Table 7
device-select	C	1	1	0	0	0	A[1:0]		Table 8	
bank-select	C	1	1	1	1	0	I	O	Table 9	
blink-select	C	1	1	1	0	AB	BF[1:0]		Table 10	

All available commands carry a continuation bit C in their most significant bit position as shown in [Figure 21](#). When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes are regarded as display data (see [Table 5](#)).

Table 5. C bit description

Bit	Symbol	Value	Description
7	C		continue bit
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

6.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 6. Mode-set command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 5
6 to 5	-	10	fixed value
4	-	-	unused
3	E		display status ^[1]
		0	disabled (blank) ^[2]
		1	enabled
2	B		LCD bias configuration ^[3]
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		LCD drive mode selection
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] The display is disabled by setting all backplane and segment outputs to V_{LCD} .

[3] Not applicable for static drive mode.

6.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data are sent to.

Table 7. Load-data-pointer command bit description

See [Section 6.3.1](#).

Bit	Symbol	Value	Description
7	C	0, 1	see Table 5
6	-	0	fixed value
5 to 0	P[5:0]	00 0000 to 10 0111	6-bit binary value, 0 to 39; transferred to the data pointer to define one of forty display RAM addresses

6.1.3 Command: device-select

The device-select command allows defining the subaddress counter value.

Table 8. Device-select command bit description

See [Section 6.3.2](#).

Bit	Symbol	Value	Description
7	C	0, 1	see Table 5
6 to 2	-	110 00	fixed value
1 to 0	A[1:0]	00 to 11	2-bit binary value, 0 to 3; transferred to the subaddress counter to define one of four hardware subaddresses

6.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 9. Bank-select command bit description

See [Section 6.3.5](#).

Bit	Symbol	Value	Description	
			Static	1:2 multiplex ^[1]
7	C	0, 1	see Table 5	
6 to 2	-	111 10	fixed value	
1	I		input bank selection ; storage of arriving display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		output bank selection ; retrieval of LCD display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

6.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 10. Blink-select command bit description

See [Section 6.1.5.1](#).

Bit	Symbol	Value	Description
7	C	0, 1	see Table 5
6 to 3	-	111 0	fixed value
2	AB		blink mode selection
		0	normal blinking ^[1]
		1	alternate RAM bank blinking ^[2]
1 to 0	BF[1:0]		blink frequency selection
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

6.1.5.1 Blinking

The display blinking capabilities of the PCA85276 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see [Table 10](#)). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequencies depends on the blink mode selected (see [Table 11](#)).

An additional feature is for an arbitrary selection of LCD segments/elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD segments/elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see [Table 6](#)).

Table 11. Blink frequencies

Blink mode	Blink frequency ^[1]
off	-
1	$f_{blink} = \frac{f_{clk}}{768}$
2	$f_{blink} = \frac{f_{clk}}{1536}$
3	$f_{blink} = \frac{f_{clk}}{3072}$

[1] The blink frequency is proportional to the clock frequency (f_{clk}). For the range of the clock frequency, see [Table 19](#).

6.2 Clock and frame frequency

6.2.1 Internal clock

The internal logic of the PCA85276 and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. If the internal oscillator is used, the output from pin CLK can be used as the clock signal for several PCA85276 in the system that are connected in cascade.

6.2.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}. The LCD frame frequency is determined by the clock frequency (f_{clk}).

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

6.2.3 Timing

The PCA85276 timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the correct timing relationship between each PCA85276 in the system is maintained by the synchronization signal at pin \overline{SYNC} . The timing also generates the LCD frame frequency signal. The frame frequency signal is a fixed division

of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$

6.3 Display RAM

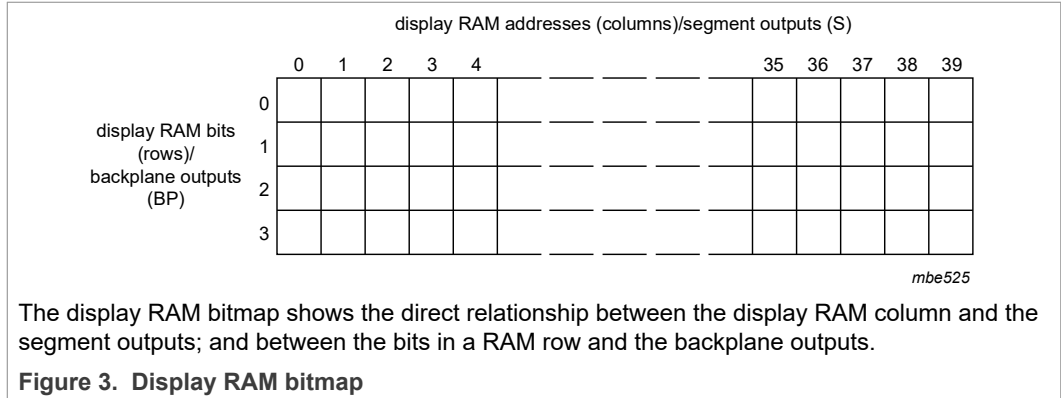
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD segments/elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bitmap, [Figure 3](#), shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



When display data is transmitted to the PCA85276, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in [Figure 4](#); the RAM filling organization depicted applies equally to other LCD types.

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as four successive 2-bit RAM words
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see [Section 6.3.3](#))
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words

drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte																																																					
static			<p>columns display RAM address/segment outputs (s) byte1</p> <table border="1"> <tr> <td>rows</td> <td>n</td> <td>n+1</td> <td>n+2</td> <td>n+3</td> <td>n+4</td> <td>n+5</td> <td>n+6</td> <td>n+7</td> </tr> <tr> <td>display RAM</td> <td>c</td> <td>b</td> <td>a</td> <td>f</td> <td>g</td> <td>e</td> <td>d</td> <td>DP</td> </tr> <tr> <td>rows/backplane</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>outputs (BP)</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td></td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> </tr> </table>	rows	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	display RAM	c	b	a	f	g	e	d	DP	rows/backplane	x	x	x	x	x	x	x	x	outputs (BP)	x	x	x	x	x	x	x	x		x	x	x	x	x	x	x	x	<p>MSB</p> <table border="1"> <tr> <td>c</td> <td>b</td> <td>a</td> <td>f</td> <td>g</td> <td>e</td> <td>d</td> <td>DP</td> </tr> </table> <p>LSB</p>	c	b	a	f	g	e	d	DP
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	DP	d																																																							
a	c	b	DP	f	e	g	d																																																		

001aa|646

x = data bit unchanged.

Figure 4. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

6.3.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see [Table 7](#)). Following this command, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in [Figure 4](#).

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If an I²C-bus data access terminates early, then the state of the data pointer is unknown. So, the data pointer must be rewritten prior to further RAM accesses.

6.3.2 Subaddress counter

The storage of display data is determined by the contents of the subaddress counter. Storage is allowed only when the content of the subaddress counter matches with the hardware subaddress applied to A0 and A1. The subaddress counter value is defined by the device-select command (see [Table 8](#)). If the content of the subaddress counter and the hardware subaddress do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCA85276 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

The hardware subaddress must not be changed while the device is being accessed on the I²C-bus interface.

6.3.3 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in [Table 12](#) (see [Figure 4](#) as well).

Table 12. Standard RAM filling in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. are not connected to any segments/elements on the display.

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:

Table 12. Standard RAM filling in 1:3 multiplex drive mode...continued

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any segments/elements on the display.

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in [Table 13](#).

Table 13. Entire RAM filling by rewriting in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to segments/elements on the display.

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in [Table 13](#) the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to segments/elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written
- The data-pointer (see [Section 6.3.1](#)) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some segments/elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

6.3.4 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. If the PCA85276 is part of a cascade the additional bits fall into the next device that also generates the acknowledge signal. If the PCA85276 is a single device or the last device in a cascade, the additional bits are discarded and no acknowledge signal is generated.

6.3.5 Bank selection

6.3.5.1 Output bank selector

The output bank selector (see [Table 9](#)) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, followed by the contents of row 1, row 2, and then row 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

6.3.5.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded by using the bank-select command (see [Table 9](#)). The input bank selector functions independently to the output bank selector.

6.3.5.3 RAM bank switching

The PCA85276 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see [Figure 5](#)). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

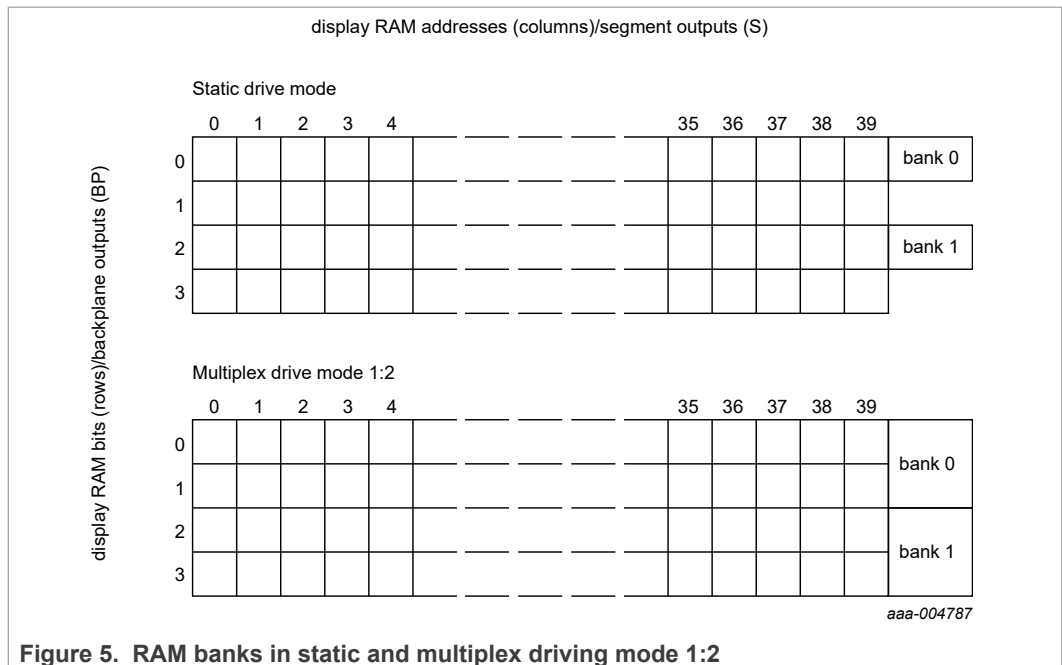


Figure 5. RAM banks in static and multiplex driving mode 1:2

There are two banks; bank 0 and bank 1. [Figure 5](#) shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see [Table 9](#)). [Figure 6](#) shows the concept.

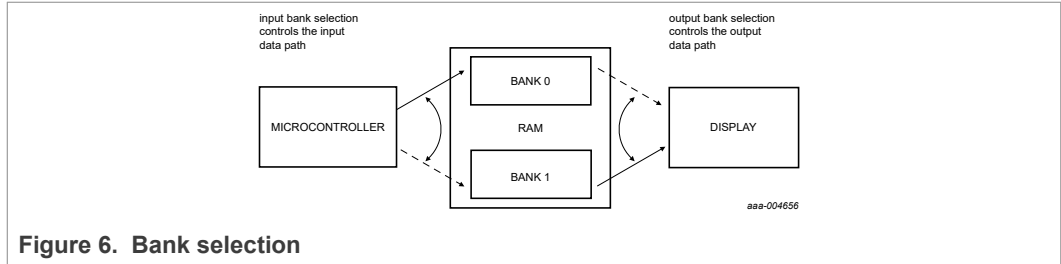


Figure 6. Bank selection

In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

In [Figure 7](#) an example is shown for 1:2 multiplex drive mode where the displayed data is read from the first two rows of the memory (bank 0), while the transmitted data is stored in the second two rows of the memory (bank 1).

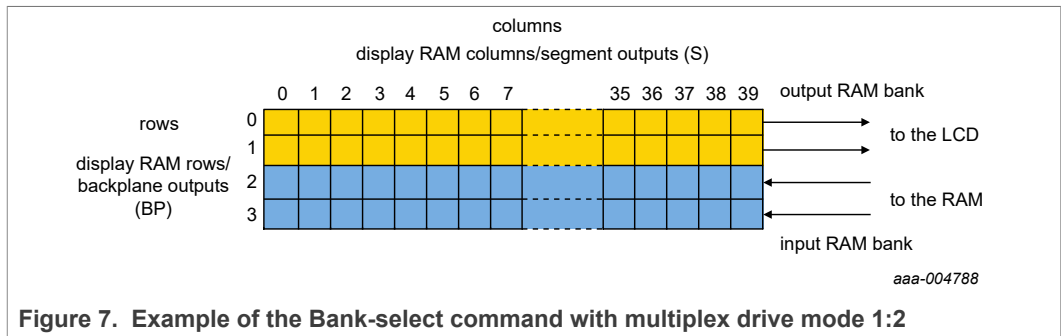


Figure 7. Example of the Bank-select command with multiplex drive mode 1:2

6.4 Initialization

At power-on the status of the I²C-bus and the registers of the PCA85276 is undefined. Therefore the PCA85276 should be initialized as quickly as possible after power-on to ensure a proper bus communication and to avoid display artifacts. The following instructions should be accomplished for initialization:

6.4.1 Device initialization

At power-on the status of the I²C-bus communication interface is undefined since this device doesn't have POR which was removed to improve the ESD performance. A START and STOP condition with dummy byte in-between must be sent after every power reset to set up the I²C-bus communication interface.

- I²C-bus (see [Section 7](#)) initialization
 - generating a START condition
 - sending 0h (1 byte) and ignoring the acknowledge – Note, this is not the device address but just a dummy byte of all zeros
 - generating a STOP condition

6.4.2 Device setup

At power-on the status of the display and configuration registers are undefined and need to be set up to properly display information on the LCD display. After the I²C-bus interface is initialized as discussed in [Section 6.4.1](#) set up the device using these register settings

- Mode-set command (see [Table 6](#)), setting
 - bit E = 0
 - bit B to the required LCD bias configuration
 - bits M[1:0] to the required LCD drive mode
- Load-data-pointer command (see [Table 7](#)), setting
 - bits P[4:0] to 0h (or any other required address)
- Device-select command (see [Table 8](#)), setting
 - bits A[1:0] to the required hardware subaddress (for example, 0h)
- Bank-select command (see [Table 9](#)), setting
 - bit I to 0
 - bit O to 0
- Blink-select command (see [Table 10](#)), setting
 - bit AB to 0 or 1
 - bits BF[1:0] to 00 (or to a desired blinking mode)
- writing meaningful information (for example, a logo) into the display RAM
- After the initialization, the display can be switched on by setting bit E = 1 with the mode-set command or left off (blank) with bit E = 0.

6.5 Possible display configurations

The possible display configurations of the PCA85276 depend on the number of active backplane outputs required. A selection of display configurations is shown in [Table 14](#). All of these configurations can be implemented in the typical system shown in [Figure 9](#).

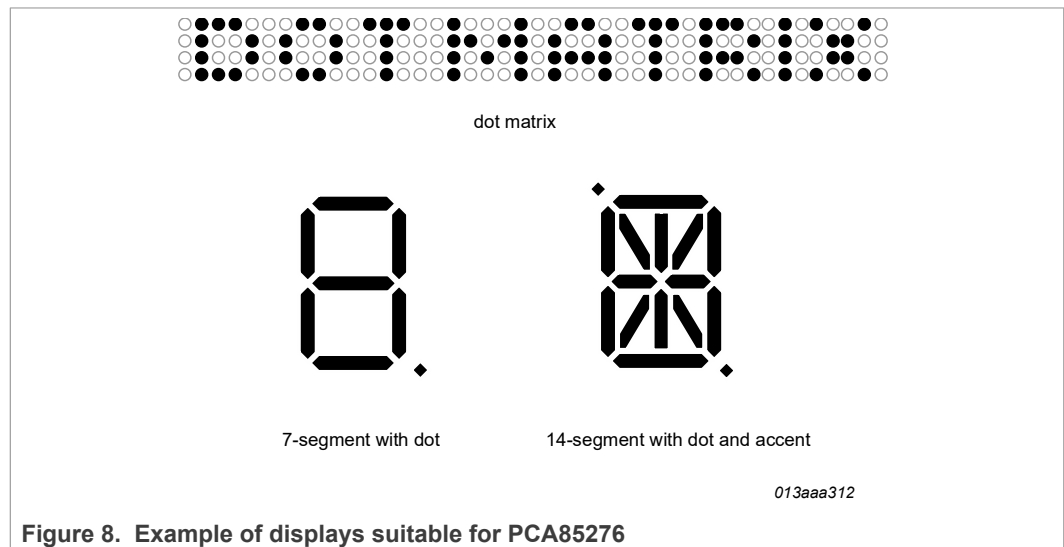


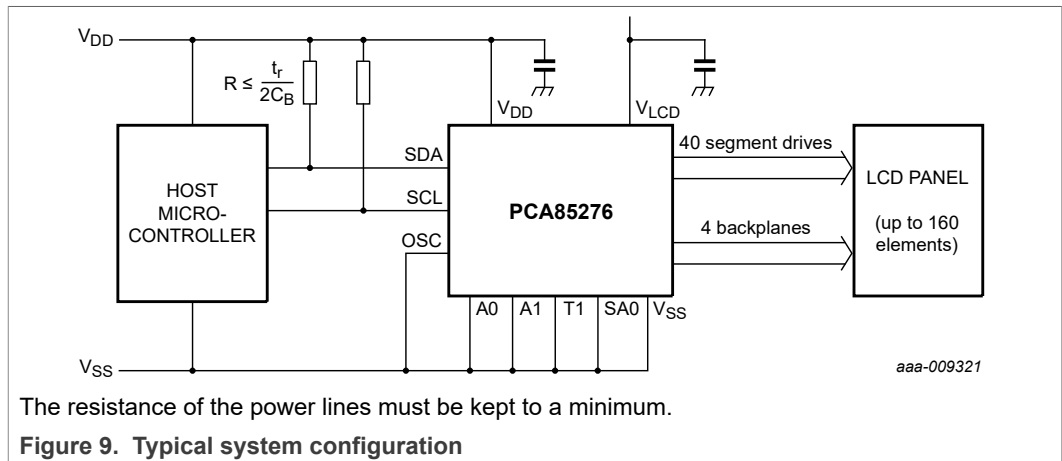
Figure 8. Example of displays suitable for PCA85276

Table 14. Selection of possible display configurations

Number of Backplanes	Icons	Digits/Characters		Dot matrix: segments/elements
		7-segment ^[1]	14-segment ^[2]	
4	160	20	10	160 (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 (2 × 40)
1	40	5	2	40 (1 × 40)

[1] 7 segment display has 8 segments/elements including the decimal point.

[2] 14 segment display has 16 segments/elements including decimal point and accent dot.



The host microcontroller maintains the 2-line I²C-bus communication channel with the PCA85276. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

6.5.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the 1/2 bias voltage level for the 1:2 multiplex drive mode configuration is selected.

6.5.2 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

6.5.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled

by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in [Table 15](#).

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 15. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

- a = 1 for $\frac{1}{2}$ bias
- a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with [Equation 1](#):

$$V_{on(RMS)} = \frac{V_{LCD}}{n} \sqrt{\frac{a^2 + 2a + n}{(1+a)^2}} \quad (1)$$

where the values for n are

- n = 1 for static drive mode
- n = 2 for 1:2 multiplex drive mode
- n = 3 for 1:3 multiplex drive mode
- n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with [Equation 2](#):

$$V_{off(RMS)} = \frac{V_{LCD}}{n} \sqrt{\frac{a^2 - 2a + n}{(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from [Equation 3](#):

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using [Equation 3](#), the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{4\sqrt{3}}{3} \right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

6.5.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see [Figure 10](#). For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see [Equation 1](#) to [Equation 3](#)) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes just named V_{th} . $V_{th(on)}$ is sometimes named saturation voltage V_{sat} .

It is important to match the module properties to those of the driver in order to achieve optimum performance.

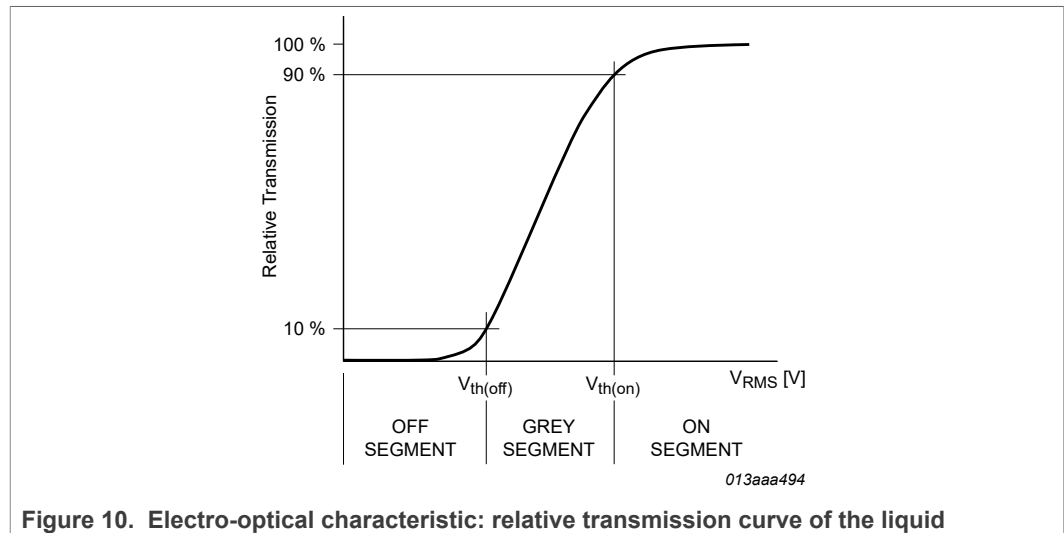


Figure 10. Electro-optical characteristic: relative transmission curve of the liquid

6.5.4 LCD drive mode waveforms

6.5.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment (Sn) drive waveforms for this mode are shown in [Figure 11](#).

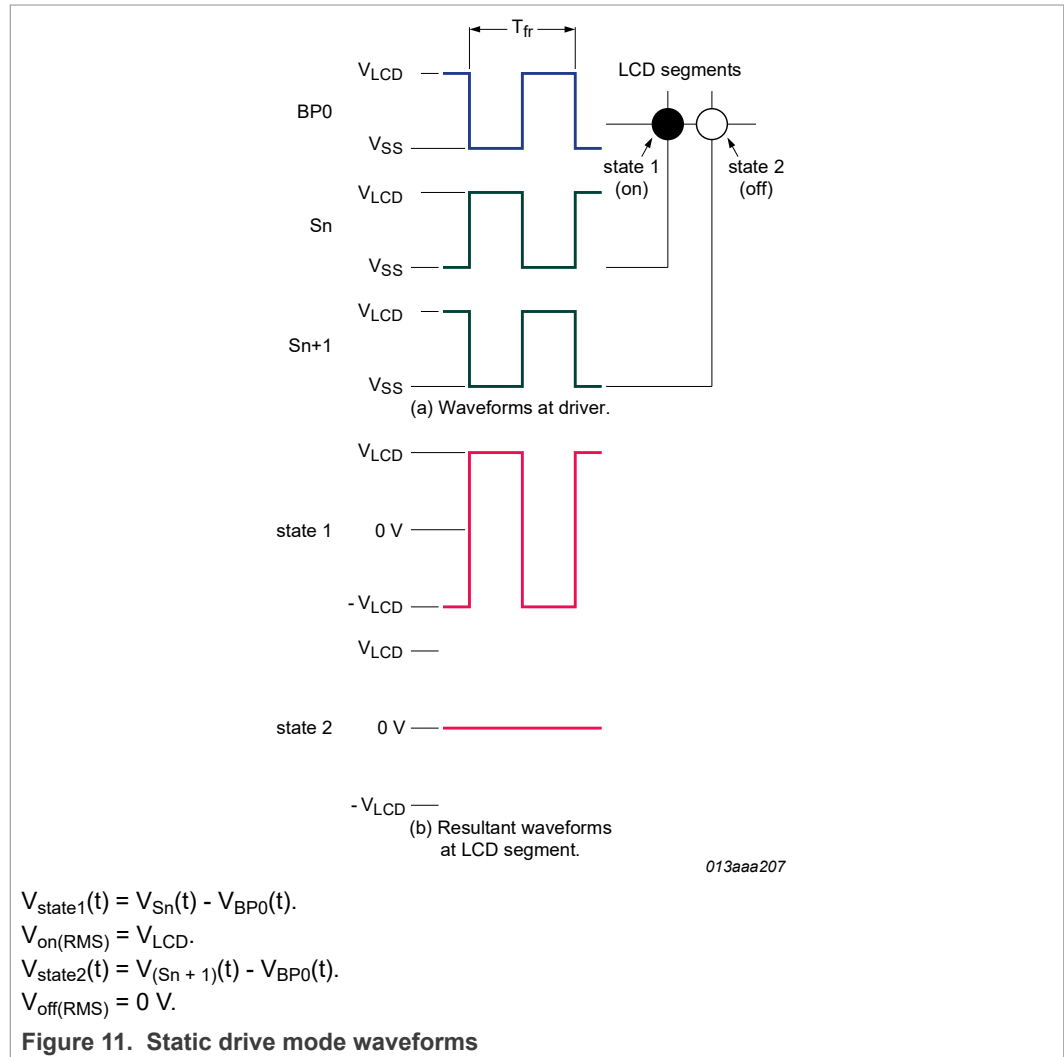
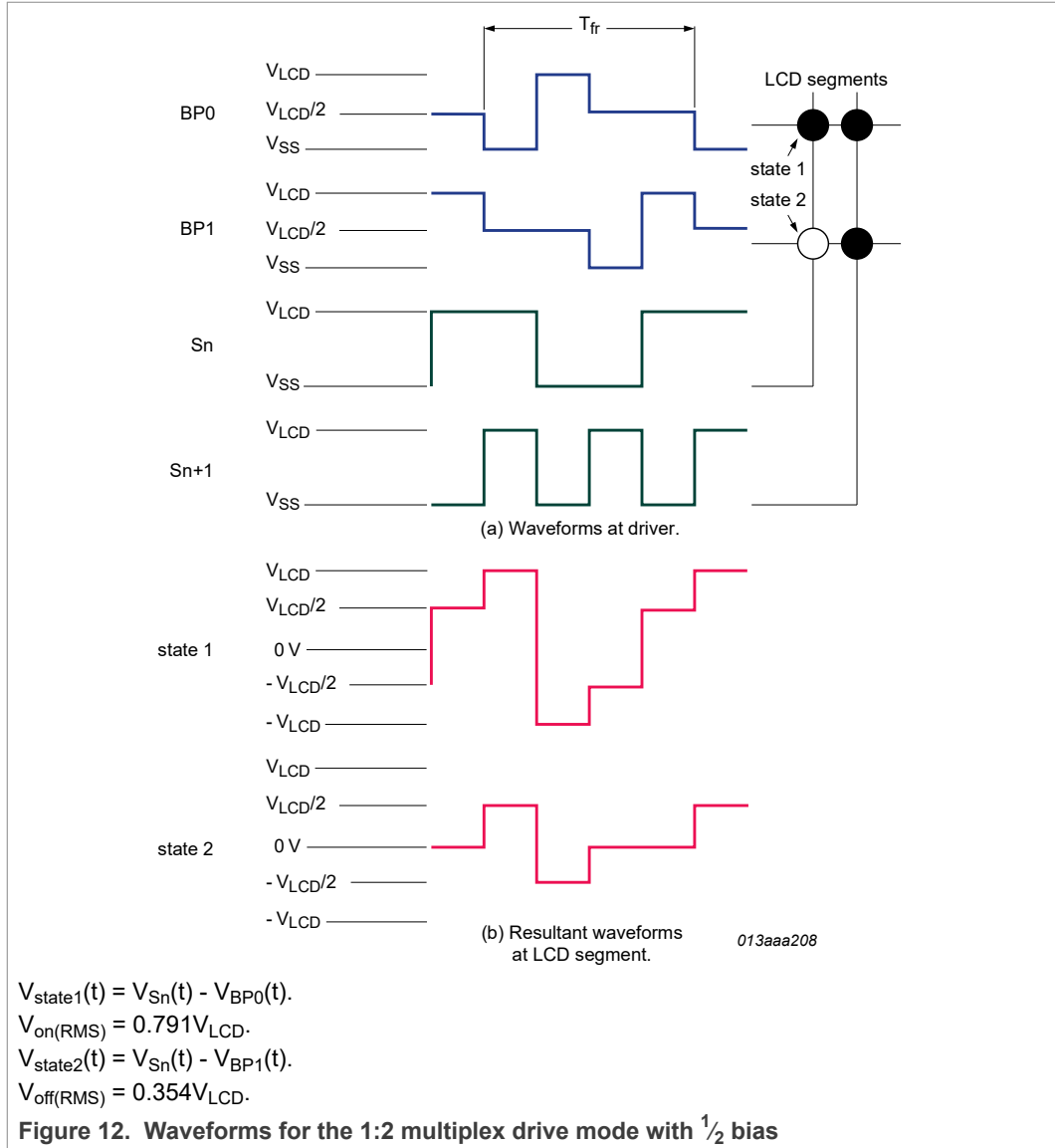
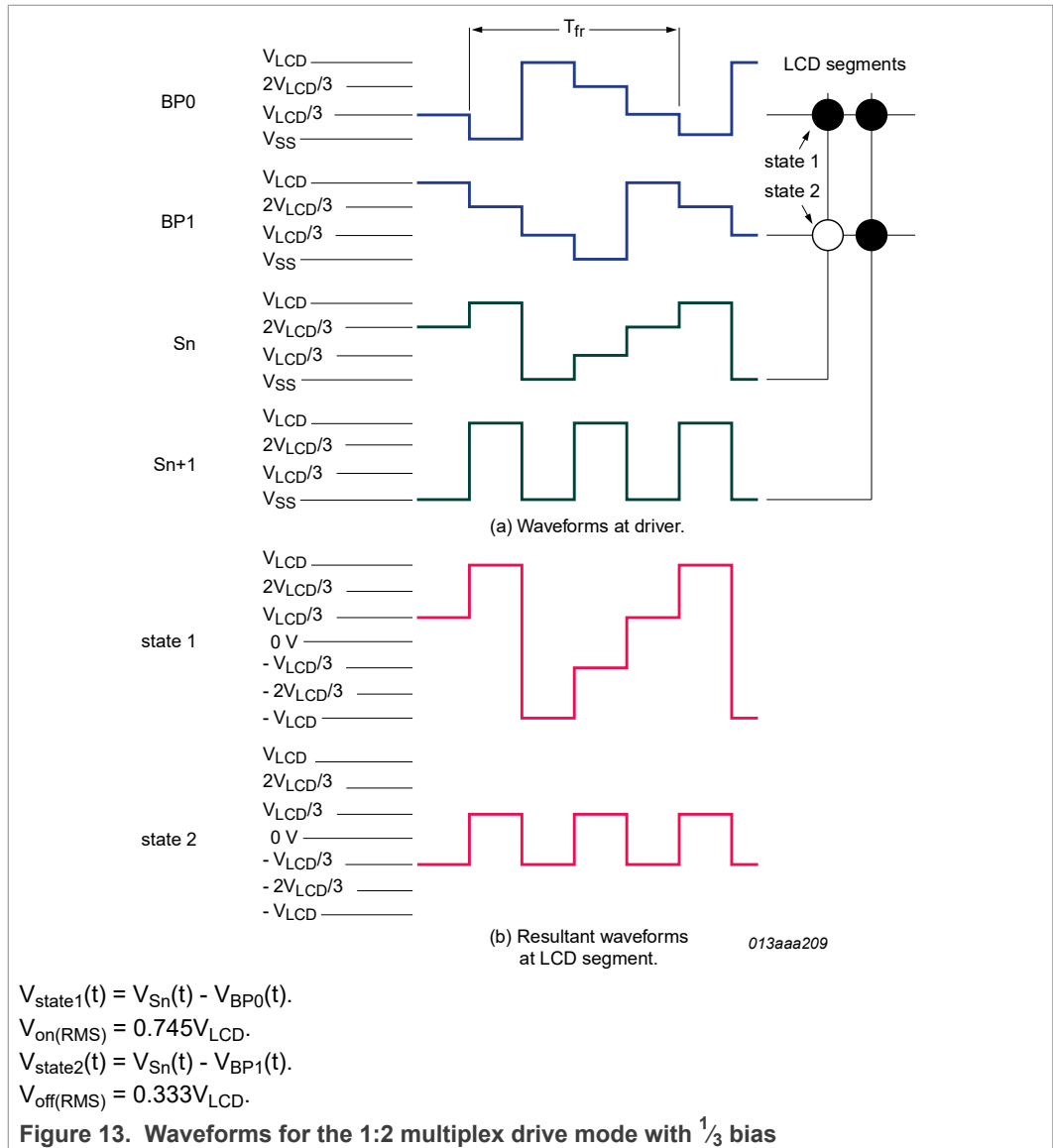


Figure 11. Static drive mode waveforms

6.5.4.2 1:2 Multiplex drive mode

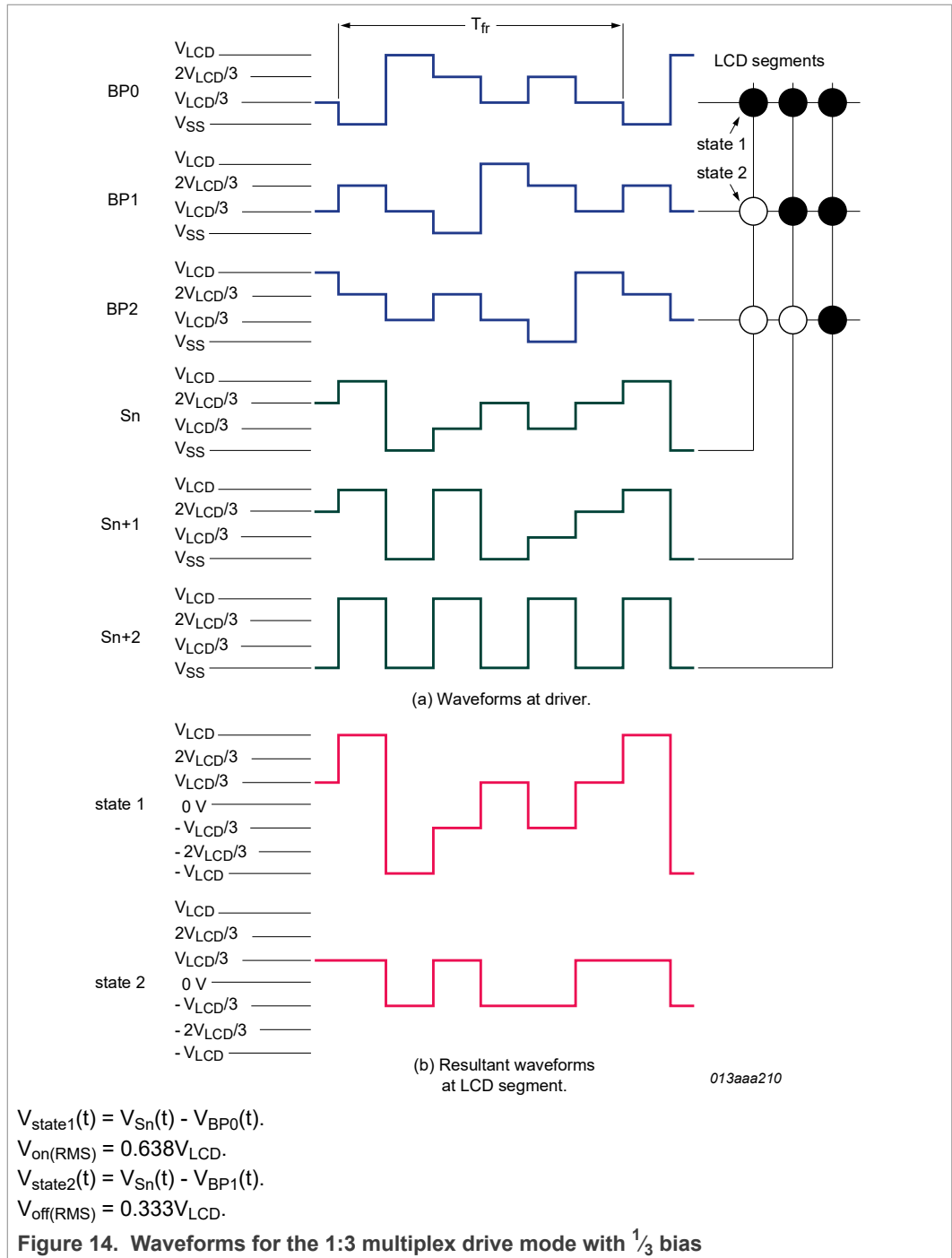
When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCA85276 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in [Figure 12](#) and [Figure 13](#).





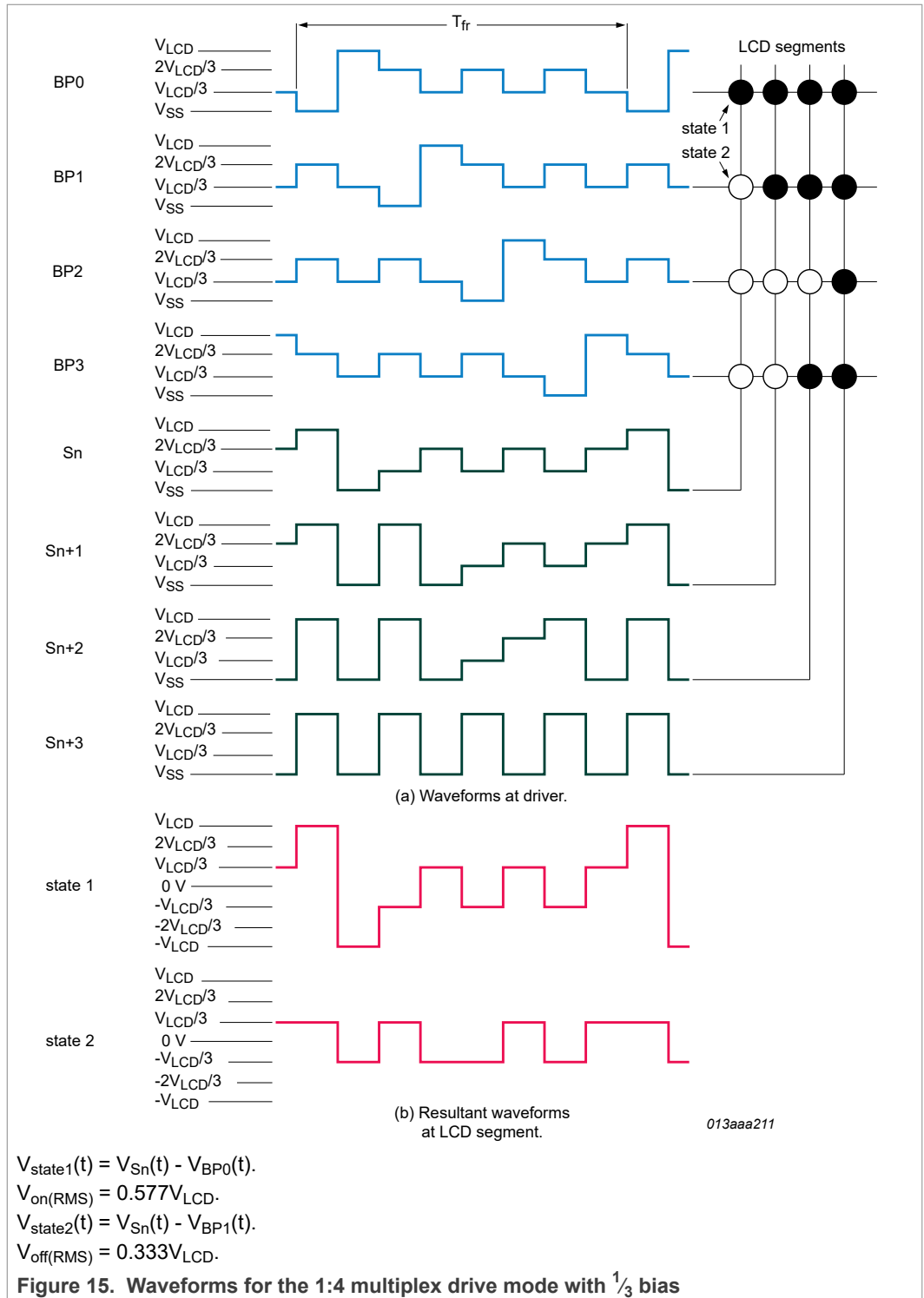
6.5.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in [Figure 14](#).



6.5.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in [Figure 15](#).



6.6 Backplane and segment outputs

6.6.1 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities
- In 1:2 multiplex drive mode, BP0 and BP2, respectively, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements

6.6.2 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DATA line (SDA) and a Serial CLOCK line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time is interpreted as a control signal (see [Figure 16](#)).

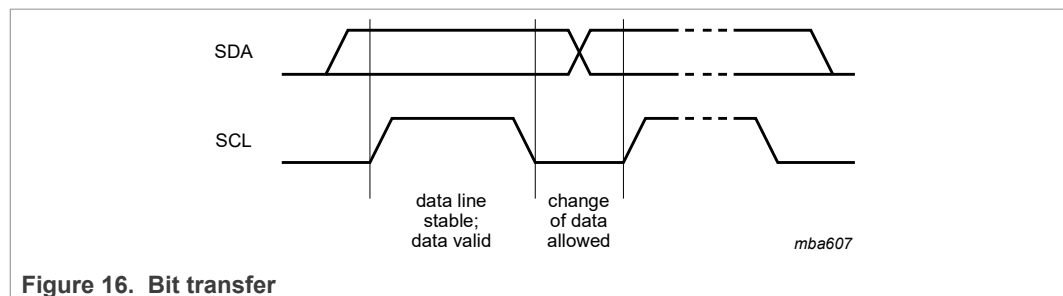


Figure 16. Bit transfer

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P.

The START and STOP conditions are illustrated in [Figure 17](#).

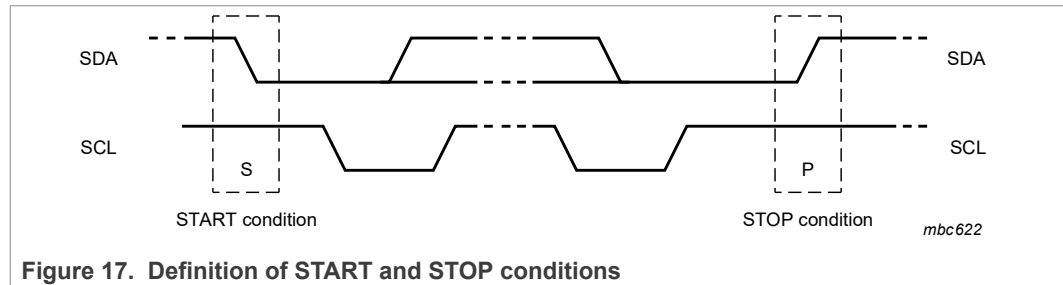


Figure 17. Definition of START and STOP conditions

7.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the controller and the devices which are controlled by the controller are the targets. The system configuration is shown in [Figure 18](#).

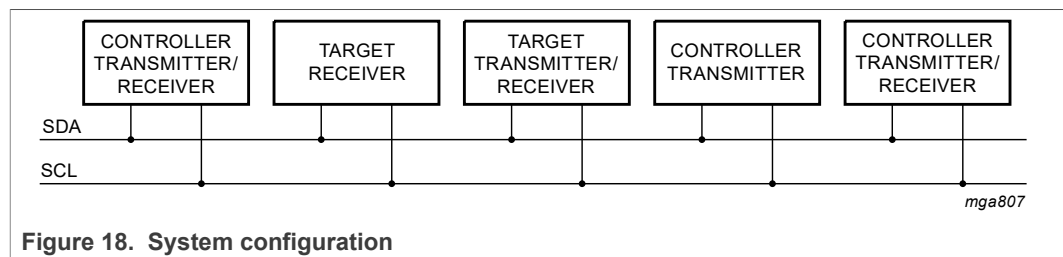


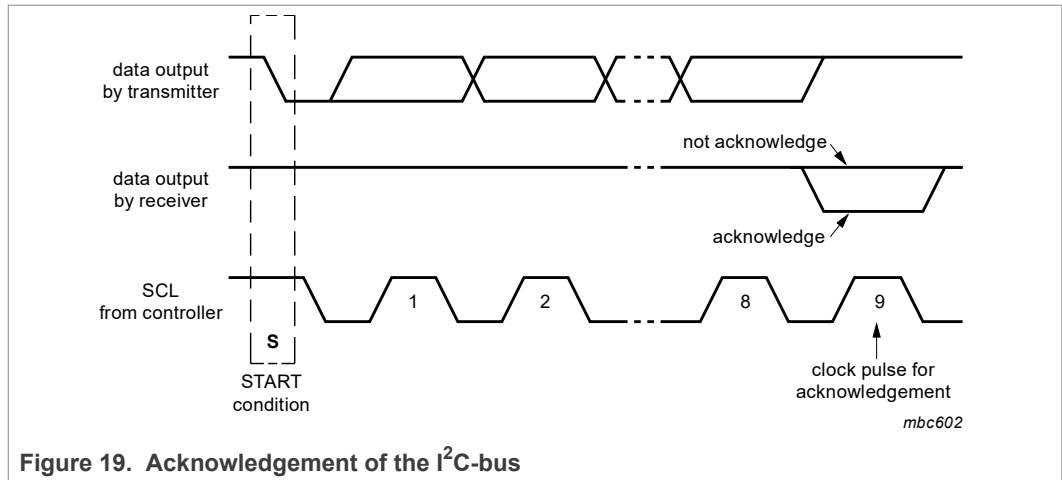
Figure 18. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A target receiver, which is addressed, must generate an acknowledge after the reception of each byte
- A controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition

Acknowledgement on the I²C-bus is illustrated in [Figure 19](#).



7.5 I²C-bus controller

The PCA85276 acts as an I²C-bus target receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus controller receiver. The only data output from the PCA85276 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus target address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0 and A1 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0 and A1 are tied to V_{SS} or V_{DD} using a binary coding scheme, so that no two devices with a common I²C-bus target address have the same hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus target addresses (0111 000 and 0111 001) are used to address the PCA85276. The entire I²C-bus target address byte is shown in [Table 16](#).

Table 16. I²C target address byte

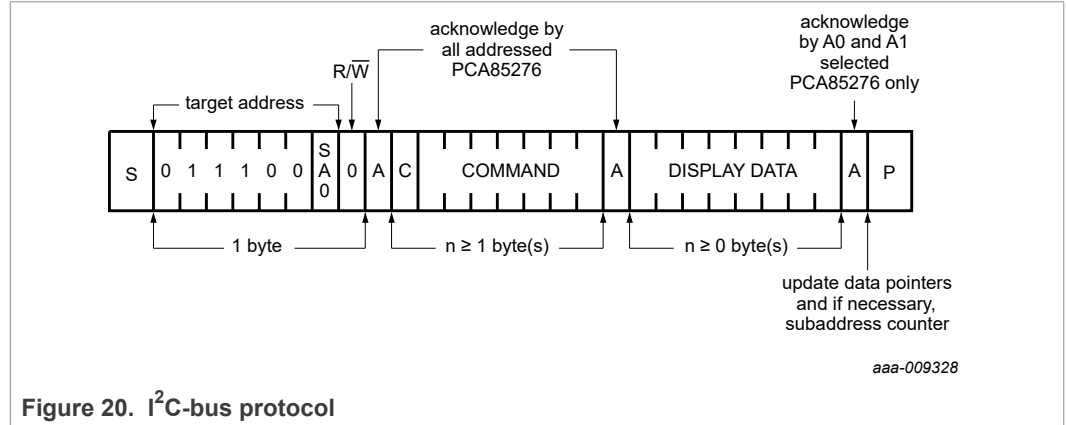
	target address							
Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	0	1	1	1	0	0	SA0	R/W

The PCA85276 is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the target address byte that a PCA85276 will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

Having two reserved target addresses allows the following on the same I²C-bus:

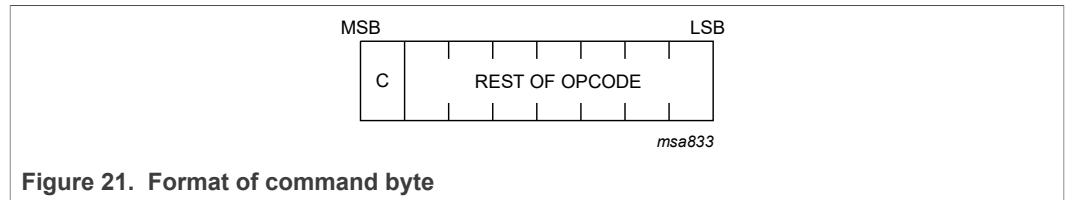
- Up to 8 PCA85276 for very large LCD applications
- The use of two types of LCD multiplex drive modes

The I²C-bus protocol is shown in Figure 20. The sequence is initiated with a START condition (S) from the I²C-bus controller which is followed by one of the two possible PCA85276 target addresses available. All PCA85276 whose SA0 inputs correspond to bit 0 of the target address respond by asserting an acknowledge in parallel. This I²C-bus transfer is ignored by all PCA85276 whose SA0 inputs are set to the alternative level.



After an acknowledgement, one or more command bytes follow that define the status of each addressed PCA85276.

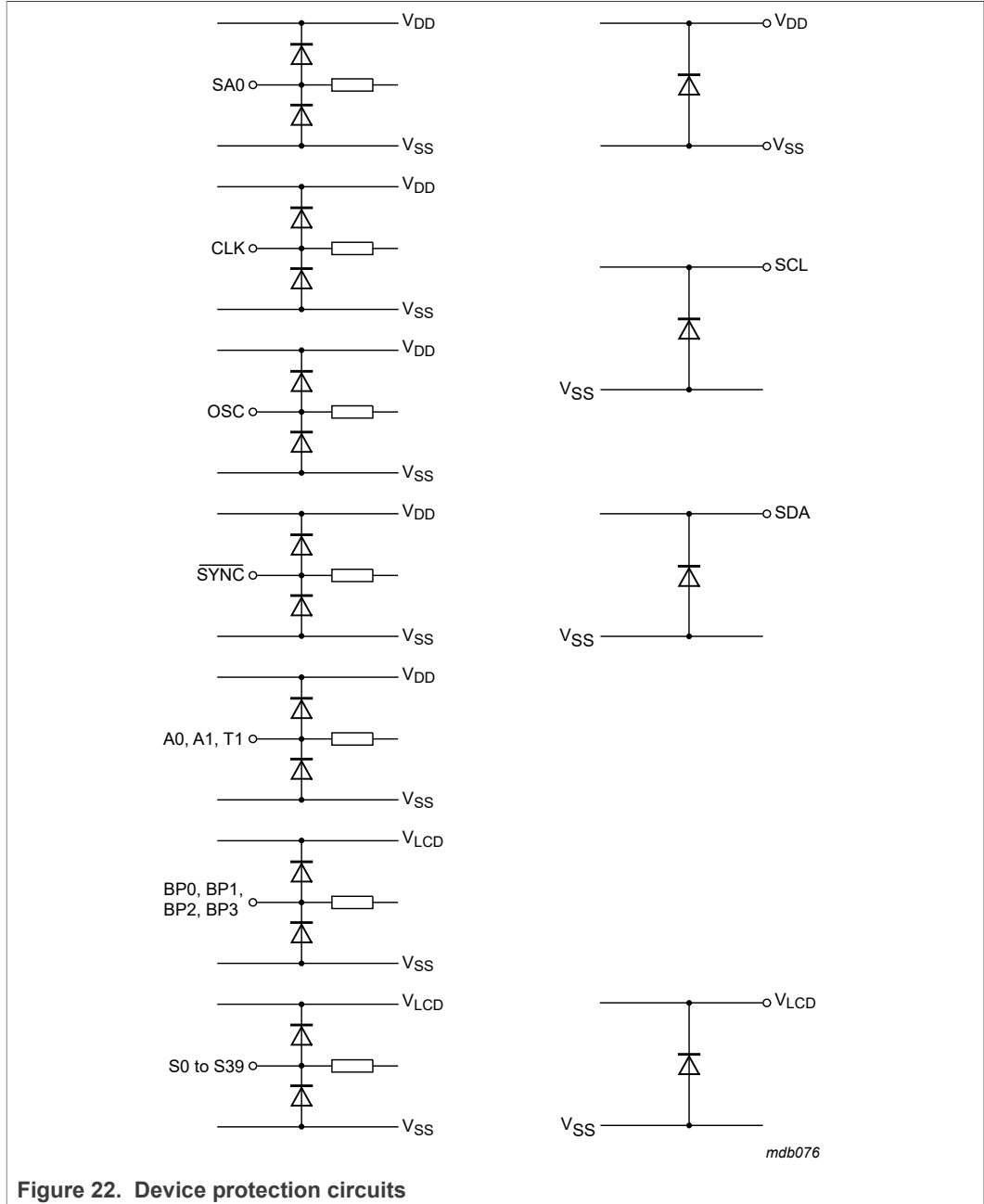
The last command byte sent is identified by resetting its most significant bit, continuation bit C (see Figure 21). The command bytes are also acknowledged by all addressed PCA85276 on the bus.



After the last command byte, one or more display data bytes may follow. Display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data directed to the intended PCA85276 device.


An acknowledgement after each byte is asserted only by the PCA85276 that are addressed via address lines A0 and A1. After the last display byte, the I²C-bus controller asserts a STOP condition (P). Alternately a START may be asserted to restart an I²C-bus access.

8 Internal circuitry




9 Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION	
	Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

10 Limiting values

Table 17. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DD}	supply voltage		-0.5	+6.5	V	
V_{LCD}	LCD supply voltage		-0.5	+9.0	V	
V_I	input voltage	on each of the pins CLK, SDA, SCL, SYNC, SA0, OSC, A0, A1, T1	-0.5	+6.5	V	
V_O	output voltage	on each of the pins S0 to S39, BP0 to BP3	-0.5	+9.0	V	
I_I	input current		-10	+10	mA	
I_O	output current		-10	+10	mA	
I_{DD}	supply current		-50	+50	mA	
$I_{DD(LCD)}$	LCD supply current		-50	+50	mA	
I_{SS}	ground supply current		-50	+50	mA	
P_{tot}	total power dissipation		-	400	mW	
P_o	output power		-	100	mW	
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±5 000	V
		CDM	[2]	-	±2 000	V
I_{lu}	latch-up current	$V_{LU} = 11.5$ V	[3]	-	200	mA
T_{stg}	storage temperature		[4]	-55	+150	°C
T_{amb}	ambient temperature	operating device		-40	+105	°C

[1] Pass level; Human Body Model (HBM), according to [1]

[2] Pass level; Charged-Device Model (CDM), according to [2]

[3] Pass level; latch-up testing according to [3] at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see [5]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

11 Static characteristics

Table 18. Static characteristics

$V_{DD} = 1.8$ V to 5.5 V; $V_{SS} = 0$ V; $V_{LCD} = 2.5$ V to 8.0 V; $T_{amb} = -40$ °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage	$V_{LCD} \leq 6.5$ V	1.8	-	5.5	V
		$V_{LCD} > 6.5$ V	2.5	-	5.5	V

Table 18. Static characteristics...continued

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }8.0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD supply voltage	$V_{DD} < 2.5\text{ V}$	2.5	-	6.5	V
		$V_{DD} \geq 2.5\text{ V}$	2.5	-	8.0	V
I_{DD}	supply current	$f_{clk(ext)} = 1536\text{ Hz}$	[1][2]	3.5	7	μA
		$V_{DD} = 3.0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2.7	-	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)} = 1536\text{ Hz}$	[1]	23	32	μA
		$V_{LCD} = 3.0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	13	-	μA
Logic ^[3]						
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0, A1, T1, SA0, SCL, SDA	V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{\text{SYNC}}$, OSC, A0, A1, T1, SA0, SCL, SDA	[4][5]	$0.7V_{DD}$	V_{DD}	V
I_{OL}	LOW-level output current	output sink current; $V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$				
		on pins CLK and $\overline{\text{SYNC}}$	1	-	-	mA
		on pin SDA	3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; $V_{OH} = 4.6\text{ V}$; $V_{DD} = 5\text{ V}$	1	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS} ; on pins CLK, SCL, SDA, A0, A1, T1, SA0	-1	-	+1	μA
$I_{L(OSC)}$	leakage current on pin OSC	$V_I = V_{DD}$	-1	-	+1	μA
C_I	input capacitance		[6]	-	7	pF
LCD outputs						
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S39	-100	-	+100	mV
R_O	output resistance	$V_{LCD} = 5\text{ V}$	[7]			
		on pins BP0 to BP3	-	1.5	-	k Ω
		on pins S0 to S39	-	6.0	-	k Ω

[1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD} ; external clock with 50 % duty factor; I²C-bus inactive.

[2] For typical values, see Figure 23.

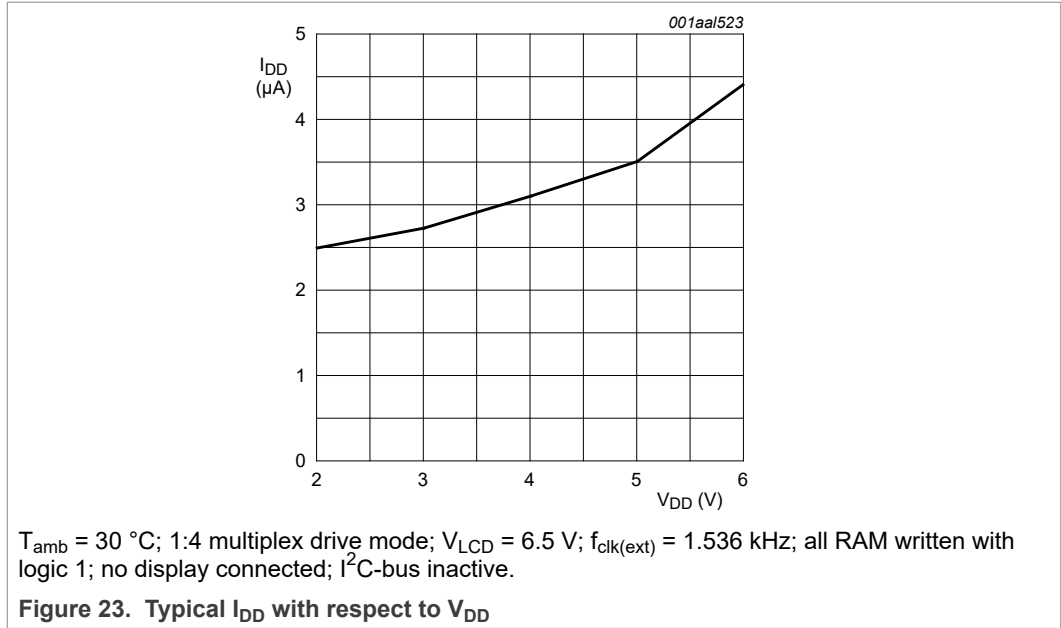
[3] The I²C-bus interface of the PCA85276 is 5 V tolerant.

[4] When tested, I²C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in Table 17 (see Figure 22 as well).

[5] Propagation delay of driver between clock (CLK) and LCD driving signals.

[6] Periodically sampled, not 100 % tested.

[7] Outputs measured one at a time.



12 Dynamic characteristics

Table 19. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = -40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f _{clk(int)}	internal clock frequency		[1] 3 505	4 800	6 240	Hz
f _{clk(ext)}	external clock frequency		960	-	6 720	Hz
f _{fr}	frame frequency	internal clock	146	200	260	Hz
		external clock	40	-	280	Hz
t _{clk(H)}	HIGH-level clock time		60	-	-	µs
t _{clk(L)}	LOW-level clock time		60	-	-	µs
Synchronization						
t _{PD(SYNC_N)}	SYNC propagation delay		-	30	-	ns
t _{SYNC_NL}	SYNC LOW time		1	-	-	µs
t _{PD(drv)}	driver propagation delay	V _{LCD} = 5 V	[2] -	-	30	µs
I²C-bus^[3]						
Pin SCL						
f _{SCL}	SCL clock frequency		-	-	400	kHz
t _{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t _{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
Pin SDA						

Table 19. Dynamic characteristics...continued

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $V_{LCD} = 2.5\text{ V to }8.0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU,DAT}$	data set-up time		100	-	-	ns
$t_{HD,DAT}$	data hold time		0	-	-	ns
Pins SCL and SDA						
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	μs
$t_{SU,STO}$	set-up time for STOP condition		0.6	-	-	μs
$t_{HD,STA}$	hold time (repeated) START condition		0.6	-	-	μs
$t_{SU,STA}$	set-up time for a repeated START condition		0.6	-	-	μs
t_r	rise time of both SDA and SCL signals	$f_{SCL} = 400\text{ kHz}$	-	-	0.3	μs
		$f_{SCL} < 125\text{ kHz}$	-	-	1.0	μs
t_f	fall time of both SDA and SCL signals		-	-	0.3	μs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{w(\text{spike})}$	spike pulse width	on the I ² C-bus	-	-	50	ns

- [1] Typical output duty factor: 50 % measured at the CLK output pin.
- [2] Not tested in production.
- [3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD} .

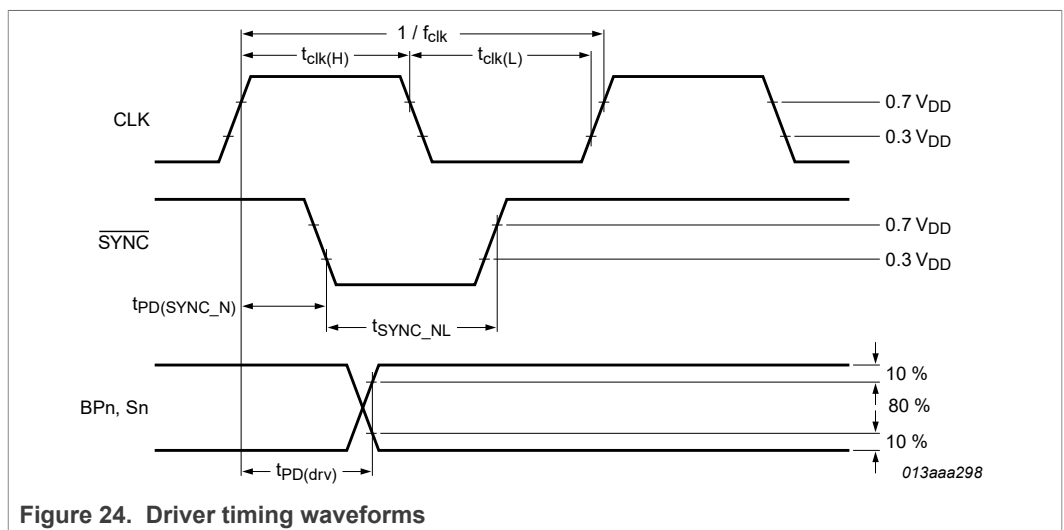
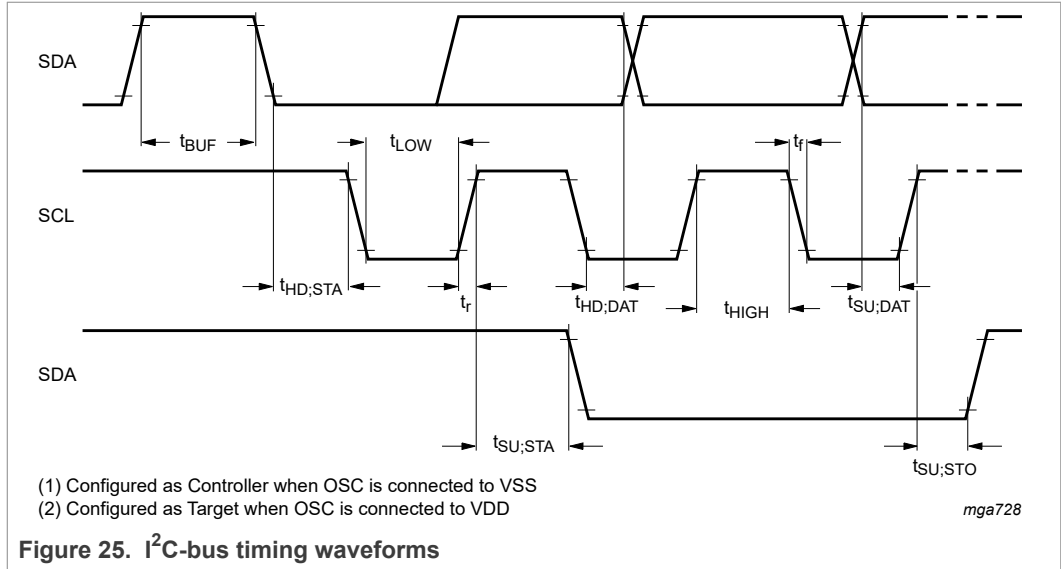


Figure 24. Driver timing waveforms



13 Application information

13.1 Cascaded operation

Large display configurations of up to 8 PCA85276 can be recognized on the same I²C-bus by using the 2-bit hardware subaddress (A0 and A1) and the programmable I²C-bus target address (SA0).

Table 20. Addressing cascaded PCA85276

Cluster	Bit SA0	Pin A1	Pin A0	Device
1	0	0	0	0
		0	1	1
		1	0	2
		1	1	3
2	1	0	0	4
		0	1	5
		1	0	6
		1	1	7

When cascaded PCA85276 are synchronized, they can share the backplane signals from one of the devices in the cascade. The other PCA85276 of the cascade contribute additional segment outputs. The backplanes can either be connected together to enhance the drive capability or some can be left open-circuit (such as the ones from the target in [Figure 26](#)) or just some of the controller and some of the target will be taken to facilitate the layout of the PCB.

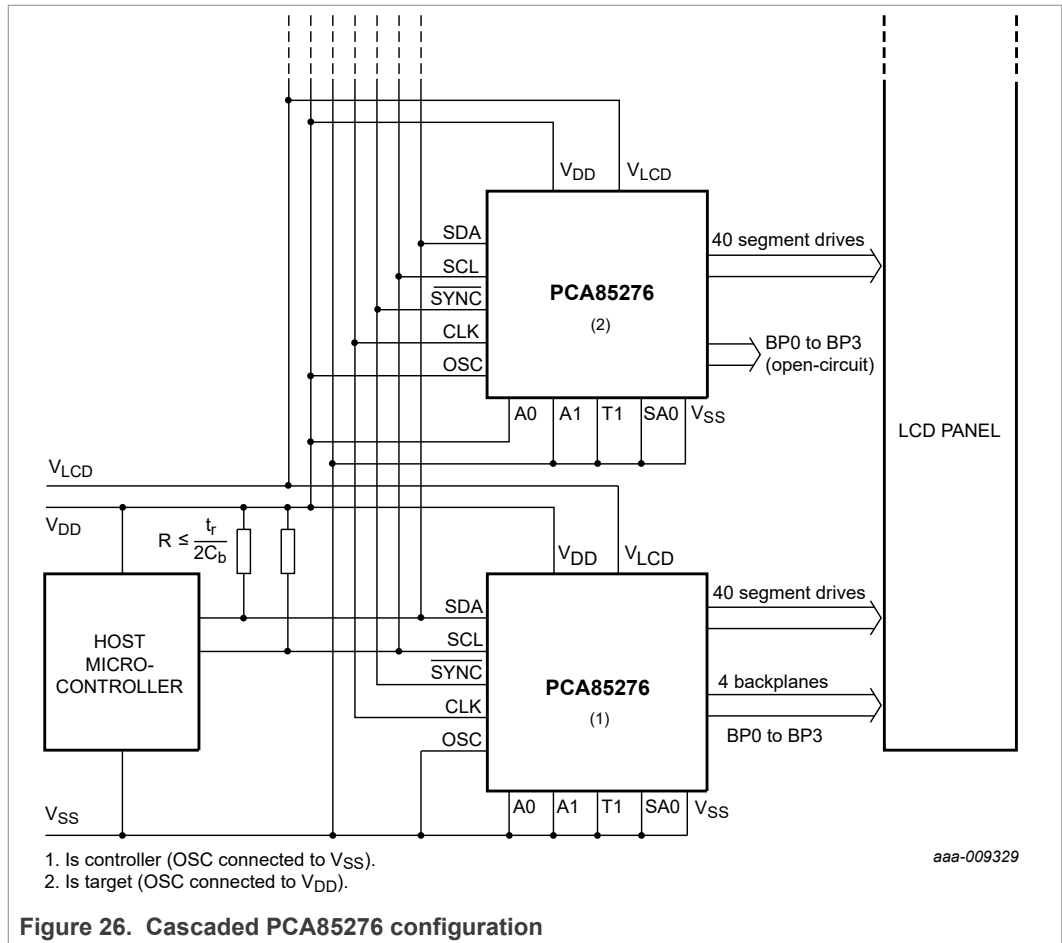


Figure 26. Cascaded PCA85276 configuration

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCA85276. Synchronization is guaranteed after a power-on and initialization. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex drive mode when PCA85276 with different SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin. The output selection is realized as an open-drain driver with an internal pull-up resistor. A PCA85276 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCA85276 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCA85276 are shown in [Figure 27](#).

The PCA85276 can always be cascaded with other devices of the same type or conditionally with other devices of the same family. This allows optimal drive selection for a given number of pixels to display. [Figure 27](#) shows the timing of the synchronization signals.

Only one controller but multiple targets are allowed in a cascade. All devices in the cascade have to use the same clock whether it is supplied externally or provided by the controller.

If an external clock source is used, all PCA85276 in the cascade must be configured such as to receive the clock from that external source (pin OSC connected to V_{DD}). Thereby it must be ensured that the clock tree is designed such that on all PCA85276

the clock propagation delay from the clock source to all PCA85276 in the cascade is as equal as possible since otherwise synchronization artifacts may occur.

In mixed cascading configurations, care has to be taken that the specifications of the individual cascaded devices are always met.

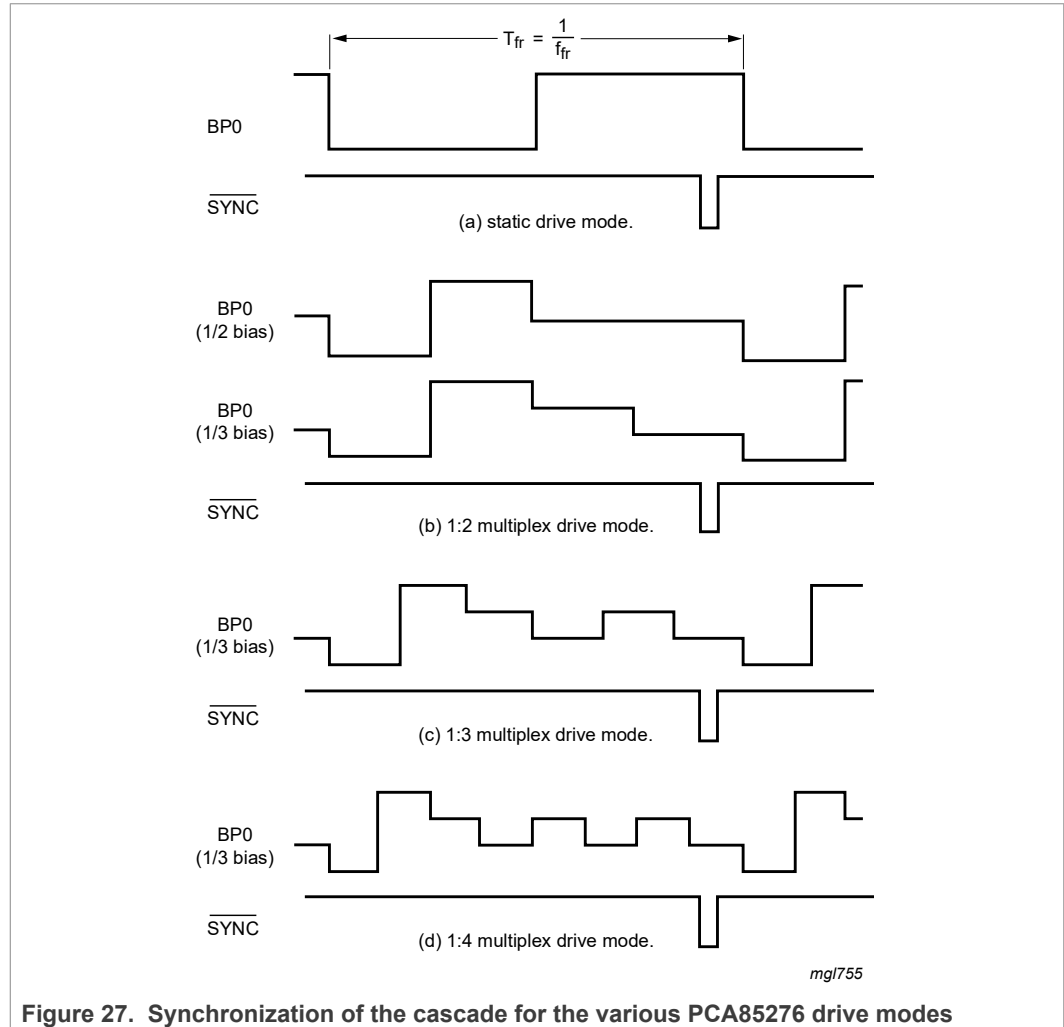


Figure 27. Synchronization of the cascade for the various PCA85276 drive modes

14 Test information

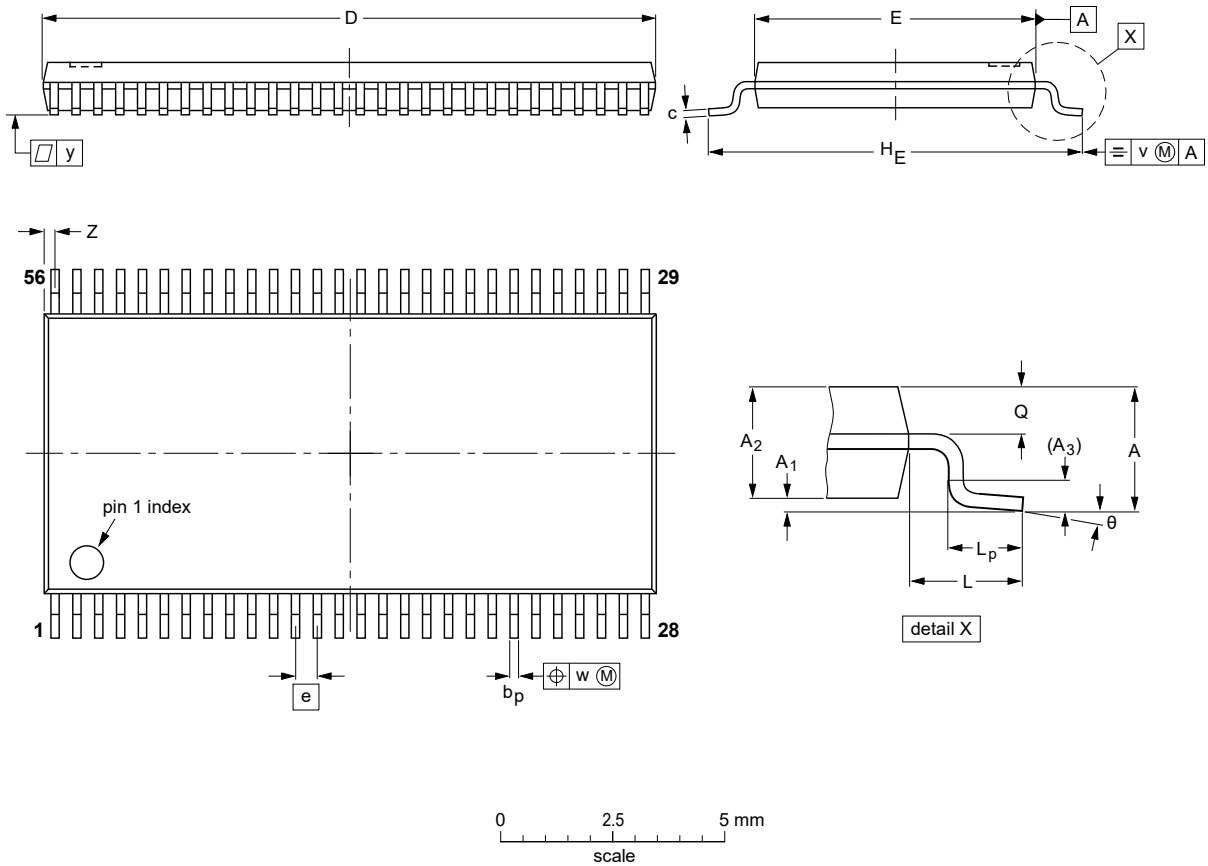
14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				99-12-27 03-02-19

Figure 28. Package outline SOT364-1 (TSSOP56) of PCA85276ATT

16 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17 Packing information

17.1 Tape and reel information

For tape and reel packing information, please see [\[4\]](#).

18 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages

- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 29](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 21](#) and [Table 22](#)

Table 21. SnPb eutectic process (from J-STD-020D)

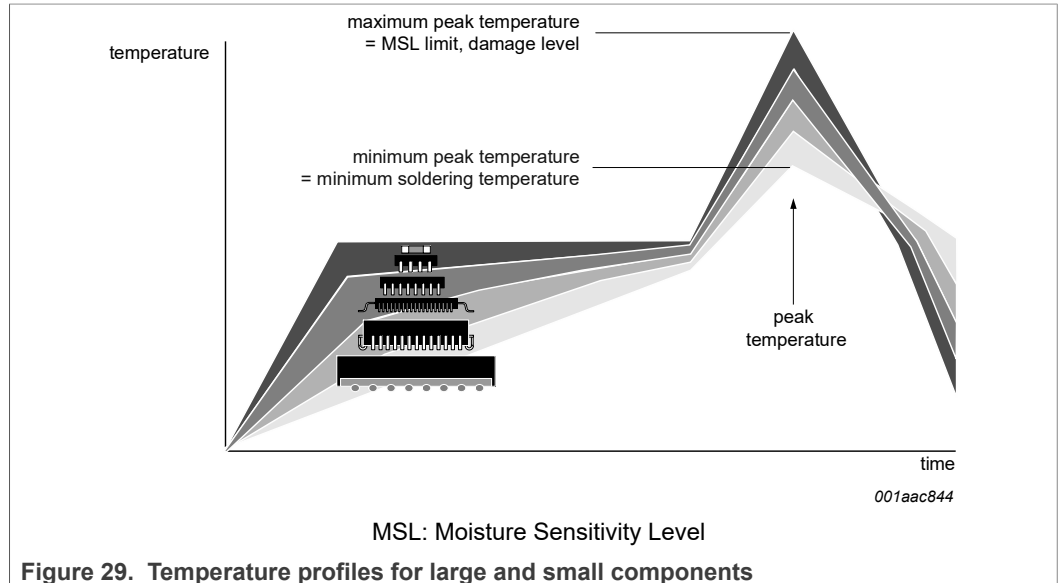
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 22. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 29](#).



For further information on temperature profiles, refer to Application Note *AN10365* “*Surface mount reflow soldering description*”.

19 Footprint information

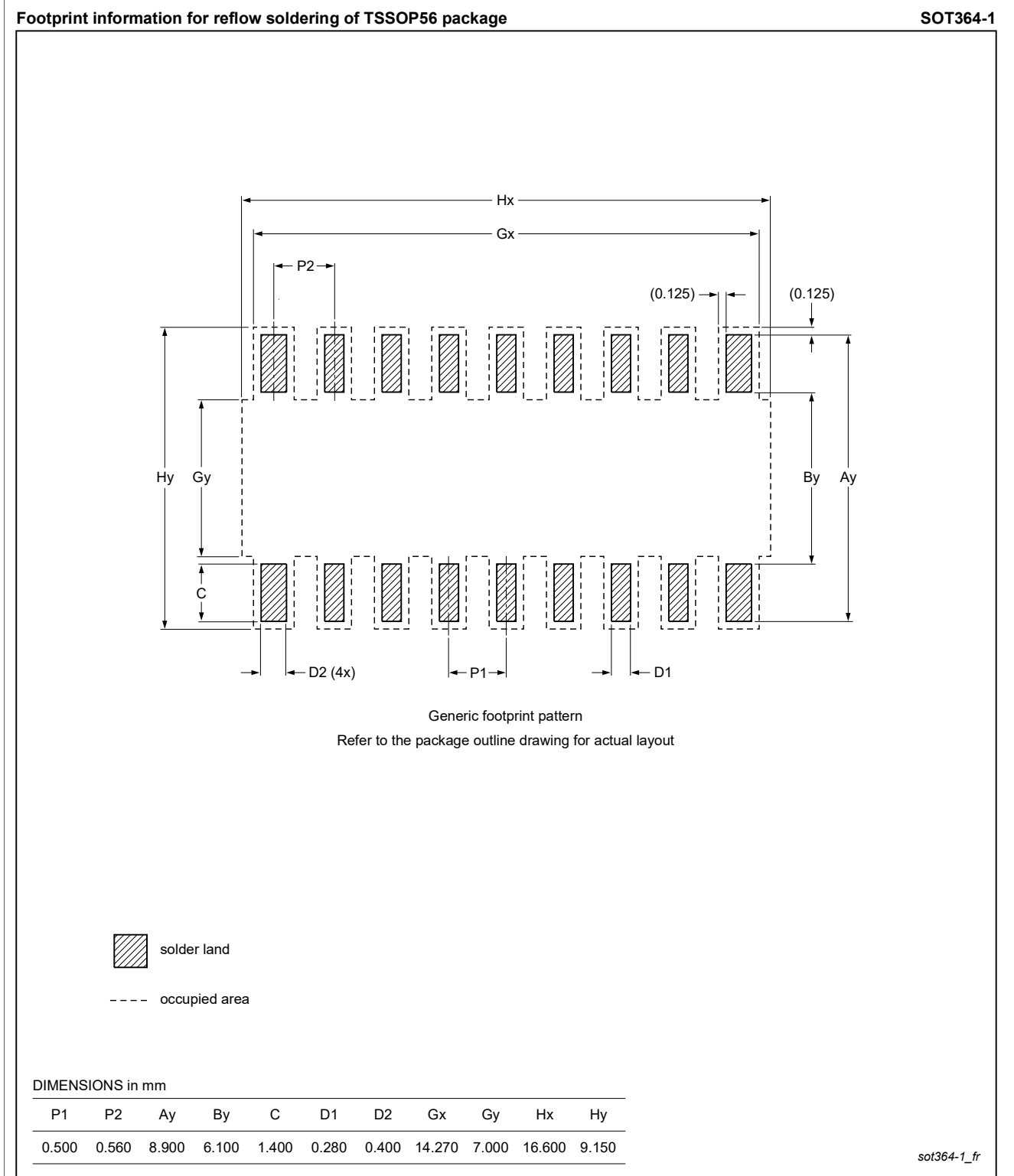


Figure 30. Footprint information for reflow soldering of SOT364-1 (TSSOP56) of PCA85276ATT

20 Appendix

20.1 LCD segment driver selection

Table 23. Selection of LCD segment drivers

Type name	Number of elements at MUX							V _{DD} (V)	V _{LCD} (V)	f _{fr} (Hz)	V _{LCD} (V) charge pump	V _{LCD} (V) temperature compensat.	T _{amb} (°C)	Interface	Package	AEC- Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256 ^[1]	N	N	-40 to 105	I ² C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 95	I ² C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 95	I ² C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	-40 to 85	I ² C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	-40 to 95	I ² C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 105	I ² C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300 ^[1]	N	N	-40 to 85	I ² C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300 ^[1]	N	N	-40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 85	I ² C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 95	I ² C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	N	N	-40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 85	I ² C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 95	I ² C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 105	I ² C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300 ^[1]	Y	Y	-40 to 105	I ² C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	-40 to 85	I ² C	Bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	-40 to 85	I ² C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	-40 to 105	I ² C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110 ^[2]	N	N	-40 to 85	I ² C	Bare die	N

Table 23. Selection of LCD segment drivers...continued

Type name	Number of elements at MUX							V _{DD} (V)	V _{LCD} (V)	f _{fr} (Hz)	V _{LCD} (V) charge pump	V _{LCD} (V) temperature compensat.	T _{amb} (°C)	Interface	Package	AEC- Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110 ^[2]	N	N	-40 to 95	I ² C	Bare die	Y
PCA85233UG	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220 ^[2]	N	N	-40 to 105	I ² C	Bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90 ^[1]	N	N	-40 to 85	I ² C	Bare die	N
PCA8530DUG	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300 ^[1]	Y	Y	-40 to 105	I ² C / SPI	Bare die	Y
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90 ^[1]	N	N	-40 to 95	I ² C	Bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176 ^[1]	N	N	-40 to 95	I ² C	Bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300 ^[1]	Y	Y	-40 to 85	I ² C / SPI	Bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300 ^[1]	Y	Y	-40 to 105	I ² C / SPI	Bare die	Y

[1] Software programmable.

[2] Hardware selectable.

21 Abbreviations

Table 24. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CMOS	Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DC	Direct Current
HBM	Human Body Model
I ² C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RAM	Random Access Memory
RC	Resistance and Capacitance
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DATa Line
SMD	Surface-Mount Device

22 References

- [1] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [2] JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [3] JESD78 IC Latch-Up Test
- [4] SOT364-1_118 TSSOP56; Reel pack; SMD, 13", packing information
- [5] UM10569 Store and transport requirements

23 Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA85276 v.4	20210929	Product data sheet	PCN202102010F01	PCA85276 v.3
Modifications:	<ul style="list-style-type: none"> Updated Section 3. See Change notice column. Global: The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy. 			
PCA85276 v.3	20181112	Product data sheet	201811010I	PCA85276 v.2
Modifications:	<ul style="list-style-type: none"> Updated Section 6.4 Updated layout of Section 3 			
PCA85276 v.2	20150409	Product data sheet	-	PCA85276 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Changed pin configuration due to redesign Enhanced SYNC pin description in Table 3 Changed typical value of I_{DD} and I_{DD(LCD)} in Table 18 Adjusted description of initialization (Section 6.4) 			
PCA85276 v.1	20140211	Product data sheet	-	-

24 Legal information

24.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Tables

Tab. 1.	Ordering information	2	Tab. 13.	Entire RAM filling by rewriting in 1:3 multiplex drive mode	13
Tab. 2.	Ordering options	2	Tab. 14.	Selection of possible display configurations	17
Tab. 3.	Pin description of PCA85276ATT (TSSOP56)	5	Tab. 15.	Biasing characteristics	18
Tab. 4.	Definition of the PCA85276 commands	5	Tab. 16.	I2C target address byte	27
Tab. 5.	C bit description	6	Tab. 17.	Limiting values	30
Tab. 6.	Mode-set command bit description	6	Tab. 18.	Static characteristics	30
Tab. 7.	Load-data-pointer command bit description	7	Tab. 19.	Dynamic characteristics	32
Tab. 8.	Device-select command bit description	7	Tab. 20.	Addressing cascaded PCA85276	34
Tab. 9.	Bank-select command bit description	7	Tab. 21.	SnPb eutectic process (from J-STD-020D)	39
Tab. 10.	Blink-select command bit description	8	Tab. 22.	Lead-free process (from J-STD-020D)	39
Tab. 11.	Blink frequencies	8	Tab. 23.	Selection of LCD segment drivers	43
Tab. 12.	Standard RAM filling in 1:3 multiplex drive mode	12	Tab. 24.	Abbreviations	45
			Tab. 25.	Revision history	46

Figures

Fig. 1.	Block diagram of PCA85276	3	Fig. 15.	Waveforms for the 1:4 multiplex drive mode with 1/3 bias	24
Fig. 2.	Pinning diagram for PCA85276ATT (TSSOP56)	4	Fig. 16.	Bit transfer	25
Fig. 3.	Display RAM bitmap	10	Fig. 17.	Definition of START and STOP conditions	26
Fig. 4.	Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I2C-bus	11	Fig. 18.	System configuration	26
Fig. 5.	RAM banks in static and multiplex driving mode 1:2	14	Fig. 19.	Acknowledgement of the I2C-bus	27
Fig. 6.	Bank selection	15	Fig. 20.	I2C-bus protocol	28
Fig. 7.	Example of the Bank-select command with multiplex drive mode 1:2	15	Fig. 21.	Format of command byte	28
Fig. 8.	Example of displays suitable for PCA85276	16	Fig. 22.	Device protection circuits	29
Fig. 9.	Typical system configuration	17	Fig. 23.	Typical IDD with respect to VDD	32
Fig. 10.	Electro-optical characteristic: relative transmission curve of the liquid	19	Fig. 24.	Driver timing waveforms	33
Fig. 11.	Static drive mode waveforms	20	Fig. 25.	I2C-bus timing waveforms	34
Fig. 12.	Waveforms for the 1:2 multiplex drive mode with 1/2 bias	21	Fig. 26.	Cascaded PCA85276 configuration	35
Fig. 13.	Waveforms for the 1:2 multiplex drive mode with 1/3 bias	22	Fig. 27.	Synchronization of the cascade for the various PCA85276 drive modes	36
Fig. 14.	Waveforms for the 1:3 multiplex drive mode with 1/3 bias	23	Fig. 28.	Package outline SOT364-1 (TSSOP56) of PCA85276ATT	37
			Fig. 29.	Temperature profiles for large and small components	40
			Fig. 30.	Footprint information for reflow soldering of SOT364-1 (TSSOP56) of PCA85276ATT	41

Contents

1	General description	1	8	Internal circuitry	29
2	Features and benefits	1	9	Safety notes	29
3	Ordering information	2	10	Limiting values	30
3.1	Ordering options	2	11	Static characteristics	30
4	Block diagram	3	12	Dynamic characteristics	32
5	Pinning information	4	13	Application information	34
5.1	Pinning	4	13.1	Cascaded operation	34
5.2	Pin description	5	14	Test information	36
6	Functional description	5	14.1	Quality information	36
6.1	Commands of PCA85276	5	15	Package outline	37
6.1.1	Command: mode-set	6	16	Handling information	38
6.1.2	Command: load-data-pointer	6	17	Packing information	38
6.1.3	Command: device-select	7	17.1	Tape and reel information	38
6.1.4	Command: bank-select	7	18	Soldering of SMD packages	38
6.1.5	Command: blink-select	7	18.1	Introduction to soldering	38
6.1.5.1	Blinking	8	18.2	Wave and reflow soldering	38
6.2	Clock and frame frequency	9	18.3	Wave soldering	39
6.2.1	Internal clock	9	18.4	Reflow soldering	39
6.2.2	External clock	9	19	Footprint information	41
6.2.3	Timing	9	20	Appendix	42
6.3	Display RAM	9	20.1	LCD segment driver selection	42
6.3.1	Data pointer	12	21	Abbreviations	45
6.3.2	Subaddress counter	12	22	References	45
6.3.3	RAM writing in 1:3 multiplex drive mode	12	23	Revision history	46
6.3.4	Writing over the RAM address boundary	13	24	Legal information	47
6.3.5	Bank selection	14			
6.3.5.1	Output bank selector	14			
6.3.5.2	Input bank selector	14			
6.3.5.3	RAM bank switching	14			
6.4	Initialization	15			
6.4.1	Device initialization	15			
6.4.2	Device setup	16			
6.5	Possible display configurations	16			
6.5.1	LCD bias generator	17			
6.5.2	Display register	17			
6.5.3	LCD voltage selector	17			
6.5.3.1	Electro-optical performance	19			
6.5.4	LCD drive mode waveforms	20			
6.5.4.1	Static drive mode	20			
6.5.4.2	1:2 Multiplex drive mode	20			
6.5.4.3	1:3 Multiplex drive mode	22			
6.5.4.4	1:4 Multiplex drive mode	23			
6.6	Backplane and segment outputs	25			
6.6.1	Backplane outputs	25			
6.6.2	Segment outputs	25			
7	Characteristics of the I2C-bus	25			
7.1	Bit transfer	25			
7.2	START and STOP conditions	25			
7.3	System configuration	26			
7.4	Acknowledge	26			
7.5	I2C-bus controller	27			
7.6	Input filters	27			
7.7	I2C-bus protocol	27			

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