

CD54/74HC4511 CD54/74HCT4511

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}): (Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F,H)	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F,H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	-55 to $+125^\circ$ C
PACKAGE TYPE E,M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE (T_{STG})	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ$ C

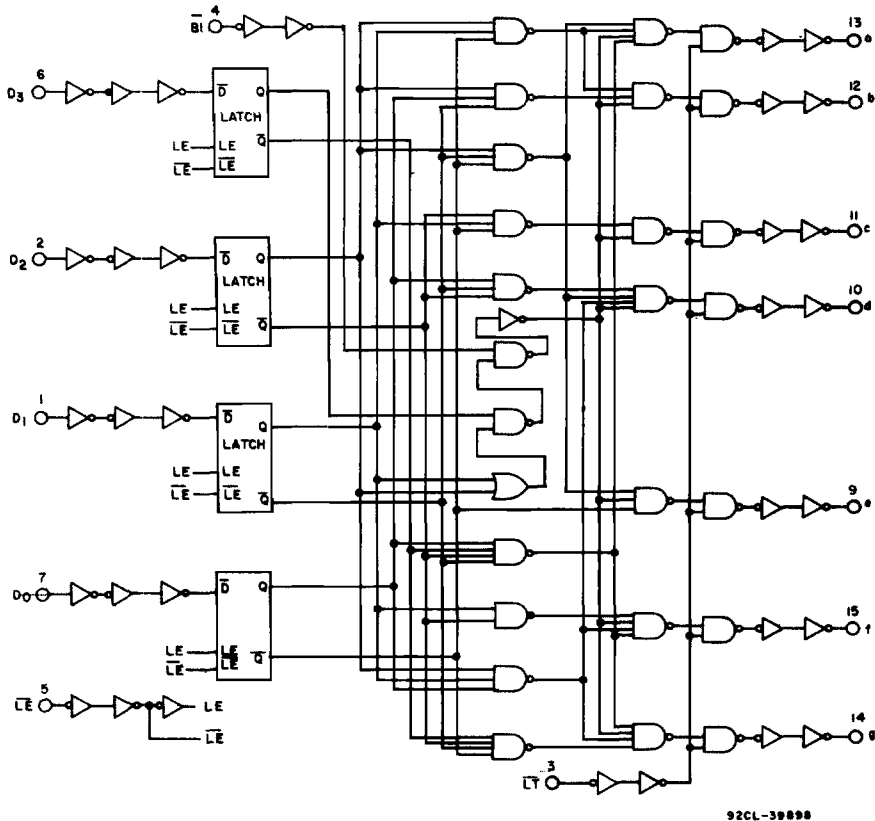


Fig. 1 - Logic diagram.

CD54/74HC4511
CD54/74HCT4511

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4511/CD54HC4511										CD74HCT4511/CD54HCT4511								UNITS			
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES				
	V _i V	I _o mA	V _{cc} V	+25° C			-40/ +85° C		-55/ +125° C		V _i V	V _{cc} V	+25° C			-40/ +85° C		-55/ +125° C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage	V _{IH}		2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—												
			6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage	V _{IL}		2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—											
			6	—	—	1.8	—	1.8	—	1.8	—	5.5										
High-Level Output Voltage	V _{OH}	V _{IL} or -0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or 4.5	4.5	4.4	—	—	4.4	—	4.4	—	4.4	V	
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—												
TTL Loads			6	5.9	—	—	5.9	—	5.9	—	V _{IH}											
Non-Standard Output		V _{IL} or -7.5	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL} or 4.5	3.98	—	—	3.84	—	3.7	—			V	
		V _{IH} -10	6	5.48	—	—	5.34	—	5.2	—	V _{IH}											
Low-Level Output Voltage	V _{OL}	V _{IL} or 0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or 4.5	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	V
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1												
			6	—	—	0.1	—	0.1	—	0.1	V _{IH}											
TTL Loads		V _{IL} or 4	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL} or 4.5	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	V
Standard Output		V _{IH} 5.2	6	—	—	0.26	—	0.33	—	0.4	V _{IH}											
Input Leakage Current	I _i	V _{cc} or Gnd	6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	±1	µA
Quiescent Device Current	I _{cc}	V _{cc} or Gnd	0	6	—	—	8	—	80	—	160	V _{cc} or Gnd	5.5	—	—	8	—	80	—	160	µA	
Additional Quiescent Device Current per input pin: 1 unit load	ΔI _{cc} *										V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	490	µA

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
\overline{LT} , \overline{LE}	1.5
\overline{BI} , Dn	0.3

*Unit Load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25° C.

CD54/74HC4511

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RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r , t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS ($V_{CC}=5$ V, $T_A=25^\circ$ C, Input $t_r, t_f=6$ ns)

CHARACTERISTIC	C_L (pF)	TYPICAL VALUES		UNITS	
		HC	HCT		
Propagation Delay:				ns	
D_n to Output	t_{PLH} t_{PHL}	15	25		
\overline{LE} to Output	t_{PLH} t_{PHL}	15	23		
\overline{BI} to Output	t_{PLH} t_{PHL}	15	18		
\overline{LT} to Output	t_{PLH} t_{PHL}	15	13		
Power Dissipation Capacitance*	C_{PD}	—	114	110	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage.}$$

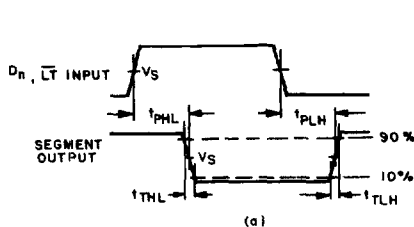
PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	LIMITS												UNITS	
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Setup Time, D_n to \overline{LE}	t_{SU}	2	—	—	—	75	—	—	—	90	—	—	—	ns	
		4.5	12	—	12	—	—	15	—	15	—	—	18		—
		6	10	—	—	—	—	13	—	—	—	—	15		—
Hold Time, D_n to \overline{LE}	t_{H1}	2	3	—	—	—	—	3	—	—	—	—	3	—	ns
		4.5	3	—	5	—	—	3	—	5	—	—	3	—	
		6	3	—	—	—	—	3	—	—	—	—	3	—	
Latch Enable Pulse Width,	t_{W}	2	80	—	—	—	—	100	—	—	—	—	120	—	MHz
		4.5	16	—	16	—	—	20	—	20	—	—	24	—	
		6	14	—	—	—	—	17	—	—	—	—	20	—	

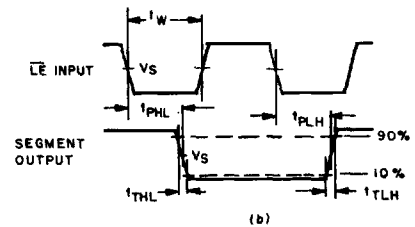
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SWITCHING CHARACTERISTICS ($C_L=50$ pF, Input $t_r, t_f=6$ ns)

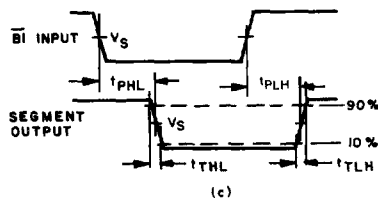
CHARACTERISTIC	V_{CC}	LIMITS												UNITS	
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay, D_n to Output	t_{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t_{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	77	—	—	
\overline{LE} to Output	t_{PLH}	2	—	270	—	—	—	340	—	—	—	405	—	—	rs
	t_{PHL}	4.5	—	54	—	54	—	68	—	68	—	81	—	81	
		6	—	46	—	—	—	58	—	—	—	69	—	—	
\overline{BI} to Output	t_{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
	t_{PHL}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
\overline{LT} to Output	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
	t_{PHL}	4.5	—	32	—	33	—	40	—	41	—	48	—	50	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF



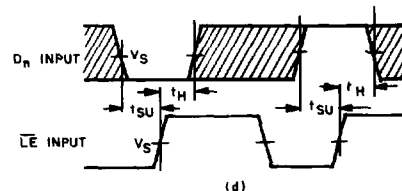
Input (D_n, \overline{LT}) to output propagation delays and output transition times



Input (\overline{LE}) to output propagation delays and latch enable pulse width



Input (\overline{BI}) to output propagation delays.



Note

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveforms showing the data set-up and hold times for D_n input to \overline{LE} input.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

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Fig. 2 - AC waveforms.