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COP472-3 Liquid Crystal Display Controller

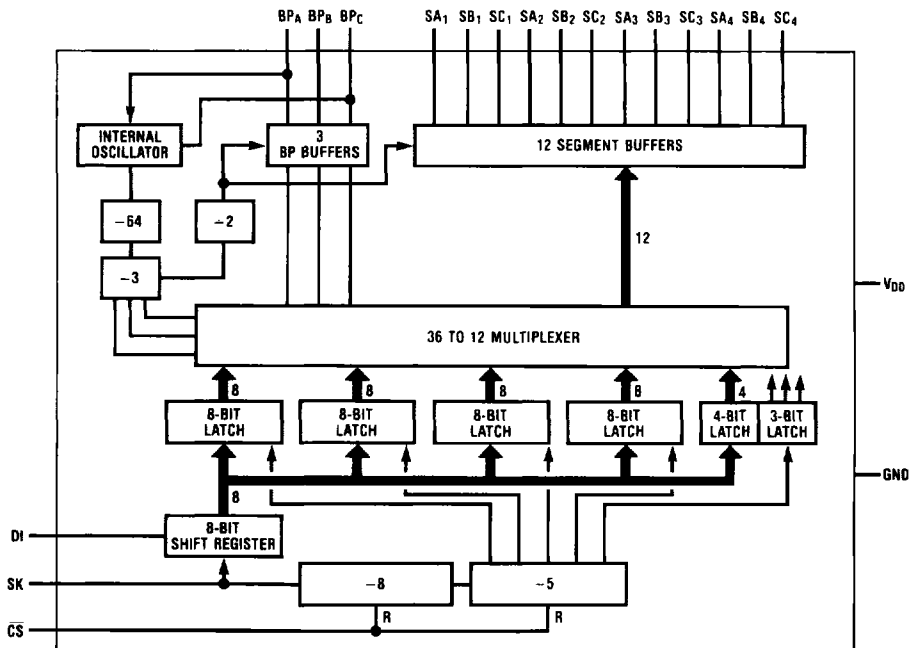
General Description

The COP472-3 Liquid Crystal Display (LCD) Controller is a peripheral member of the COPST[™] family, fabricated using CMOS technology. The COP472-3 drives a multiplexed liquid crystal display directly. Data is loaded serially and is held in internal latches. The COP472-3 contains an on-chip oscillator and generates all the multi-level waveforms for backplanes and segment outputs on a triplex display. One COP472-3 can drive 36 segments multiplexed as 3 x 12 (4½ digit display). Two COP472-3 devices can be used together to drive 72 segments (3 x 24) which could be an 8½ digit display.

Features

- Direct interface to TRIPLEX LCD
- Low power dissipation (100 μ W typ.)
- Low cost
- Compatible with all COPS processors
- Needs no refresh from processor
- On-chip oscillator and latches
- Expandable to longer displays
- Operates from display voltage
- MICROWIRE[™] compatible serial I/O
- 20-pin Dual-In-Line package and 20-pin SO

Block Diagram



TL/DD/69S2-1

Absolute Maximum Ratings

Voltage at CS, DI, SK pins $-0.3V$ to $+9.5V$
 Voltage at all other Pins $-0.3V$ to $V_{DD} + 0.3V$
 Operating Temperature Range $0^{\circ}C$ to $70^{\circ}C$

Storage Temperature $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temp. (Soldering, 10 Seconds) $300^{\circ}C$

DC Electrical Characteristics

GND = 0V, $V_{DD} = 3.0V$ to $5.5V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$ (depends on display characteristics)

| Parameter | Conditions | Min | Max | Units |
|--|--------------------|---------------------------------|---------------------------------|---------|
| Power Supply Voltage, V_{DD} | | 3.0 | 5.5 | Volts |
| Power Supply Current, I_{DD} (Note 1) | $V_{DD} = 5.5V$ | | 250 | μA |
| | $V_{DD} = 3V$ | | 100 | μA |
| Input Levels DI, SK, CS V_{IL} V_{IH} | | $0.7 V_{DD}$ | 0.8 | Volts |
| | | | 9.5 | Volts |
| BPA (as Osc. in) V_{IL} V_{IH} | | $V_{DD} - 0.6$ | 0.6 | Volts |
| | | | V_{DD} | Volts |
| Output Levels, BPC (as Osc. Out) V_{OL} V_{OH} | | $V_{DD} - 0.4$ | 0.4 | Volts |
| | | | V_{DD} | Volts |
| Backplane Outputs (BPA, BPB, BPC) $V_{BPA, BPB, BPC ON}$ $V_{BPA, BPB, BPC OFF}$ | During BP+ Time | $V_{DD} - \Delta V$ | V_{DD} | Volts |
| | | $\frac{1}{3} V_{DD} - \Delta V$ | $\frac{1}{3} V_{DD} + \Delta V$ | Volts |
| $V_{BPA, BPB, BPC ON}$ $V_{BPA, BPB, BPC OFF}$ | During BP- Time | 0 | ΔV | Volts |
| | | $\frac{2}{3} V_{DD} - \Delta V$ | $\frac{2}{3} V_{DD} + \Delta V$ | Volts |
| Segment Outputs (SA ₁ ~ SA ₄) $V_{SEG ON}$ $V_{SEG OFF}$ | During BP+ Time | 0 | ΔV | Volts |
| | | $\frac{2}{3} V_{DD} - \Delta V$ | $\frac{2}{3} V_{DD} + \Delta V$ | Volts |
| $V_{SEG ON}$ $V_{SEG OFF}$ | During BP- Time | $V_{DD} - \Delta V$ | V_{DD} | Volts |
| | | $\frac{1}{3} V_{DD} - \Delta V$ | $\frac{1}{3} V_{DD} + \Delta V$ | Volts |
| Internal Oscillator Frequency | | 15 | 80 | kHz |
| Frame Time (Int. Osc. \div 192) | | 2.4 | 12.8 | ms |
| Scan Frequency ($1/T_{SCAN}$) | | 39 | 208 | Hz |
| SK Clock Frequency | | 4 | 250 | kHz |
| SK Width | | 1.7 | | μs |
| DI Data Setup, t_{SETUP} Data Hold, t_{HOLD} | | 1.0 | | μs |
| | | 100 | | ns |
| \overline{CS} t_{SETUP} t_{HOLD} | | 1.0 | | μs |
| | | 1.0 | | μs |
| Output Loading Capacitance | | | 100 | pF |

Note 1: Power supply current is measured in stand-alone mode with all outputs open and all inputs at V_{DD} .

Note 2: $\Delta V = 0.05V_{DD}$.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------|--------------------------|
| Voltage at CS, DI, SK Pins | -0.3V to +9.5V |
| Voltage at All Other Pins | -0.3V to $V_{DD} + 0.3V$ |
| Operating Temperature Range | -40°C to +85°C |

| | |
|---|-----------------|
| Storage Temperature | -65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

DC Electrical Characteristics

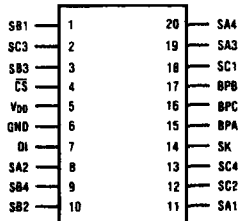
GND = 0V, V_{DD} = 3.0V to 5.5V, T_A = -40°C to +85°C (depends on display characteristics)

| Parameter | Conditions | Min | Max | Units |
|--|--------------------|--|---|----------------|
| Power Supply Voltage, V_{DD} | | 3.0 | 5.5 | Volts |
| Power Supply Current, I_{DD} (Note 1) | $V_{DD} = 5.5V$ | | 300 | μA |
| | $V_{DD} = 3V$ | | 120 | μA |
| Input Levels DI, SK, CS V_{IL} V_{IH} | | 0.7 V_{DD} | 0.8 | Volts |
| | | | 9.5 | Volts |
| BPA (as Osc. In) V_{IL} V_{IH} | | $V_{DD} - 0.6$ | 0.6 | Volts |
| | | | V_{DD} | Volts |
| Output Levels, BPC (as Osc. Out) V_{OL} V_{OH} | | $V_{DD} - 0.4$ | 0.4 | Volts |
| | | | V_{DD} | Volts |
| Backplane Outputs (BPA, BPB, BPC) $V_{BPA, BPB, BPC}$ ON $V_{BPA, BPB, BPC}$ OFF | During BP+ Time | $V_{DD} - \Delta V$ $\frac{1}{3} V_{DD} - \Delta V$ | V_{DD} $\frac{1}{3} V_{DD} + \Delta V$ | Volts Volts |
| | During BP- Time | 0 $\frac{2}{3} V_{DD} - \Delta V$ | ΔV $\frac{2}{3} V_{DD} + \Delta V$ | Volts Volts |
| Segment Outputs (SA ₁ ~ SA ₄) V_{SEG} ON V_{SEG} OFF | During BP+ Time | 0 $\frac{2}{3} V_{DD} - \Delta V$ | ΔV $\frac{2}{3} V_{DD} + \Delta V$ | Volts Volts |
| | During BP- Time | $V_{DD} - \Delta V$ $\frac{1}{3} V_{DD} - \Delta V$ | V_{DD} $\frac{1}{3} V_{DD} + \Delta V$ | Volts Volts |
| Internal Oscillator Frequency | | 15 | 80 | kHz |
| Frame Time (Int. Osc. \div 192) | | 2.4 | 12.8 | ms |
| Scan Frequency (1/ T_{SCAN}) | | 39 | 208 | Hz |
| SK Clock Frequency | | 4 | 250 | kHz |
| SK Width | | 1.7 | | μs |
| DI Data Setup, t_{SETUP} Data Hold, t_{HOLD} | | 1.0 | | μs |
| | | 100 | | ns |
| CS t_{SETUP} t_{HOLD} | | 1.0 | | μs |
| | | 1.0 | | μs |
| Output Loading Capacitance | | | 100 | pF |

Note 1: Power supply current is measured in stand-alone mode with all outputs open and all inputs at V_{DD} .

Note 2: $\Delta V = 0.05 V_{DD}$.

Dual-in-Line Package



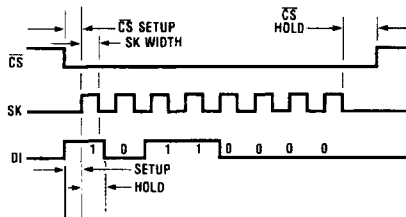
Top View

TL/DD/6932-2

| Pin | Description |
|-----------------|---|
| \overline{CS} | Chip select |
| VDD | Power supply (display voltage) |
| GND | Ground |
| DI | Serial data input |
| SK | Serial clock input |
| BPA | Display backplane A (or oscillator in) |
| BPB | Display backplane B |
| BPC | Display backplane C (or oscillator out) |
| SA1 ~ SC4 | 12 multiplexed outputs |

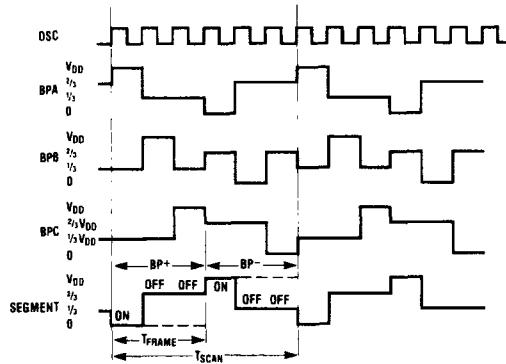
Order Number COP472MW-3 or COP472N-3
See NS Package Number M20A or N20A

FIGURE 2. Connection Diagram



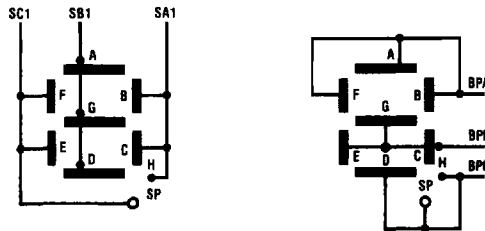
TL/DD/6932-3

FIGURE 3. Serial Load Timing Diagram



TL/DD/6932-4

FIGURE 4. Backplane and Segment Waveforms



TL/DD/6932-5

FIGURE 5. Typical Display Internal Connections
Epson LD-370

Functional Description

The COP472-3 drives 36 bits of display information organized as twelve segments and three backplanes. The COP472-3 requires 40 information bits: 36 data and 4 control. The function of each control bit is described below. Display information format is a function of the LCD interconnections. A typical segment/backplane configuration is illustrated in *Figure 5*, with this configuration the COP472-3 will drive 4 digits of 9 segments.

To adapt the COP472-3 to any LCD display configuration, the segment/backplane multiplex scheme is illustrated in Table I.

Two or more COP472-3 chips can be cascaded to drive additional segments. There is no limit to the number of COP472-3's that can be used as long as the output loading capacitance does not exceed specification.

TABLE I. COP472-3 Segment/Backplane Multiplex Scheme

| Bit Number | Segment, Backplane | Data to Numeric Display | |
|------------|--------------------|-------------------------|---------|
| 1 | SA1, BPC | SH | |
| 2 | SB1, BPB | SG | |
| 3 | SC1, BPA | SF | |
| 4 | SC1, BPB | SE | Digit 1 |
| 5 | SB1, BPC | SD | |
| 6 | SA1, BPB | SC | |
| 7 | SA1, BPA | SB | |
| 8 | SB1, BPA | SA | |
| 9 | SA2, BPC | SH | |
| 10 | SB2, BPB | SG | |
| 11 | SC2, BPA | SF | |
| 12 | SC2, BPB | SE | Digit 2 |
| 13 | SB2, BPC | SD | |
| 14 | SA2, BPB | SC | |
| 15 | SA2, BPA | SB | |
| 16 | SB2, BPA | SA | |
| 17 | SA3, BPC | SH | |
| 18 | SB3, BPB | SG | |
| 19 | SC3, BPA | SF | |
| 20 | SC3, BPB | SE | Digit 3 |
| 21 | SB3, BPC | SD | |
| 22 | SA3, BPB | SC | |
| 23 | SA3, BPA | SB | |
| 24 | SB3, BPA | SA | |
| 25 | SA4, BPC | SH | |
| 26 | SB4, BPB | SG | |
| 27 | SC4, BPA | SF | |
| 28 | SC4, BPB | SE | Digit 4 |
| 29 | SB4, BPC | SD | |
| 30 | SA4, BPB | SC | |
| 31 | SA4, BPA | SB | |
| 32 | SB4, BPA | SA | |
| 33 | SC1, BPC | SPA | Digit 1 |
| 34 | SC2, BPC | SP2 | Digit 2 |
| 35 | SC3, BPC | SP3 | Digit 3 |
| 36 | SC4, BPC | SP4 | Digit 4 |
| 37 | not used | | |
| 38 | Q6 | | |
| 39 | Q7 | | |
| 40 | SYNC | | |

SEGMENT DATA BITS

Data is loaded in serially, in sets of eight bits. Each set of segment data is in the following format:

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| SA | SB | SC | SD | SE | SF | SG | SH |
|----|----|----|----|----|----|----|----|

Data is shifted into an eight bit shift register. The first bit of the data is for segment H, digit 1. The eighth bit is segment A, digit 1. A set of eight bits is shifted in and then loaded into the digit one latches. The second set of 8 bits is loaded into digit two latches. The third set into digit three latches, and the fourth set is loaded into digit four latches.

CONTROL BITS

The fifth set of 8 data bits contains special segment data and control data in the following format:

| | | | | | | | |
|------|----|----|---|-----|-----|-----|-----|
| SYNC | Q7 | Q6 | X | SP4 | SP3 | SP2 | SP1 |
|------|----|----|---|-----|-----|-----|-----|

The first four bits shifted in contain the special character segment data. The fifth bit is not used. The sixth and seventh bits program the COP472-3 as a stand alone LCD driver or as a master or slave for cascading COP472-3's. BPC of the master is connected to BPA of each slave. The following table summarizes the function of bits six and seven:

| Q7 | Q6 | Function | BPC Output | BPA Output |
|----|----|-------------|----------------------|------------------|
| 1 | 1 | Slave | Backplane Output | Oscillator Input |
| 0 | 1 | Stand Alone | Backplane Output | Backplane Output |
| 1 | 0 | Not Used | Internal Osc. Output | Oscillator Input |
| 0 | 0 | Master | Internal Osc. Output | Backplane Output |

The eighth bit is used to synchronize two COP472-3's to drive an 8½-digit display.

LOADING SEQUENCE TO DRIVE A 4½-DIGIT DISPLAY

Steps:

1. Turn \overline{CE} low.
2. Clock in 8 bits of data for digit 1.
3. Clock in 8 bits of data for digit 2.
4. Clock in 8 bits of data for digit 3.
5. Clock in 8 bits of data for digit 4.
6. Clock in 8 bits of data for special segment and control function of BPC and BPA.

| | | | | | | | |
|---|---|---|---|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | SP4 | SP3 | SP2 | SP1 |
|---|---|---|---|-----|-----|-----|-----|

7. Turn \overline{CS} high.

Note: \overline{CS} may be turned high after any step. For example to load only 2 digits of data, do steps 1, 2, 3, and 7.

\overline{CS} must make a high to low transition before loading data in order to reset internal counters.

LOADING SEQUENCE TO DRIVE AN 8½-DIGIT DISPLAY

Two or more COP472-3's may be connected together to drive additional segments. An eight digit multiplexed display is shown in Figure 7. The following is the loading sequence to drive an eight digit display using two COP472-3's. The right chip is the master and the left the slave.

Steps:

1. Turn \overline{CS} low on both COP472-3's.
2. Shift in 32 bits of data for the slave's four digits.
3. Shift in 4 bits of special segment data: a zero and three ones.

| | | | | | | | |
|---|---|---|---|-----|-----|-----|-----|
| 1 | 1 | 1 | 0 | SP4 | SP3 | SP2 | SP1 |
|---|---|---|---|-----|-----|-----|-----|

This synchronizes both the chips and BPA is oscillator input. Both chips are now stopped.

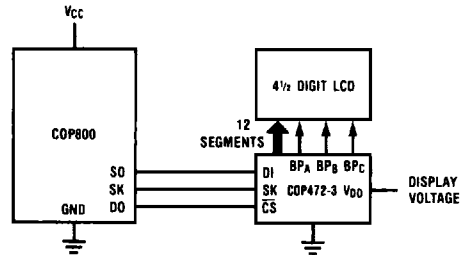
4. Turn \overline{CS} high to both chips.
5. Turn \overline{CS} low to master COP472-3.
6. Shift in 32 bits of data for the master's 4 digits.
7. Shift in four bits of special segment data, a one and three zeros.

| | | | | | | | |
|---|---|---|---|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | SP4 | SP3 | SP2 | SP1 |
|---|---|---|---|-----|-----|-----|-----|

This sets the master COP472-3 to BPA as a normal backplane output and BPC as oscillator output. Now both the chips start and run off the same oscillator.

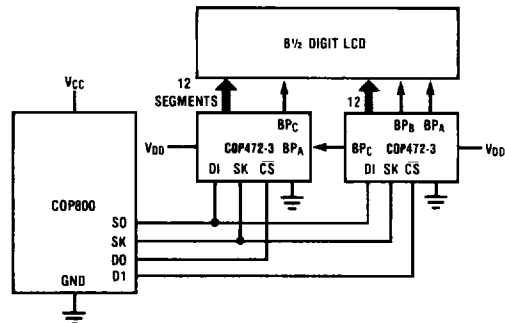
8. Turn \overline{CS} high.

The chips are now synchronized and driving 8 digits of display. To load new data simply load each chip separately in the normal manner, keeping the correct status bits to each COP472-3 (0110 or 0001).



TL/DD/6932-6

FIGURE 6. System Diagram - 4½ Digit Display



TL/DD/6932-7

FIGURE 7. System Diagram - 8½ Digit Display