CA3207, CA3208

BiMOS Sequencer Driver and Segment Latch-Driver for Vacuum Fluorescent Displays

Features:

- *Serial input, parallel output*
- *Total of 14 outputs*
- *CMOS and T^2L compatible inputs*
- *Low-power CMOS Logic–Bipolar high-voltage output BiMOS process*
- *Use with vacuum fluorescent display*
- *Will operate in an output voltage range of 35 V to 55 V*

Sequencer Driver (CA3207E)

- *Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)*
- *Signal dimming through Gates 1 or 2*

Latch Driver (CA3208E)

- *Drives any combination of 14 outputs selected by DATA input*
- *Two or more devices may be interconnected by means of the CE and $\overline{CE}$ inputs to drive more than 14 characters*

The RCA-CA3207E and CA3208E*, sequence-driver and segment latch-driver, respectively, are used in combination to drive vacuum fluorescent display devices of up to 14 segments with up to 14 characters of display. The CA3207E selects the digit or character to be displayed in sequence and the CA3208E turns on the required number of segments of the character selected.

Each sequencer-driver will sequentially activate 14 characters. The sequencer-driver clock line may be used to drive the cross-coupled $\overline{CE}$ and CE inputs of 2 segment-latch drivers to provide for the display of up to 28 characters (see Fig. 12). The logic portion of both circuits use CMOS technology operating at 5 volts. The output drivers use bipolar technology and operate at supply voltages up to 55 volts. The CA3207E will source 40-mA per character and the CA3208E will source 7.5-mA per segment.

Both types are supplied in the 22-lead dual-in-line plastic package (E suffix), and they are also available in chip form (H suffix).

*Formerly Dev. Type No. TA10563 and TA10564, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:

V_{CC}, Pin 3 to GND, Pin 10 ..... 55 V

V_{DD}, Pin 4 to GND, Pin 10 ..... 6 V

DEVICE DISSIPATION:

Up to T_A=+85°C ..... 750 mW

Above T_A=+85°C ..... 13 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... -40 to +85°C

Storage ..... -55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

File Number **1322**

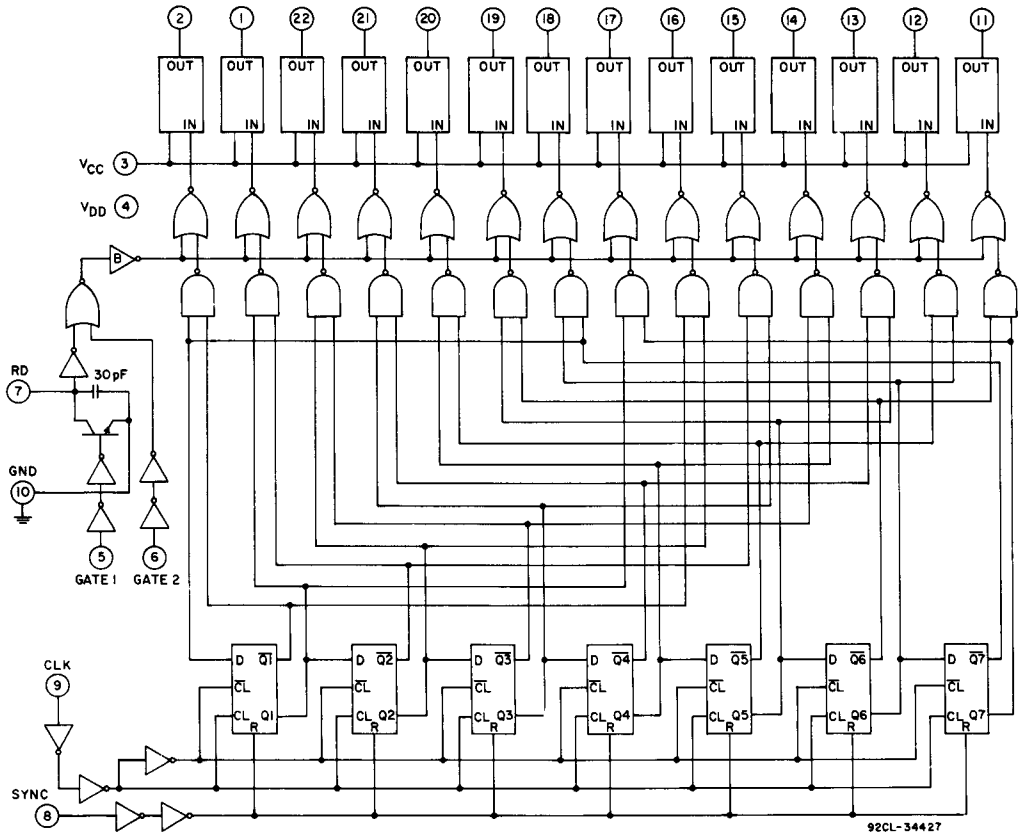
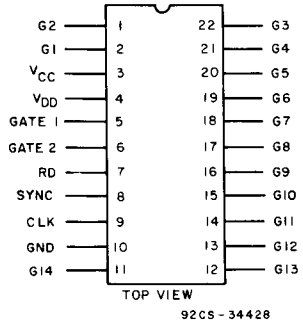


Fig. 1 - Sequencer-driver (CA3207E) logic diagram.



TERMINAL ASSIGNMENT
CA3207E

CA3207, CA3208

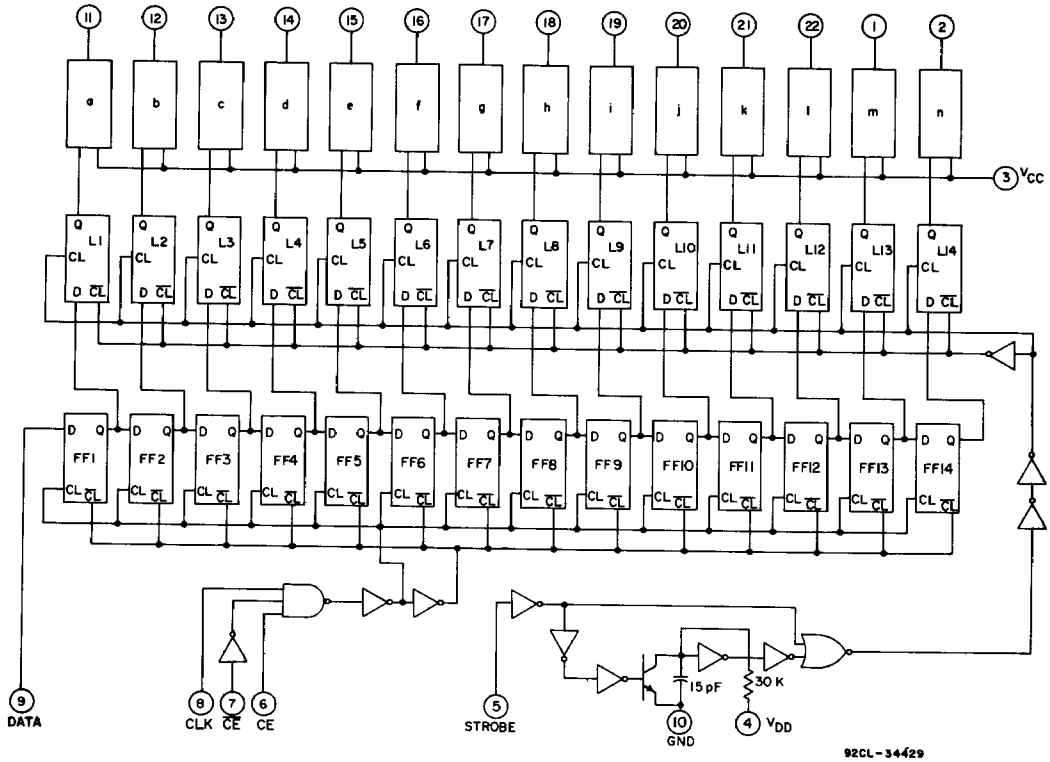
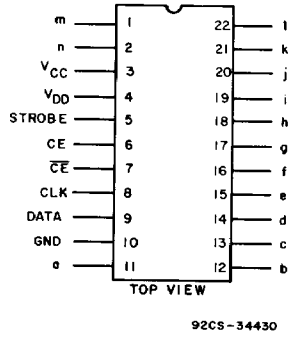


Fig. 2 - Segment-latch driver (CA3208E) logic diagram.

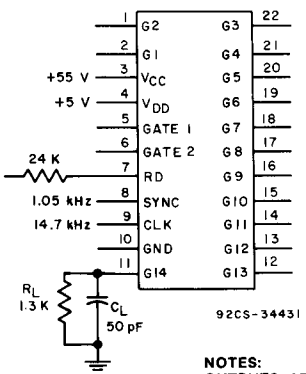


TERMINAL ASSIGNMENT
CA3208E

CA3207, CA3208

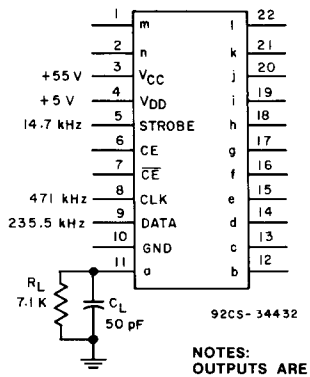
STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, See Fig. 3 and Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CA3207E		CA3208E		
			Min.	Max.	Min.	Max.	
V_{CC} Supply Current	I_{CC}	No outputs "ON"	—	10	—	—	mA
		Half outputs HIGH "ON"	—	—	—	65	
V_{DD} Supply Current	I_{DD}	All inputs HIGH	—	1	—	—	mA
		All inputs LOW	—	—	—	800	μA
		All inputs HIGH	—	—	—	1	
Input Current, Low-Level	I_{IL}	V_{IN}=0 V	—	1	—	1	μA
Input Current, High-Level	I_{IH}	V_{IN}=5 V	—	1	—	1	
Output Voltage, Low-Level	V_{OL}	R_L=1.3K	—	1	—	—	V
		R_L=7.1K	—	—	—	1	
Output Voltage, High-Level	V_{OH}	I_{OH}=40 mA	53	—	—	—	
		I_{OH}=7.5 mA	—	—	53	—	
Input Low Voltage	V_{IL}		—	1.5	—	1.5	V
Input High Voltage	V_{IH}		3.5	—	3.5	—	



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (1.3 K) AND C_L (50 pF) WHICH RESULTS IN A 40-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V and 5 V.

Fig. 3 - Sequencer-driver (CA3207E) test circuit.



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (7.1 K) AND C_L (50 pF) WHICH RESULTS IN A 7.5-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V AND 5 V.

Fig. 4 - Segment-latch driver (CA3208E) test circuit.

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, R_L=1.3K

CHARACTERISTIC		LIMITS CA3207E Min.	LIMITS CA3207E Max.	UNITS
Sequencer-Driver, See Fig. 5				
Sync Pulse Width	t_{SW}	2	—	μs
Time Delay Gate 1:				
Input-to-Output Inhibit	t_{GI}	—	1.5	μs
Input-to-Output Enable	t_{GE}	—	2.3	μs
Lead Time Sync to Gate	t_{SG}	0.5	—	μs
Lead Time Clock to Gate	t_{CG}	0.5	—	μs
Clock Frequency	f_{CL}	—	14	kHz

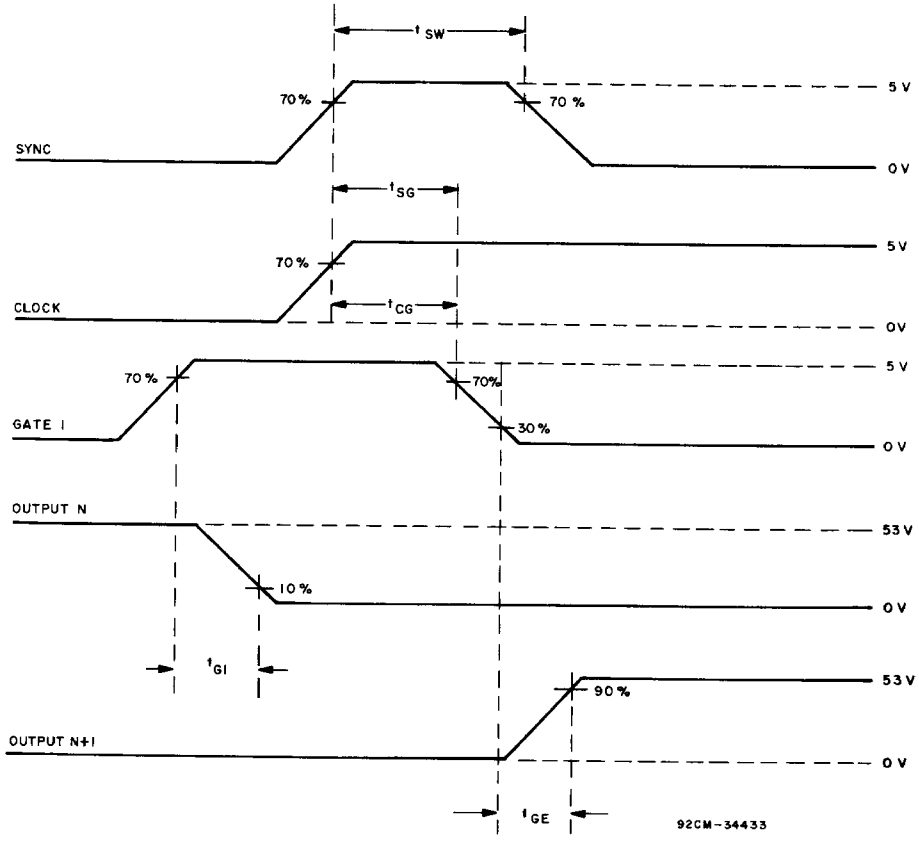

Fig. 5 - Sequencer-driver (CA3207E) timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L= 50 pF, R_L=7.1 K

CHARACTERISTIC		LIMITS CA3208E Min.	LIMITS CA3208E Max.	UNITS
Segment-Latch Driver, See Fig. 6				
Time Delay:				
Strobe to Output	t_{PLH}	0.4	1.8	
Strobe to Output	t_{PHL}	—	2.6	μs
CE or $\overline{CE}$ to Clock	t_{CE}	0.8	—	
Input Data Set-Up Time	t_{SU}	0.5	—	μs
Input Data Hold Time	t_H	0.5	—	
Clock Frequency	f_{CL}	—	448	kHz
Data Frequency	f_D	—	224	

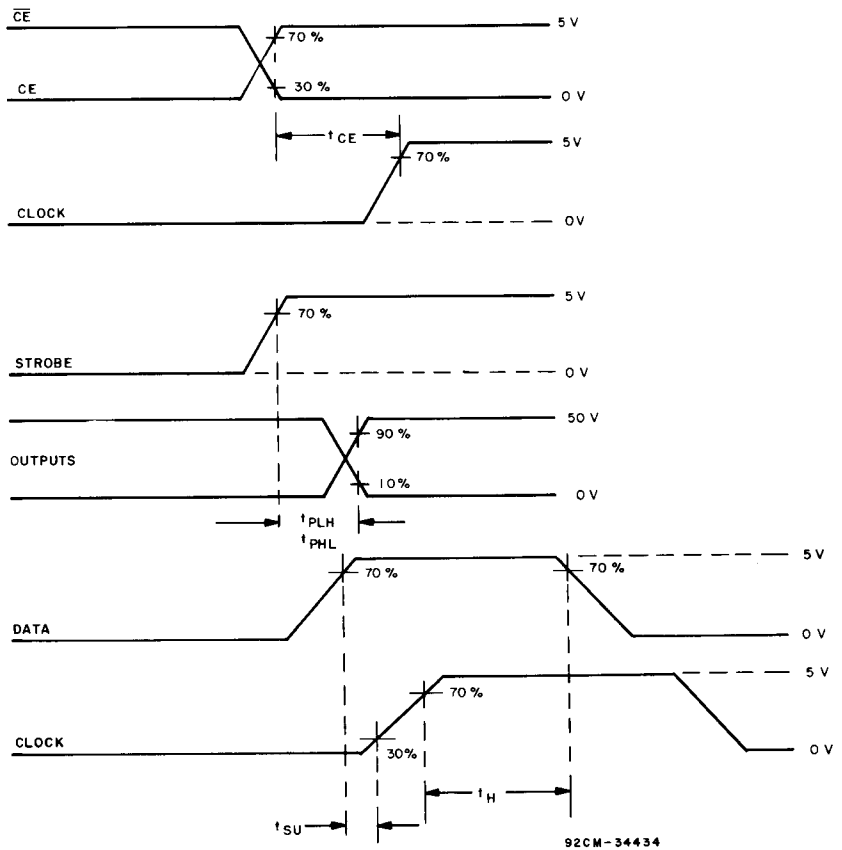

Fig. 6 - Segment-latch driver (CA3208E) timing waveforms.

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Circuit Descriptions

Sequencer-Driver (CA3207E)

The CA3207E circuit consists of a 7-stage Johnson counter, which is reset by the positive transition of the sync pulse and which is clocked on the positive transitions of the clock pulse. The outputs of the counter are decoded to turn on one output driver at a time in sequence, for the period of one clock pulse (normally 70 μs). The 14 output drivers are each capable of sourcing 40 mA of current and in a typical application will be connected to the grids of a vacuum fluorescent display, thereby performing a digit select function on a display of up to 14 characters. All outputs are set to zero by the application of a positive "1" level to either of the gate terminals, 5 and 6. The action of the 7-stage counter is unaffected by the presence of inhibit levels on the gate terminals. The gate terminals can be used for a controlled power down or for chopping where display dimmer is desired. The only difference between the two terminals is that gate 1, pin 5, has a delayed falling edge, which delays the release of the output drivers for a time determined by the value of the resistor connected between pin 7 and V_{DD}.

Segment-Latch Driver (CA3208E)

This circuit consists of a 14-bit shift register accepting serial data at pin 9 at a typical rate of 224 kHz and being clocked on the rising edge of the 448-kHz clock signal.

The leading edge of a 14-kHz strobe signal generates an internal strobe pulse through the one shot, which shifts the data, in parallel, from the shift register to the output latches, which in turn set the output drivers to the corresponding state. There are 14 output drivers, each capable of driving 7.5-mA at 55 volts, simultaneously. The drivers are normally connected to the anodes or segments of the vacuum fluorescent display. In a multi-character display, all corresponding segments in each character would be linked together. Activation of a particular character is made by the CA3207E Sequencer-Driver turning on the appropriate output and raising the grid of the display to a positive value.

Clock Enable (CE) and Clock Enable Not ($\overline{CE}$) pins are available for use in system applications. The first enables the chip with a logic level "1" and the second with a logic level"0".

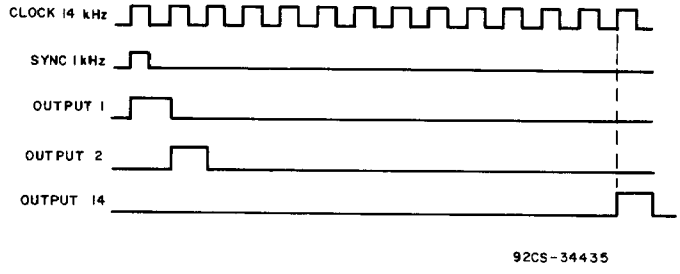
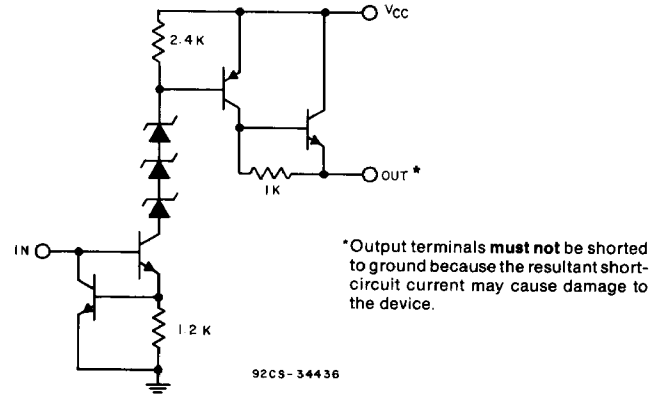


Fig. 7 - Sequencer driver (CA3207E) timing waveforms.



*Output terminals **must not** be shorted to ground because the resultant short-circuit current may cause damage to the device.

Fig. 8 - Sequencer driver (CA3207E) output circuit.

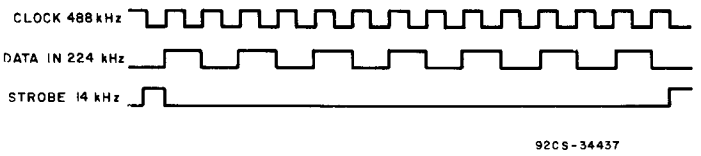
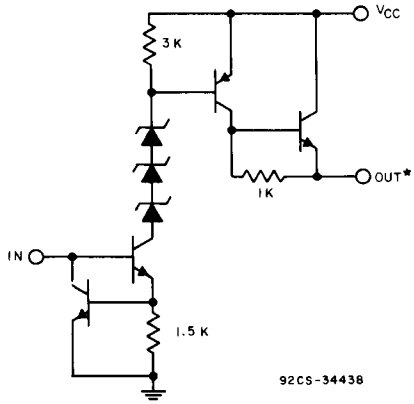


Fig. 9 - Segment-latch driver (CA3208E) timing waveforms.



*Output terminals **must not** be shorted to ground because the resultant short-circuit current may cause damage to the device.

Fig. 10 - Segment latch-driver (CA3208E) output circuit.

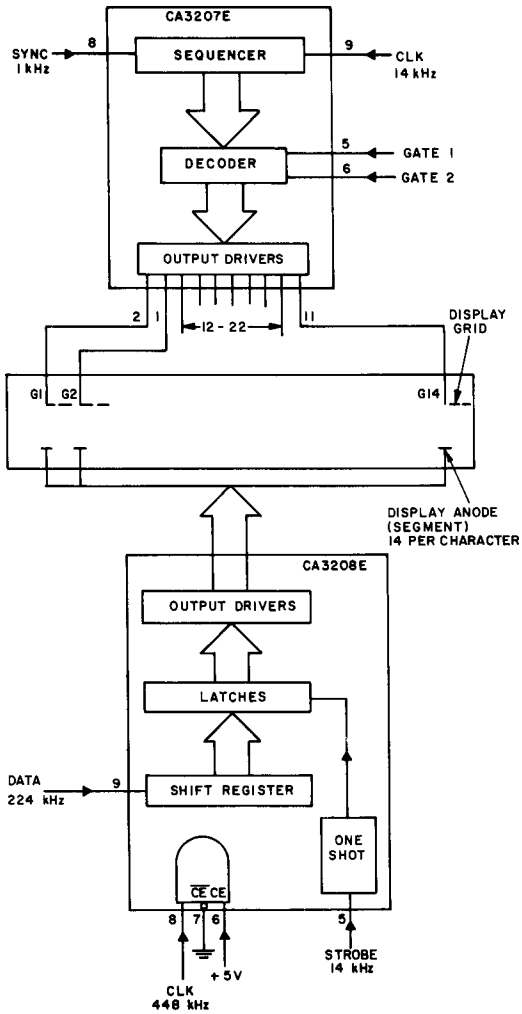


Fig. 11 - Typical systems application of the CA3207E and CA3208E display circuits.

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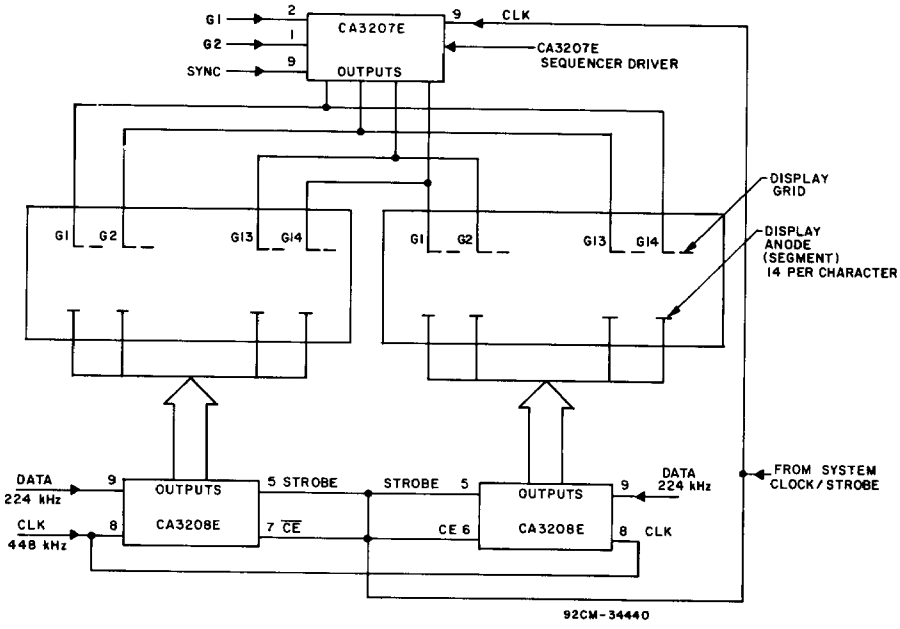
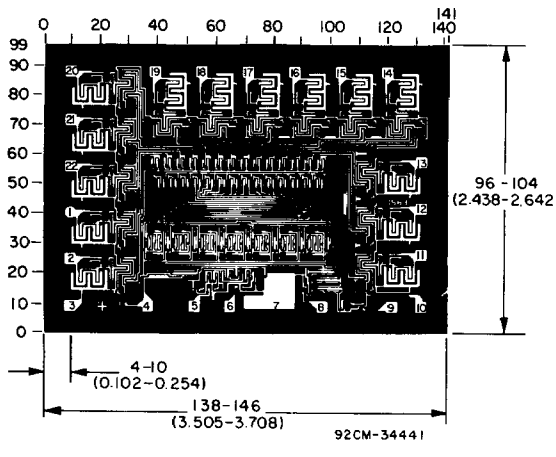
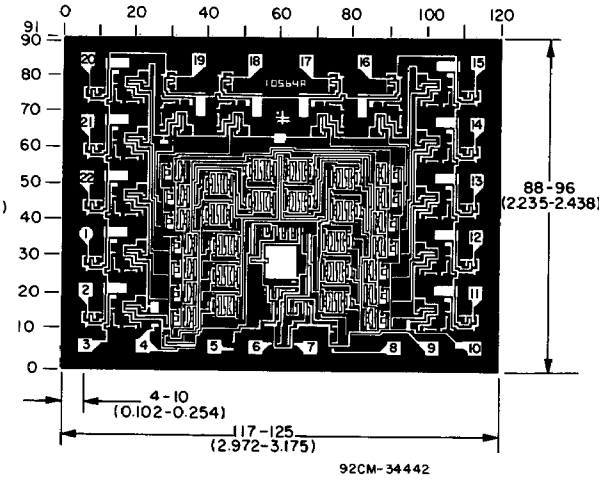


Fig. 12 - Typical systems application of the CA3207E and 2 CA3208E circuits for a total 28-character display.



Dimensions and pad layout for the CA3207H.



Dimensions and pad layout for the CA3208H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).