

# Low Duty LCD Segment Driver

**BU9795BKV**

**MAX 140 Segments (SEG35×COM4)**

## General Description

BU9795BKV is a 1/4 Duty General-purpose LCD driver that can be used for consumer / battery operated products. BU9795KV can drive up to 140 LCD Segments. It has integrated display RAM for reducing CPU load. Also, it is designed with low power consumption and no external component needed.

## Key Specifications

- Supply Voltage Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 140 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

## Features

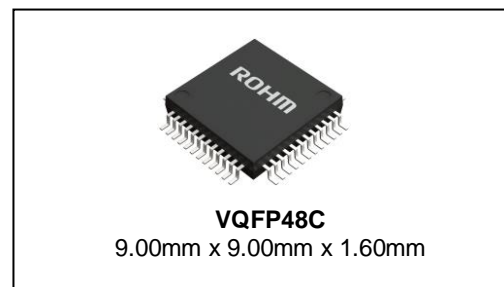
- Integrated RAM for Display Data (DDRAM) : 35 × 4bit (Max 140 Segments)
- LCD Drive Output : 4 Common output, Max 35 Segment output
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit
- No external Components
- Low Power Consumption Design

## Applications

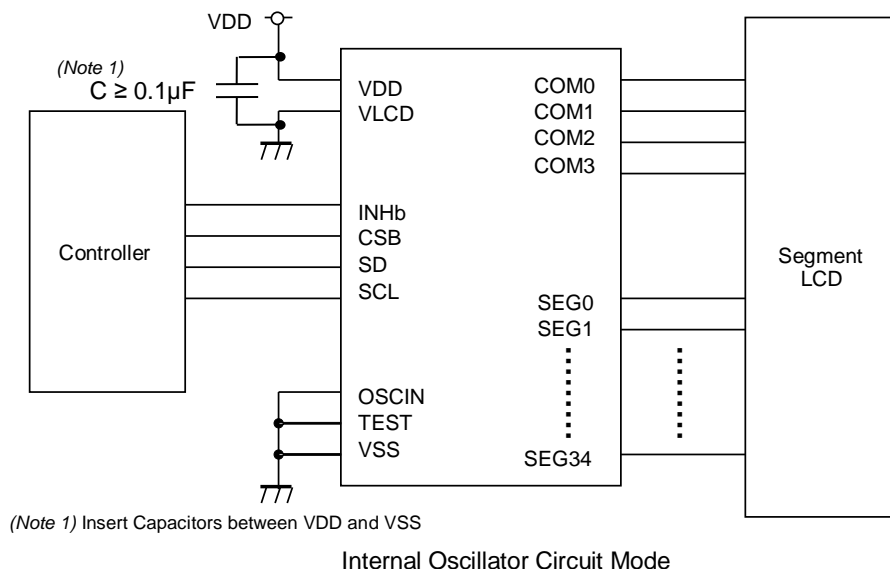
- Metering
  - Home Automation Goods
  - White Goods
  - Small Appliances
  - Healthcare Products
  - Battery Operated Products
- etc.

## Package

**W (Typ) x D (Typ) x H (Max)**



## Typical Application Circuit



**Figure 1. Typical Application Circuit**

Block Diagrams / Pin Configurations / Pin Description

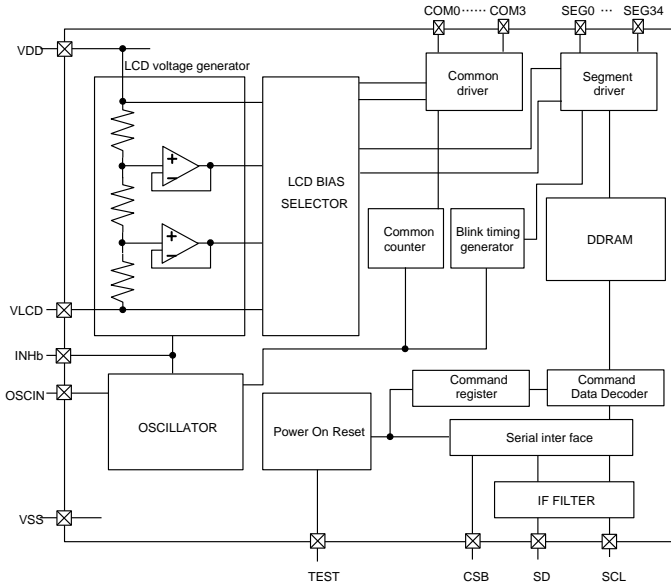


Figure 2. Block Diagram

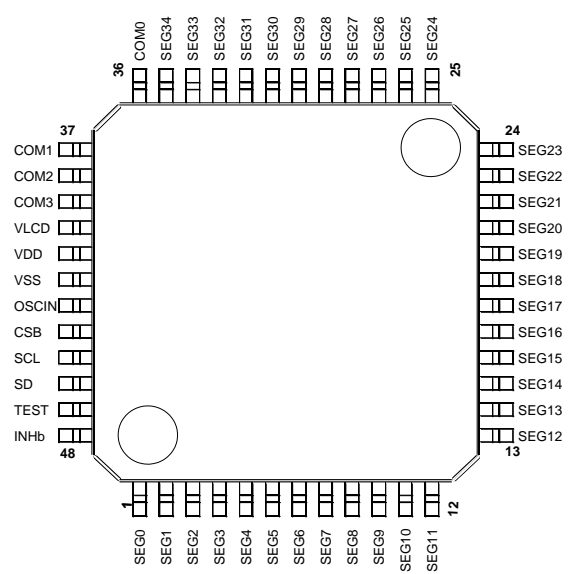


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Pin Name	Pin No.	I/O	Function	Handling when unused
INHb	48	I	Input pin for turn off display H : turn on display L : turn off display	VDD
TEST	47	I	POR enable setting VDD: POR disenable (Note) VSS: POR enable	VSS
OSCIN	43	I	Input pin for external clock External clock and Internal clock can be changed by command. Must be connected to VSS when using internal oscillation circuit.	VSS
SD	46	I	Serial data input	-
SCL	45	I	Serial data transfer clock	-
CSB	44	I	Chip select : "L" active	-
VSS	42	-	Ground	-
VDD	41	-	Power supply	-
VLCD	40	I	Power supply for LCD driving	-
SEG0 to 34	1 to 35	O	Segment output for LCD driving	OPEN
COM0 to 3	36 to 39	O	Common output for LCD driving	OPEN

(Note) This function is guaranteed by design, not tested in production process.  
Software Reset is necessary to initialize IC in case of TEST=VDD.

## Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remark
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power Supply
Power Supply Voltage2	VLCD	-0.5 to VDD	V	LCD Drive Voltage
Power Dissipation	Pd	0.60 <sup>(Note 1)</sup>	W	
Input Voltage Range	V <sub>IN</sub>	-0.5 to VDD+0.5	V	
Operating Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	

(Note 1) Derate by 6.0mW/°C when exceeding above Ta=25°C (when mounted in ROHM's standard board).

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

## Recommended Operating Conditions (Ta=-40°C to +85°C, VSS=0V)

Parameter	Symbol	Ratings			Unit	Remark
		Min	Typ	Max		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power Supply
Power Supply Voltage2	VLCD	0	-	VDD-2.4	V	LCD Drive Voltage, VDD-VLCD ≥ 2.4V

## Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
"H" Level Input Voltage	V <sub>IH</sub>	0.7VDD	-	VDD	V	SD, SCL, CSB, INHb, OSCIN
"L" Level Input Voltage	V <sub>IL</sub>	VSS	-	0.3VDD	V	SD, SCL, CSB, INHb, OSCIN
"H" Level Input Current	I <sub>IH</sub>	-	-	1	μA	SD, SCL, CSB, INHb, OSCIN <sup>(Note 2)</sup> , TEST
"L" Level Input Current	I <sub>IL</sub>	-1	-	-	μA	SD, SCL, CSB, INHb, OSCIN <sup>(Note 2)</sup> , TEST
LCD Driver ON-Resistance	SEG	R <sub>ON</sub>	-	3.5	-	kΩ Iload=±10μA
	COM	R <sub>ON</sub>	-	3.5	-	
VLCD Supply Voltage	VLCD	0	-	VDD -2.4	V	VDD-VLCD ≥ 2.4V
Standby Current	I <sub>st</sub>	-	-	5	μA	Display off, Oscillator off
Power Consumption 1	I <sub>DD1</sub>	-	12.5	30	μA	VDD=3.3V, VLCD=0V, Ta=25°C, Power save mode1, FR=70Hz, 1/3 bias, Frame inverse
Power Consumption 2	I <sub>DD2</sub>	-	20	40	μA	VDD=3.3V, VLCD=0V, Ta=25°C, Normal mode, FR=80Hz, 1/3 bias, Line inverse

(Note 2) For External clock mode only

**Electrical Characteristics – continued**

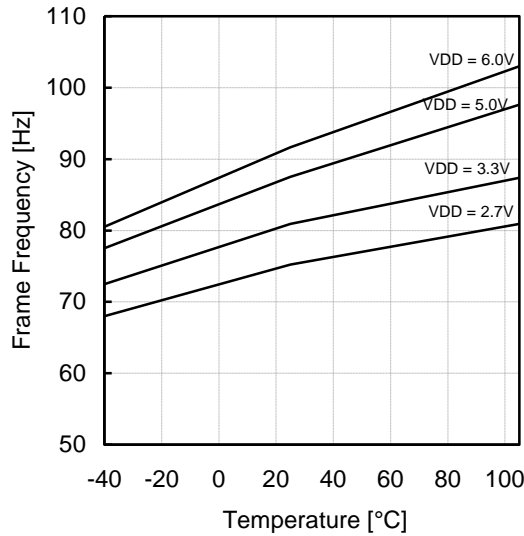
Oscillation Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency1	f <sub>CLK1</sub>	56	80	104	Hz	FR = 80Hz setting, VDD=2.5V to 5.5V, Ta=-40°C to +85°C
Frame Frequency2	f <sub>CLK2</sub>	70	80	90	Hz	FR = 80Hz setting, VDD=3.3V, Ta=25°C
Frame Frequency3	f <sub>CLK3</sub>	77.5	87.5	97.5	Hz	FR = 80Hz setting, VDD=5.0V, Ta=25°C
Frame Frequency4	f <sub>CLK4</sub>	67.5	87.5	108	Hz	FR = 80Hz setting, VDD=5.0V, Ta=-40°C to +85°C
External Clock Rise Time	t <sub>r</sub>	-	-	0.3	μs	External clock mode (OSCIN) <i>(Note)</i>
External Clock Fall Time	t <sub>f</sub>	-	-	0.3	μs	
External Frequency	f <sub>EXCLK</sub>	15	-	300	kHz	
External Clock Duty	t <sub>DTY</sub>	30	50	70	%	

*(Note)* <Frame frequency calculation at External clock mode>

- DISCTL 320Hz setting: Frame frequency [Hz] = External clock [Hz] / 128
- DISCTL 284Hz setting: Frame frequency [Hz] = External clock [Hz] / 144
- DISCTL 213Hz setting: Frame frequency [Hz] = External clock [Hz] / 192
- DISCTL 160Hz setting: Frame frequency [Hz] = External clock [Hz] / 256
- DISCTL 80Hz setting: Frame frequency [Hz] = External clock [Hz] / 512
- DISCTL 71Hz setting: Frame frequency [Hz] = External clock [Hz] / 576
- DISCTL 64Hz setting: Frame frequency [Hz] = External clock [Hz] / 648
- DISCTL 53Hz setting: Frame frequency [Hz] = External clock [Hz] / 768

**【Reference Data】**



**Figure 4. Frame Frequency Typical Temperature Characteristics**

Electrical Characteristics – continued

MPU Interface Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	$t_r$	-	-	80	ns	
Input Fall Time	$t_f$	-	-	80	ns	
SCL Cycle Time	$t_{SCYC}$	400	-	-	ns	
“H” SCL Pulse Width	$t_{SHW}$	100	-	-	ns	
“L” SCL Pulse Width	$t_{SLW}$	100	-	-	ns	
SD Setup Time	$t_{SDS}$	20	-	-	ns	
SD Hold Time	$t_{SDH}$	50	-	-	ns	
CSB Setup Time	$t_{CSS}$	50	-	-	ns	
CSB Hold Time	$t_{CSH}$	50	-	-	ns	
“H” CSB Pulse Width	$t_{CHW}$	50	-	-	ns	

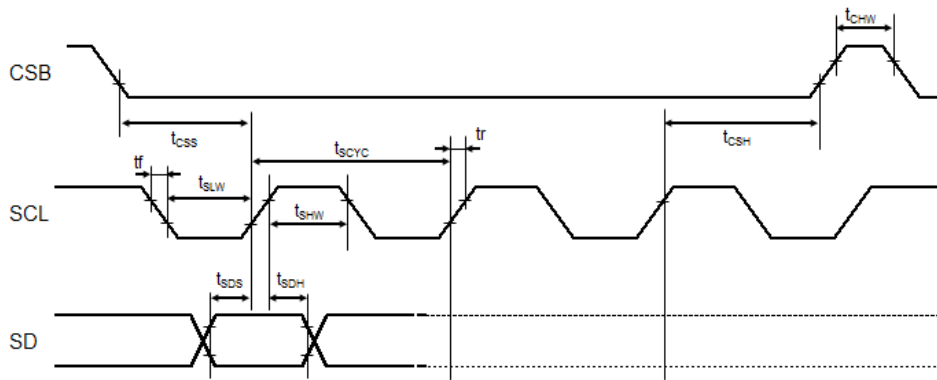


Figure 5. Interface Timing

I/O Equivalent Circuit

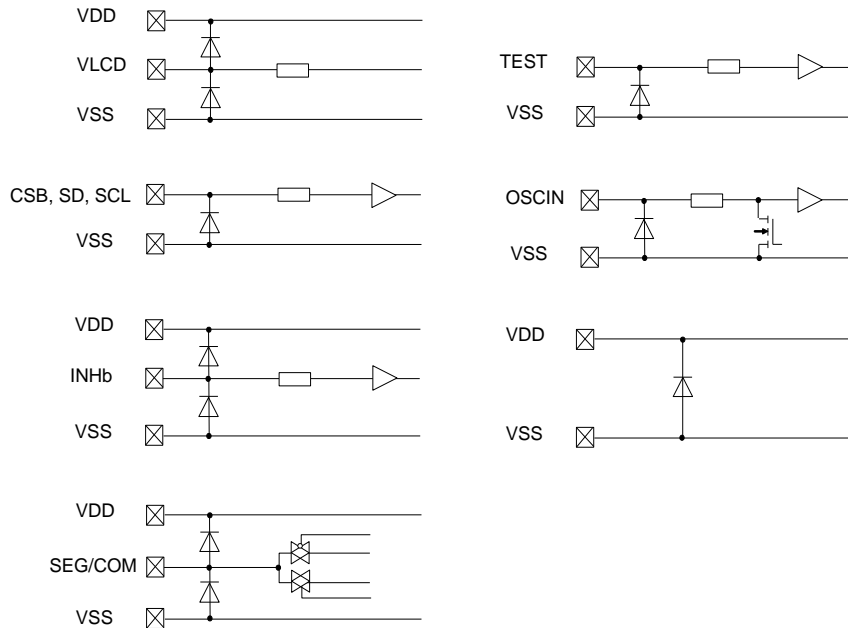
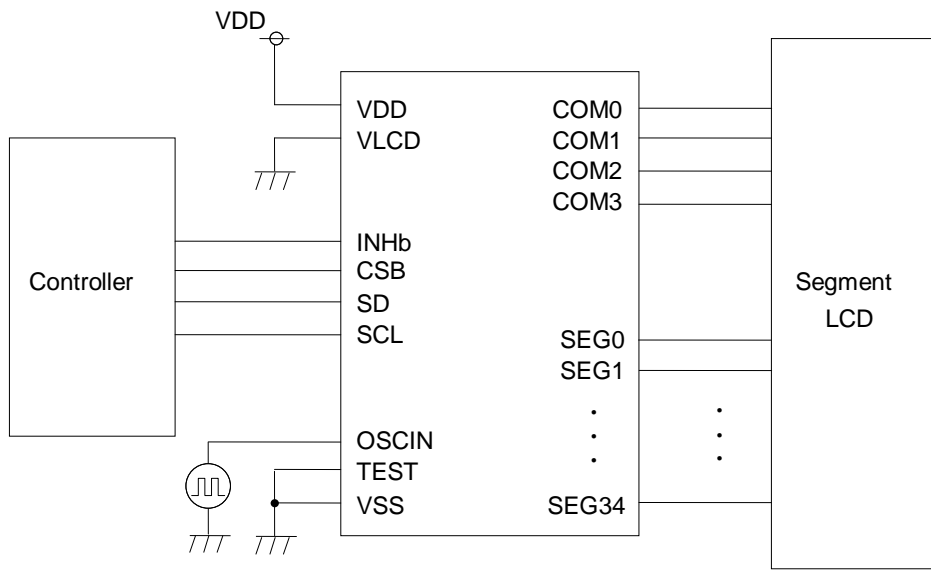
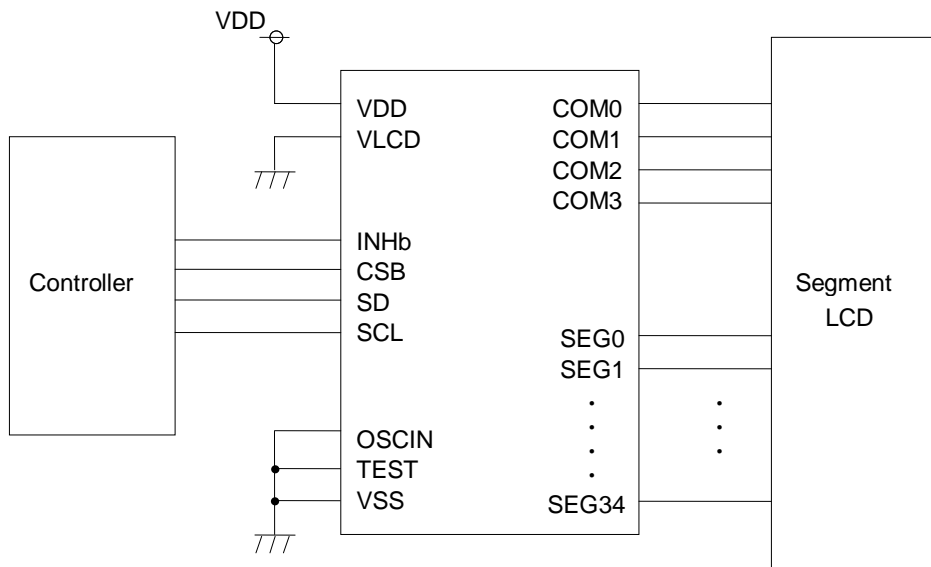


Figure 6. I/O Equivalent Circuit

Application Example



External clock mode



Internal Clock Mode

Figure 7. Example of Application Circuit

**Function Descriptions**

1. Command and Data Transfer Method

1.1 3-SPI (3wire Serial Interface)

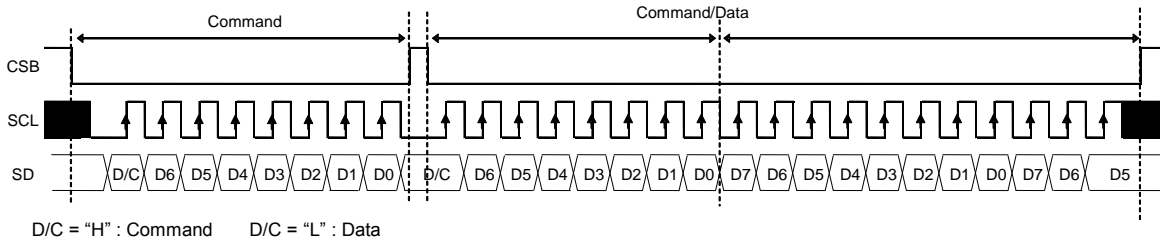
BU9795BKV is controlled by 3-wire signal (CSB, SCL, and SD).

First, Interface counter is initialized with CSB="H", and CSB="L" makes SD and SCL input enable.

The protocol of 3-SPI transfer is as follows.

Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by D6 to D0 during CSB = "L".

(Internal data is latched at the rising edge of SCL, it is converted to 8bits parallel data at the falling edge of 8th CLK.)



**Figure 8. 3-SPI Command/Data Transfer Format**

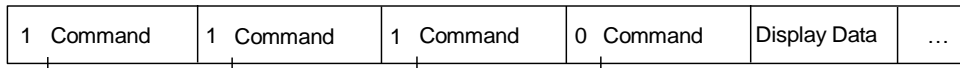
1.2 Command Transfer Method

After CSB="H"→"L", 1st byte is always a command input.

MSB of the command input data will be judged that the next byte data, it is a command or Display Data (This bit is called "command or data judgment bit").

When set "command or data judge bit"="1", next byte will be (continuously) command.

When set "command or data judge bit"="0", next byte data is Display Data.



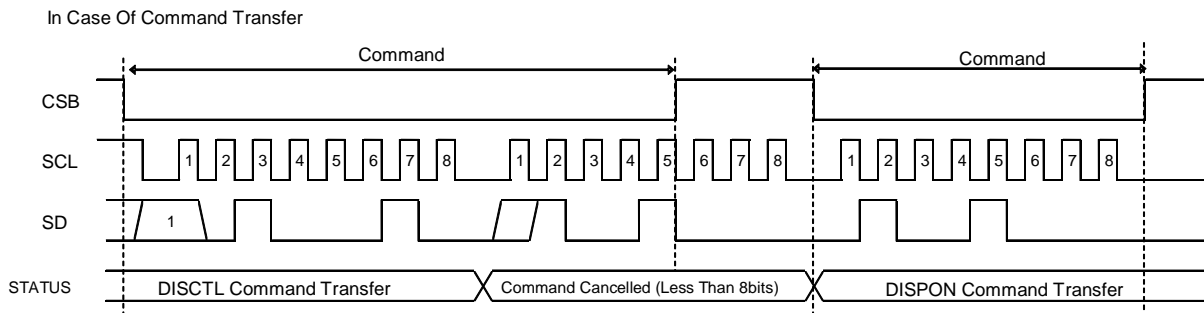
Once it becomes Display Data transfer condition, it will not be back to command input condition even if D/C=1.

So if you want to send command data again, set CSB="L"→"H".

(CSB "L"→"H" will cancel data transfer condition.)

Command transfer is done by 8bits unit, so if CSB="L"→"H" with less than 8bits data transfer, command will be cancelled.

It will be able to transfer command with CSB="L" again.



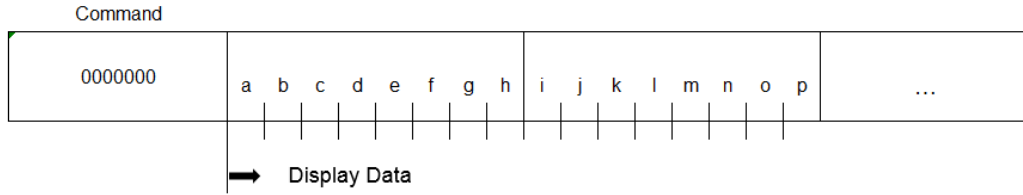
**Figure 9. Command Transfer Format**

1. Command and Data Transfer Method – continued

1.3 Write Display Data and transfer method

BU9795BKV has Display Data RAM (DDRAM) of 35×4=140bit.

The relationship between data input and display data, DDRAM data and address are as follows.



8bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.

(When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function. (Refer to [ADSET command](#) for the Address set order.)

		DDRAM address															
		00h	01h	02h	03h	04h	05h	06h	07h	...	1Eh	1Fh	20h	21h	22h		
BIT	0	a	e	i	m	q	u									COM0	
	1	b	f	j	n	r	v									COM1	
	2	c	g	k	o	s	x									COM2	
	3	d	h	l	p	t	y									COM3	
		SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	...	SEG 30	SEG 31	SEG 32	SEG 33	SEG 34		

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer. (Command transfer is done every 8bits)

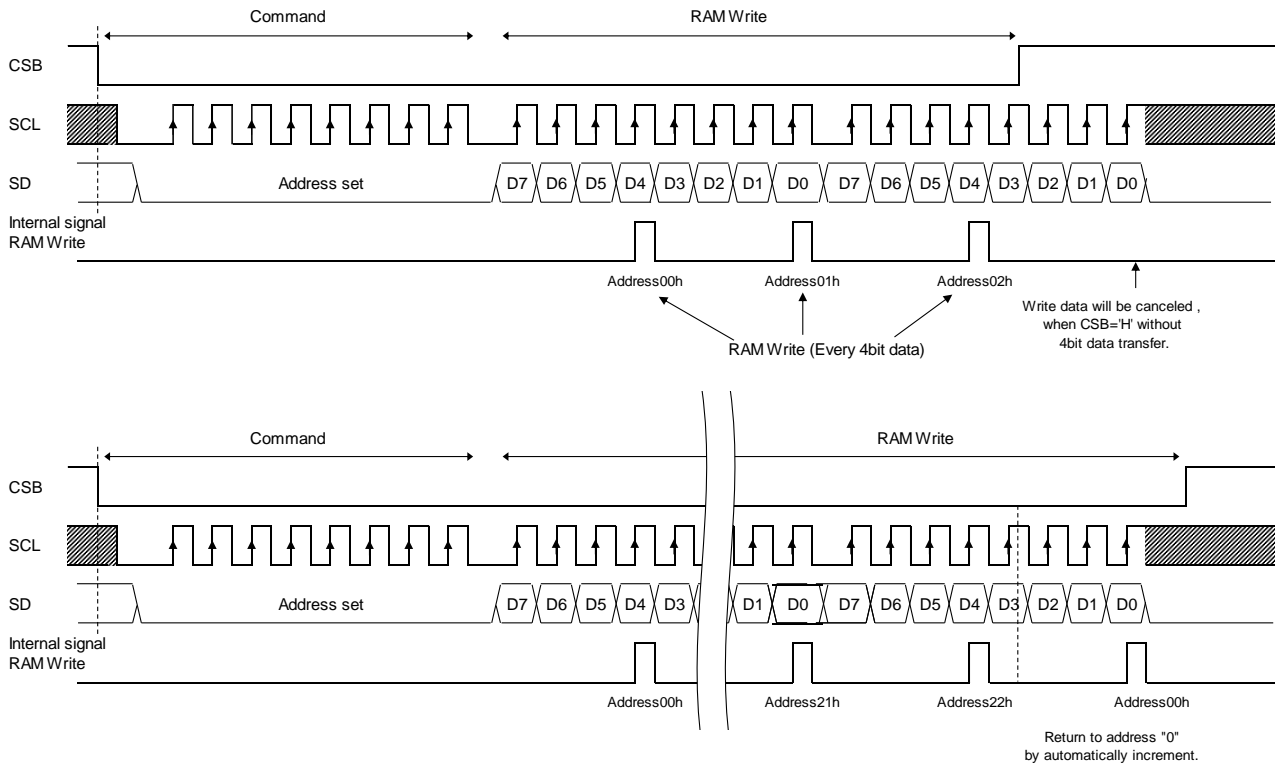


Figure 10. Data Transfer Format



**Function Descriptions – continued**

**2. OSCILLATOR**

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

When you use external clock, execute ICSET command and connect OSCIN to external clock.

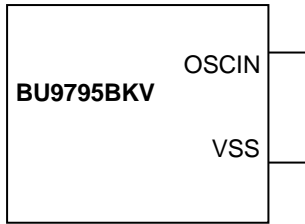


Figure 11. Internal Oscillator Circuit Mode

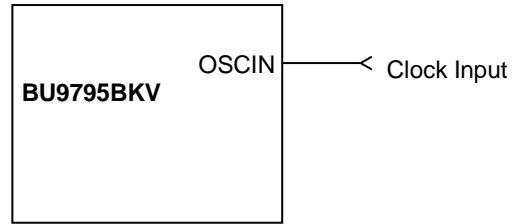


Figure 12. External clock mode

**3. LCD Driver Bias Circuit**

This LSI generates LCD driving voltage with on-chip Buffer AMP.

And it can drive LCD at low power consumption.

1/3 and 1/2Bias can be set in MODESET command.

Line and frame inversion can be set in DISCTL command.

Refer to "[LCD Driving Waveform](#)" about each LCD driving waveform.

**4. Blink Timing Generator**

BU9795BKV is equipped with Blinking function.

Blink mode is asserted by BLKCTL command.

The Blink frequency varies depending on  $f_{CLK}$  characteristics at Internal clock mode.

Refer to [Oscillation Characteristics](#) for  $f_{CLK}$ .

**5. Reset (Initial) Condition**

Initial condition after executing Software Reset is as follows.

(1) Display is OFF.

(2) DDRAM address is initialized (DDRAM Data is not initialized).

Refer to [Command Description](#) about initialize value of register.

**Command / Function List**

Table of Functions Description

No.	Command	Function
1	Mode Set (MODESET)	Set LCD Drive Mode
2	Address Set (ADSET)	Set LCD Display Mode 1
3	Display Control (DISCTL)	Set LCD Display Mode 2
4	Set IC Operation (ICSET)	Set IC Operation
5	Blink Control (BLKCTL)	Set Blink Mode
6	All Pixel Control (APCTL)	Set All Pixels ON/OFF Display

Detailed Command Description

D7 (MSB) is bit for command or data judgment.  
 Refer to [Command and data transfer method](#).

C : 0 : Next byte is RAM Write data.  
 1 : Next byte is command.

1.Mode Set (MODE SET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(\* : Don't care)

Set Display on and off

Setting	P3	Reset initial condition
Display off (DISPOFF)	0	○
Display on (DISPON)	1	-

Display off : Regardless of DDRAM data, all Segment and Common output will be stopped after 1 frame of data write. Display off mode will be finished by Display on.

Display on : Segment and Common output will be active and start to read the Display Data from DDRAM.

(Note) When Display on/off is controlled by INHb terminal, it is not synchronized with display frame period.

Set bias level

Setting	P2	Reset initial condition
1/3 Bias	0	○
1/2 Bias	1	-

Refer to [LCD driving waveform](#) (Example of SEG and COM output waveform by Bias level setting.).

2.Address Set (ADSET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

Address data is specified in P[4 : 0] and P2 (ICSET command) as follows.

	MSB			LSB
Internal register	Address [5]	Address [4]	...	Address [0]
Bit of each command	ICSET [P2]	ADSET [P4]	...	ADSET [P0]

The address is 00h in reset condition. The valid address is 00h to 22h.

Another address is invalid, (otherwise address will be set to 00h.)

The ICSET command is only to define the register setting ("0" or "1") of MSB of the address and does not set the address. Address counter will be set only when ADSET command is executed. When ICSET[P2] is set, the previous state is maintained until ICSET command is executed again or when Software Reset is executed.

Detailed Command Description – continued

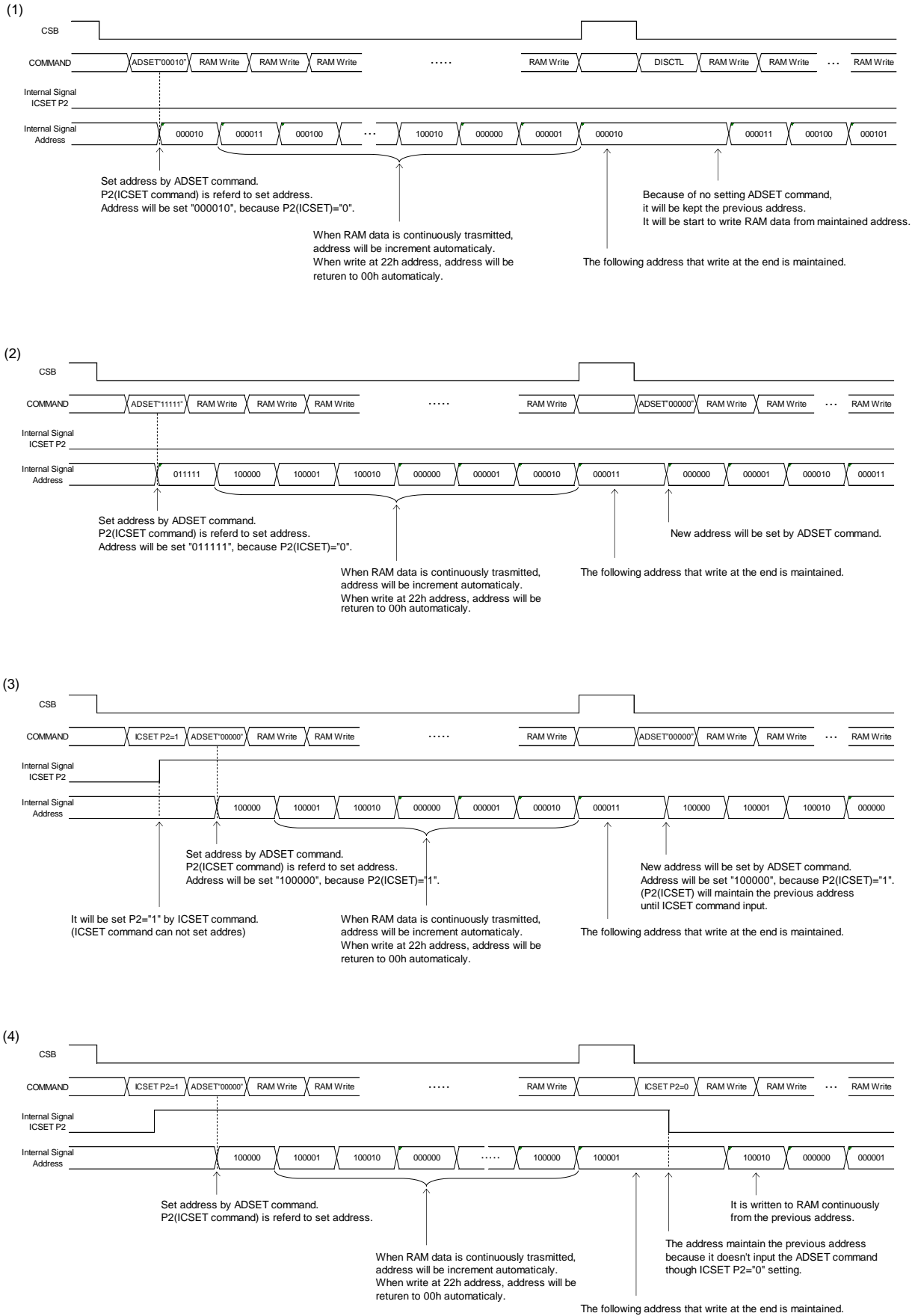


Figure 13. Address Set Sequence

Detailed Command Description – continued

3. Display Control (DISCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame Frequency

Setting <sup>(Note 1)</sup>	P4	P3	FRSEL <sup>(Note 2)</sup>	Reset initial condition
80Hz	0	0	0	○
71Hz	0	1	0	-
64Hz	1	0	0	-
53Hz	1	1	0	-
160Hz	0	0	1	-
213Hz	1	1	1	-
284Hz	0	1	1	-
320Hz	1	0	1	-

(Note 1) The frame frequency varies according to the characteristics of f<sub>CLK</sub> when internal oscillation circuit is used.  
 (Refer to [Oscillation Characteristics](#) for f<sub>CLK</sub> properties).

(Note 2) Refer to [BLKCTL](#) for FRSEL

Set LCD Drive Waveform

Setting	P2	Reset initial condition
Line Inversion	0	○
Frame Inversion	1	-

Power consumption is reduced in the following order:

Line inversion > Frame inversion

Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.

Regarding driving waveform, refer to [LCD Driving Waveform](#).

Set Power Save Mode (low current consumption mode)

Setting	P1	P0	Reset initial condition
Power Save Mode 1	0	0	-
Power Save Mode 2	0	1	-
Normal Mode	1	0	○
High Power Mode	1	1	-

Power consumption is increased in the following order:

Power save mode 1 < Power save mode 2 < Normal mode < High power mode

Use VDD- VLCD ≥ 3.0V in High power mode condition.

(Reference Current Consumption data)

Setting	Reset initial condition
Power Save Mode 1	×0.5
Power Save Mode 2	×0.67
Normal Mode	×1.0
High Power Mode	×1.8

The data above is for reference only. Actual consumption depends on Panel load.

Detailed Command Description – continued

4. Set IC Operation (ICSET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2 : Set MSB data of DDRAM address.  
 Execute ADSET command for it to take effect on an address.  
 Refer to “ADSET” command for details.

Setting	P2	Reset initial condition
Address MSB”0”	0	○
Address MSB”1”	1	-

Set Software Reset Condition

Setting	P1
No Operation	0
Software Reset	1

When “Software Reset” is executed, BU9795BKV will be reset to initial condition.  
 If software reset is executed, the value of P2 and P0 will be ignored and they will be reset to initial condition.  
 (Refer to “Reset initial condition”)

Switch between Internal oscillator operating mode and external clock mode.

Setting	P0	Reset initial condition
Internal oscillator operating mode	0	○
External Clock Input mode	1	-

Internal oscillator operating mode: OSCIN must be connected to VSS level.  
 External Clock mode: Input external clock from OSCIN terminal.

< Frame frequency Calculation at External clock mode >

- DISCTL 320Hz select : Frame frequency [Hz] = External clock[Hz] / 128
- DISCTL 284Hz select : Frame frequency [Hz] = External clock[Hz] / 144
- DISCTL 213Hz select : Frame frequency [Hz] = External clock[Hz] / 192
- DISCTL 160Hz select : Frame frequency [Hz] = External clock[Hz] / 256
- DISCTL 80Hz select : Frame frequency [Hz] = External clock[Hz] / 512
- DISCTL 71Hz select : Frame frequency [Hz] = External clock[Hz] / 576
- DISCTL 64Hz select : Frame frequency [Hz] = External clock[Hz] / 648
- DISCTL 53Hz select : Frame frequency [Hz] = External clock[Hz] / 768

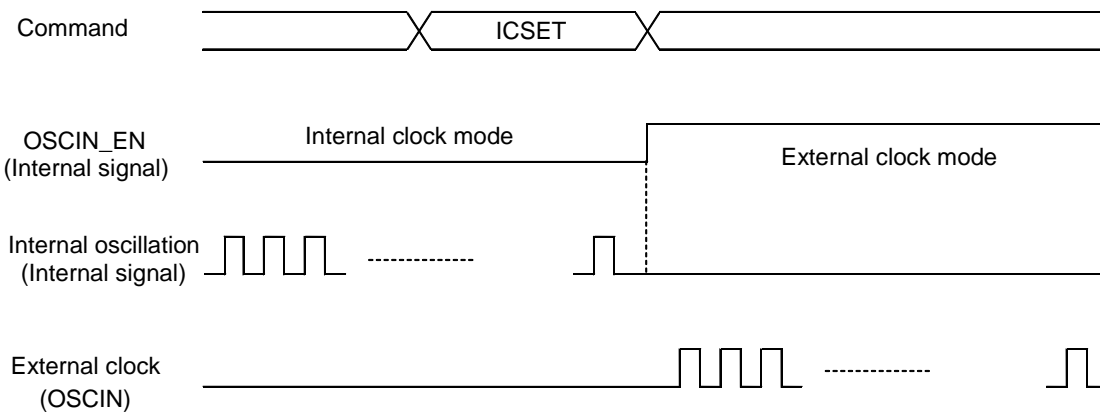


Figure 14. OSC MODE Switching Timing

**Detailed Command Description – continued**

## 5. Blink Control (BLKCTL)

MSB

LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	P2	P1	P0

## Set Blink Condition

Setting	P1	P0	Reset initial condition
OFF	0	0	○
0.5 (Hz)	0	1	-
1 (Hz)	1	0	-
2 (Hz)	1	1	-

The Blink frequency varies depending on  $f_{CLK}$  characteristics at Internal oscillator operating mode. Refer to [Oscillation Characteristics](#) for  $f_{CLK}$ .

## Set Frame Frequency Setting(FRSEL)

Setting	P2	Reset initial condition
Normal	0	○
200Hz mode	1	-

## 6. All Pixel Control (APCTL)

MSB

LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

## All Display Set ON/OFF

Setting	P1	Reset initial condition
Normal	0	○
All Pixel on	1	-

Setting	P0	Reset initial condition
Normal	0	○
All Pixel off	1	-

All pixels on: All pixels are on regardless of DDRAM data.  
All pixels off: All pixels are off regardless of DDRAM data.

This command is valid in Display on status. The data of DDRAM is not changed by this command. If set both P1 and P0 = "1", APOFF will be selected.

LCD Driving Waveform

(1/3bias)

Line Inversion

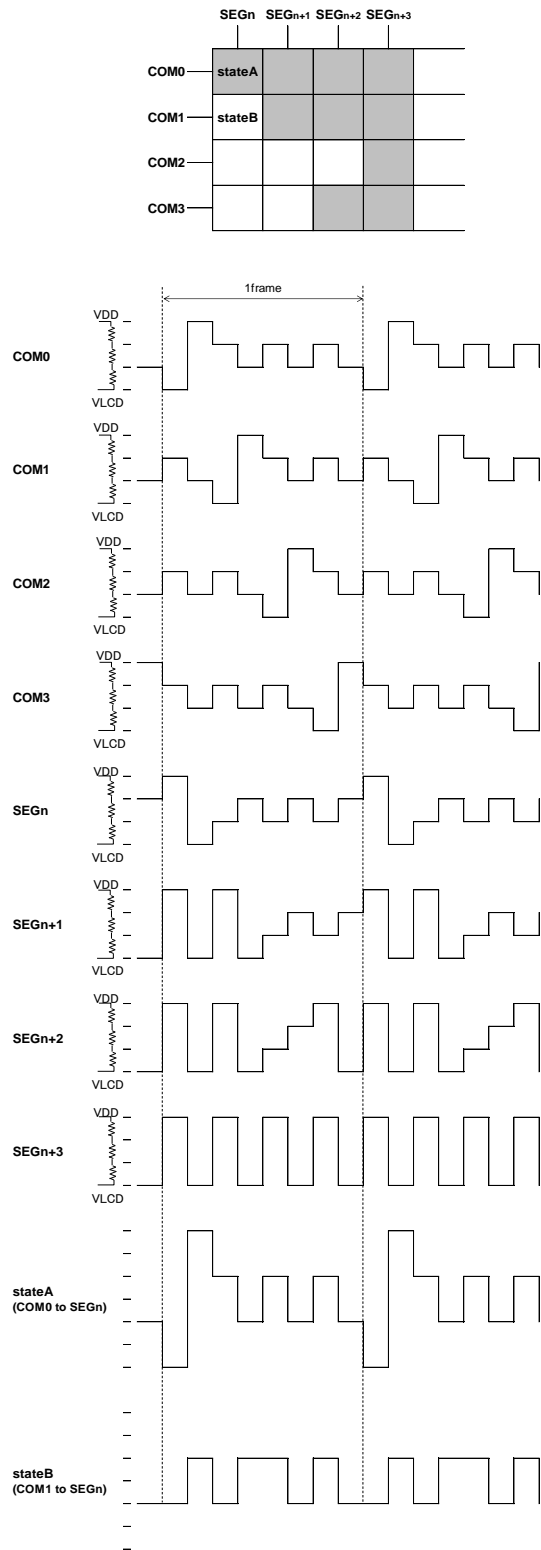


Figure 15. Line Inversion Waveform (1/3bias)

Frame Inversion

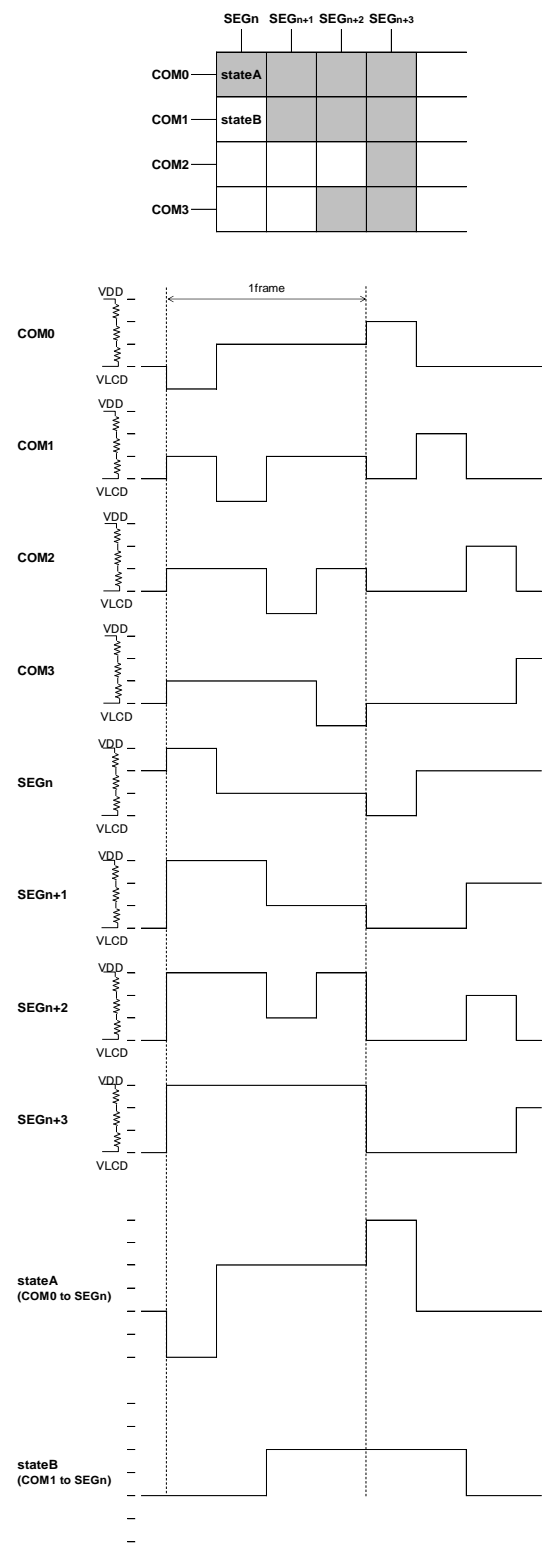


Figure 16. Frame Inversion Waveform (1/3bias)

LCD Driving Waveform – continued

(1/2bias)

Line Inversion

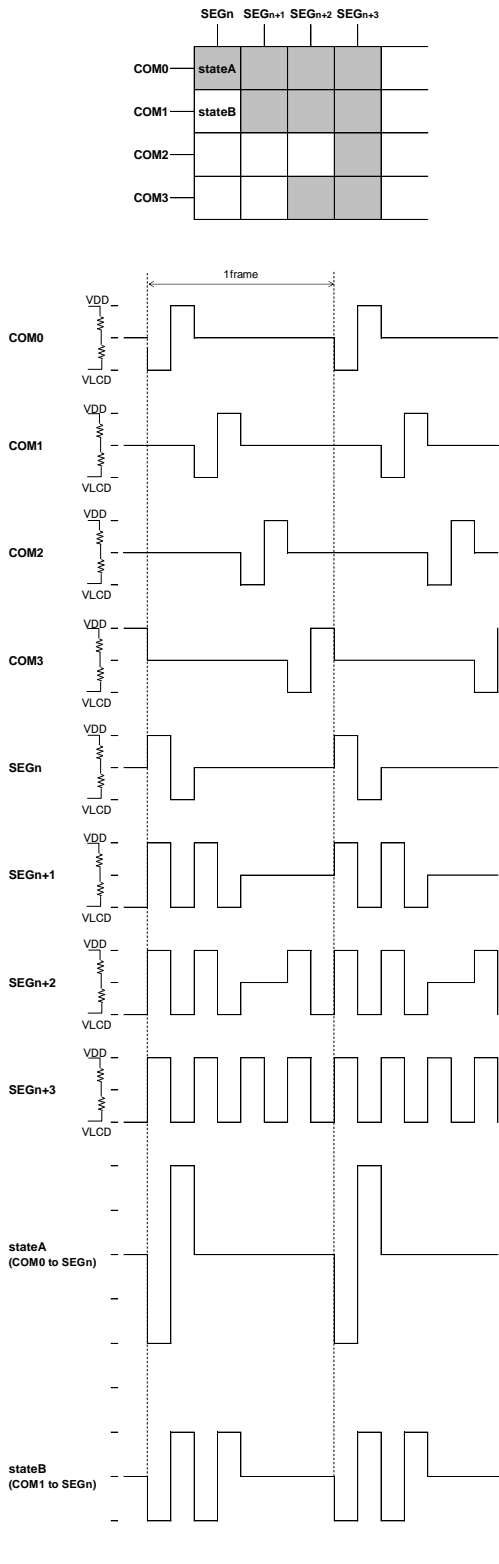


Figure 17. Line Inversion Waveform (1/2bias)

Frame Inversion

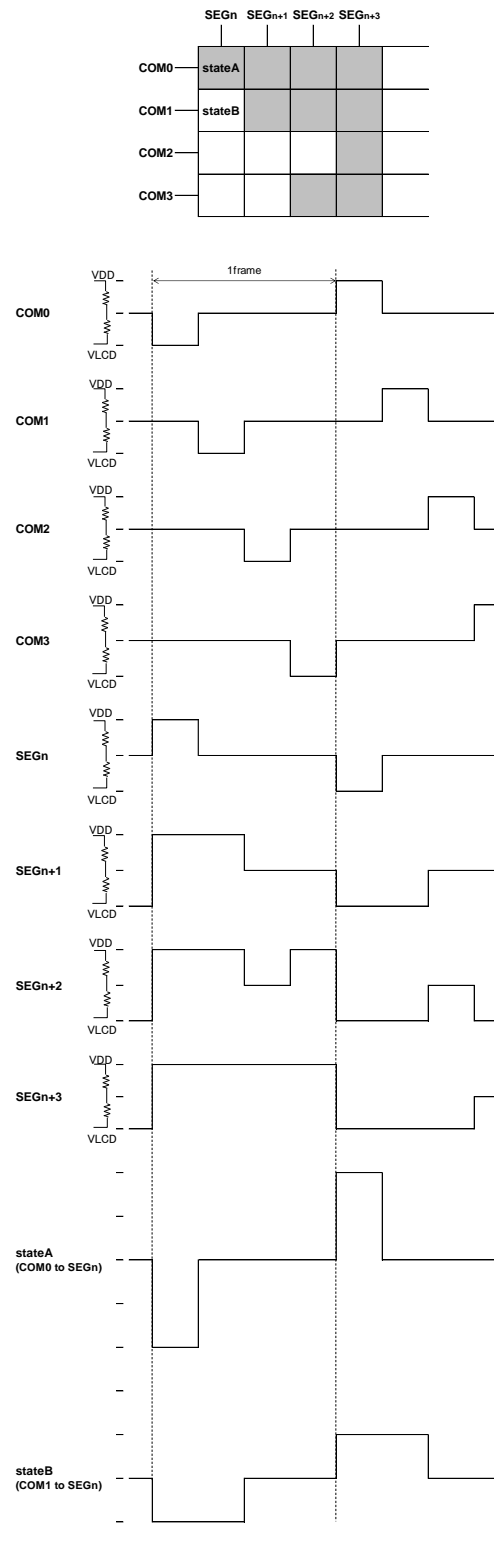


Figure 18. Frame Inversion Waveform (1/2bias)



Example of Display Data

If COM and SEG line pattern is shown as in Figure 19 and Figure 20, and DDRAM data is shown as in Table 2, display pattern will be shown as in Figure 21.

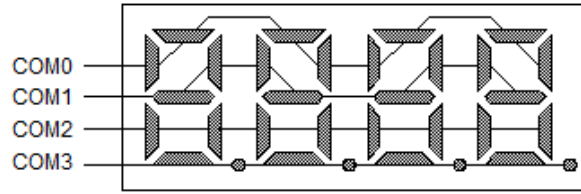


Figure 19. Example COM Line Pattern

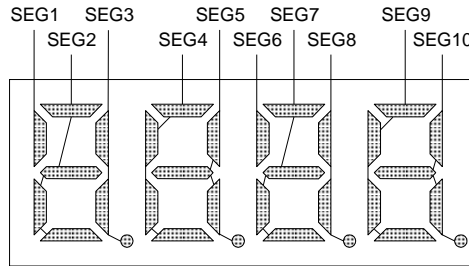


Figure 20. Example SEG Line Pattern



Figure 21. Example Display Pattern

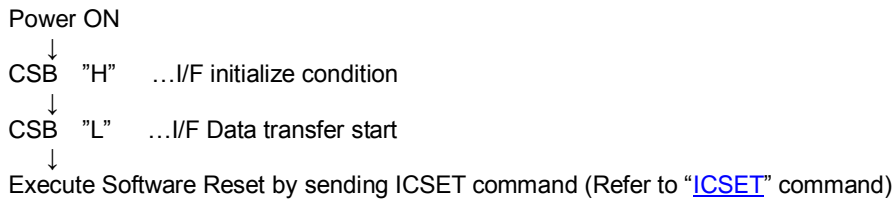
Table 2. DDRAM Data Map

	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	
	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	
	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	
	0	1	2	3	4	5	6	7	8	9	0A	0B	0C	0D	0E	0F	10	11	12	13
COM0	D0	0	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
COM2	D2	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Address      00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h

**Initialize Sequence**

Follow sequence below after Power ON to set BU9795BKV to initial condition.



\* Each register value, DDRAM address and DDRAM data are random after Power ON until initialize sequence is executed.

**Start Sequence**

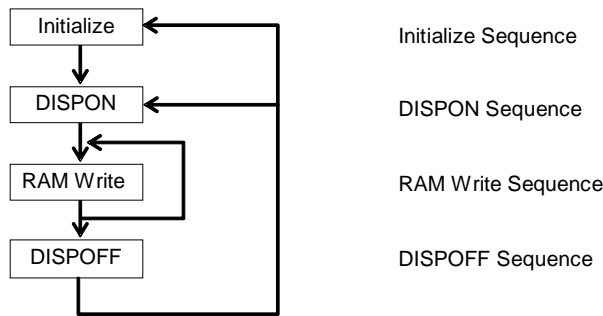
Start Sequence Example 1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power ON									VDD=0V to 5V (Tr=0.1ms)
	↓									
2	Wait 100µs									Initialize IC
	↓									
3	CSB "H"									Initialize I/F data
	↓									
4	CSB "L"									I/F Data transfer start
	↓									
5	ICSET	1	1	1	0	1	*	1	0	Software Reset
	↓									
6	BLKCTL	1	1	1	1	0	*	0	1	
	↓									
7	DISCTL	1	0	1	0	0	1	1	0	
	↓									
8	ICSET	1	1	1	0	1	0	0	0	RAM Address MSB set
	↓									
9	ADSET	0	0	0	0	0	0	0	0	RAM Address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	Address 02h to 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h to 00h
	↓									
11	CSB "H"									I/F Data transfer stop
	↓									
12	CSB "L"									I/F Data transfer start
	↓									
13	MODESET	1	1	0	*	1	0	*	*	Display on
	↓									
14	CSB "H"									I/F Data transfer stop

(\*: don't care)

Start Sequence – continued

Start Sequence Example 2



BU9795BKV is initialized with Initialize Sequence, starts to display with “DISPON Sequence”, updates Display Data with “RAM Write Sequence” and stops the display with “DISPOFF sequence”. If you want to resume to display, BU9795BKV will resume display with DISPON Sequence.

Initialize Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Power ON									IC initialized
Wait 100us									I/F initialized
CSB "H"									
CSB "L"									
ICSET	1	1	1	0	1	0	1	0	Software Reset
MODESET	1	1	0	0	0	0	0	0	Display off
ADSET	0	0	0	0	0	0	0	0	RAM Address set
Display Data	*	*	*	*	*	*	*	*	Display Data
...									
CSB "H"									

DISPON Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB "L"									
DISCTL	1	0	1	1	1	1	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	0	0	0	Display on
CSB "H"									

RAM Write Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB "L"									
DISCTL	1	0	1	1	1	1	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	0	0	0	Display on
ADSET	0	0	0	0	0	0	0	0	RAM Address set
Display Data	*	*	*	*	*	*	*	*	Display Data
...									
CSB "H"									

DISPOFF Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
MODESET	1	1	0	0	0	0	0	0	Display off
CSB 'H'									

Abnormal operation may occur in BU9795BKV due to the effect of noise or other external factor. To avoid this phenomenon, it is highly recommended to input command according to sequence when the operating of initialize, Display On/Off and the refresh of RAM Data.

**Cautions of “Power ON Condition”**

Power supply sequence

Keep Power ON/OFF sequence as below waveform.

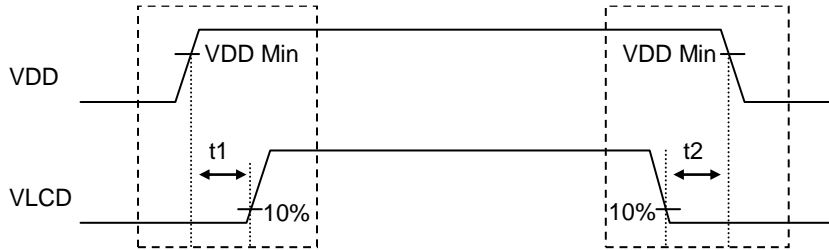
To prevent incorrect display, malfunction and abnormal current,

VDD must be turned on before VLCD in power up sequence.

VDD must be turned off after VLCD in power down sequence.

Satisfy  $VDD - 2.4V \geq VLCD$ ,  $t1 > 0ns$  and  $t2 > 0ns$ .

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.



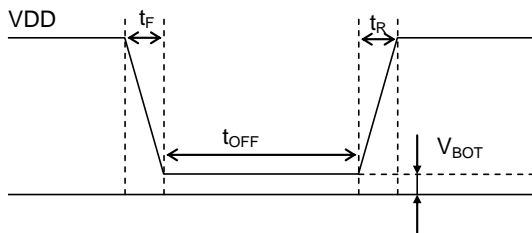
**Figure 22. Power Supply Sequence**

BU9795BKV has “POR” (Power ON Reset) circuit and Software Reset function.

Keep the following recommended Power ON conditions in order to power up properly.

(1) Set power up conditions to meet the recommended  $t_R$ ,  $t_F$ ,  $t_{OFF}$ , and  $V_{BOT}$  specification below in order to ensure POR operation.

Set pin TEST=“L” to enable POR circuit.



Recommended condition of  $t_R$ ,  $t_F$ ,  $t_{OFF}$ ,  $V_{BOT}$  ( $T_a = +25^\circ C$ )

$t_R^{(Note)}$	$t_F^{(Note)}$	$t_{OFF}^{(Note)}$	$V_{BOT}^{(Note)}$
Max 5ms	Max 5ms	Min 20ms	Less than 0.3V

(Note) This function is guaranteed by design, not tested in production process.

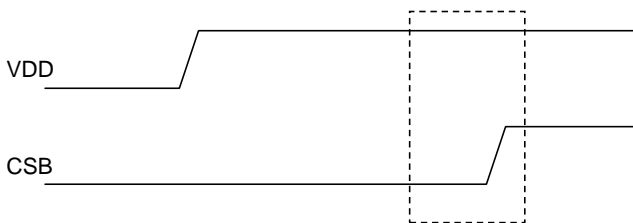
**Figure 23. Rising Waveform Diagram**

(2) If it is difficult to meet the above condition, execute the following sequence after Power ON.

Note however that it cannot accept command while supply is unstable or below the minimum supply range.

Note also that software reset is not a complete alternative to POR function.

(a) CSB = “L” → “H” condition



**Figure 24. CSB Timing**

(b) Execute Software Reset in ICSET command after CSB to “L”.

(Refer to “[ICSET](#)” command)

**Display off Operation in External clock mode**

After receiving MODESET(Display off), BU9795BKV enter to DISPOFF sequence synchronized with frame then Segment and Common pins output VSS level after 1frame of OFF data write.

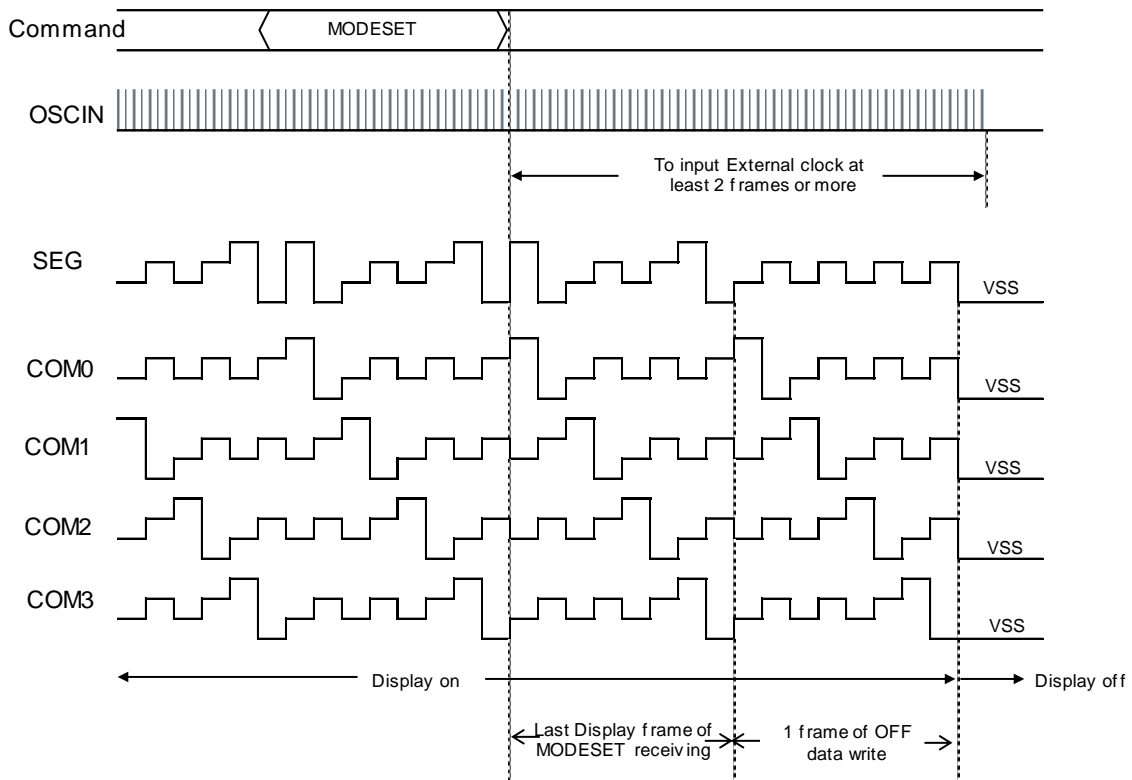
Therefore, in External clock mode, it is necessary to input the external clock based on each frame frequency setting after sending MODESET(Display off).

For the required number of clock, refer to Power save mode FR of DISCTL.

Input the external clock as below.

- DISCTL 320HZ setting(Frame frequency [Hz] = External clock [Hz] / 128), it needs over 256clk
- DISCTL 284HZ setting(Frame frequency [Hz] = External clock [Hz] / 144), it needs over 288clk
- DISCTL 213HZ setting(Frame frequency [Hz] = External clock [Hz] / 192), it needs over 384clk
- DISCTL 160HZ setting(Frame frequency [Hz] = External clock [Hz] / 256), it needs over 512clk
- DISCTL 80HZ setting(Frame frequency [Hz] = External clock [Hz] / 512), it needs over 1024clk
- DISCTL 71HZ setting(Frame frequency [Hz] = External clock [Hz] / 576), it needs over 1152clk
- DISCTL 64HZ setting(Frame frequency [Hz] = External clock [Hz] / 648), it needs over 1296clk
- DISCTL 53HZ setting(Frame frequency [Hz] = External clock [Hz] / 768), it needs over 1536clk

Refer to the timing chart below.



**Figure 25. External Clock Stop Timing**

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

**Operational Notes – continued****9. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**11. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**12. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

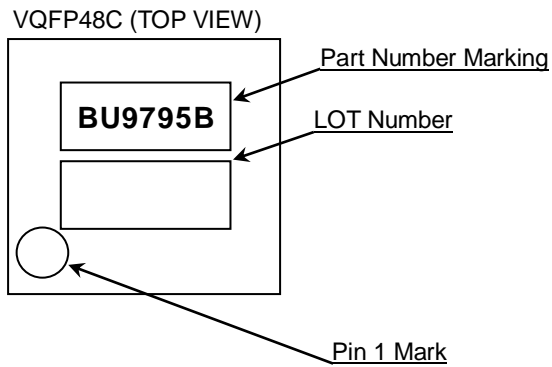
Ordering Information

B U 9 7 9 5 B K V	-	E 2
Part Number	Package KV : VQFP48C	Packaging Specification E2: Embossed tape and reel

Lineup

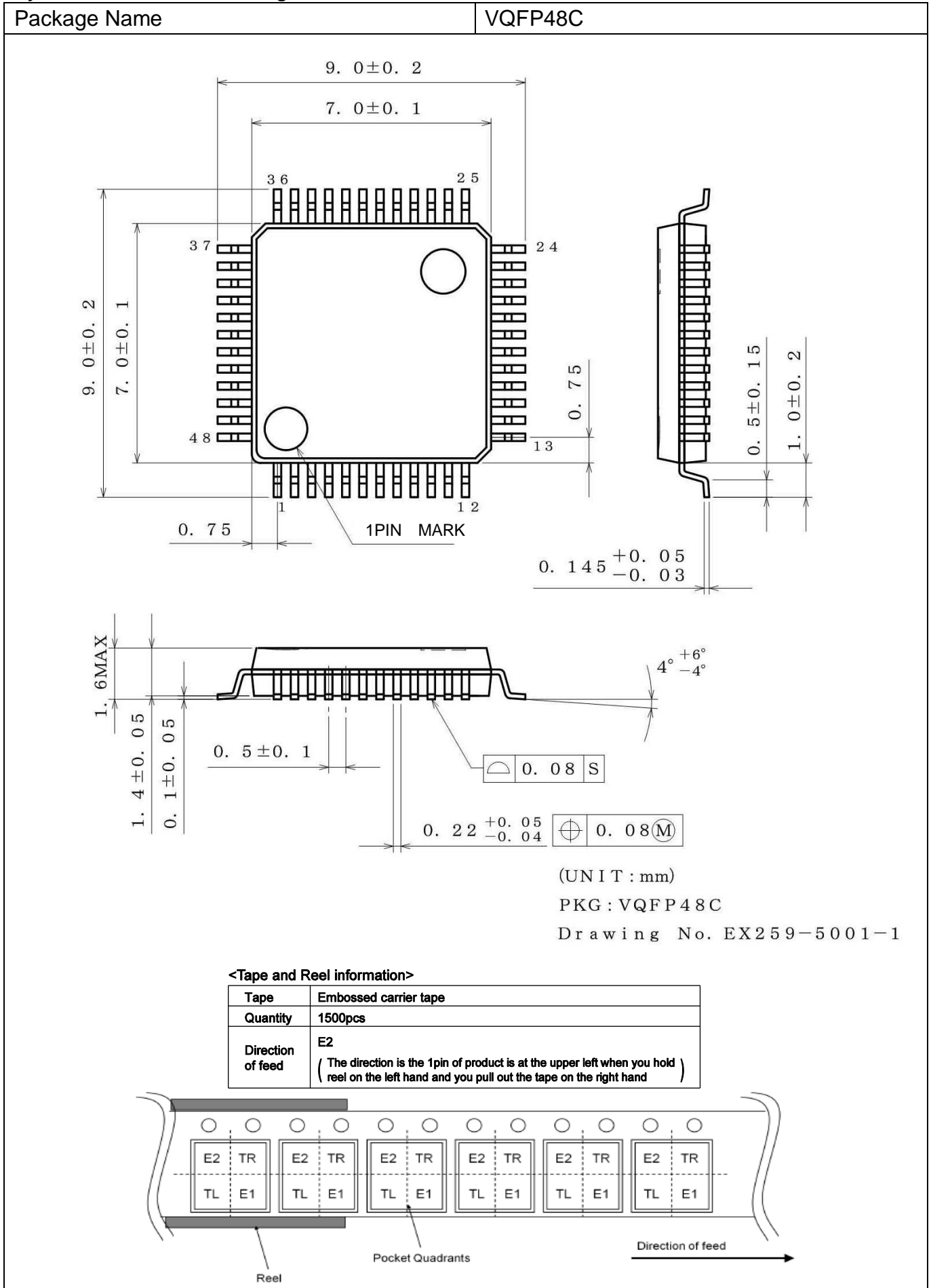
Package		Orderable Part Number
VQFP48C	Reel of 1500	BU9795BKV-E2

Marking Diagram





Physical Dimension and Packing Information



## Revision History

Date	Revision	Changes
25. Apr. 2016	001	New Release
10. Nov. 2017	002	Add BU9795BKV(VQFP48C) P.4 Add Caution2 in Absolute Maximum Ratings condition. (Moved from Operational Notes) P.23 Add the comment in Caution in Cautions of "Power- ON Condition." (Moved from Operational Notes) P.24 Add Display off operation in External clock mode P.25 Move "5. Thermal Consideration" to "Absolute Maximum Ratings condition" P.26 Move "13. Data transmission" to "Cautions of "Power ON Condition". P.27 Add VQFP48C to Ordering Information, Lineup and Marking Diagram P.29 Add VQFP48C Physical Dimension and Packing Information
01. Apr. 2020	003	Remove BU9795BGUW (VBGA049W040A)

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CLASS IV		CLASS III	

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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