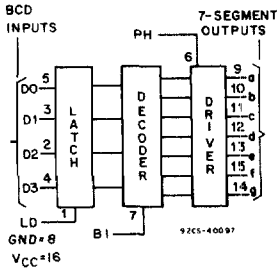


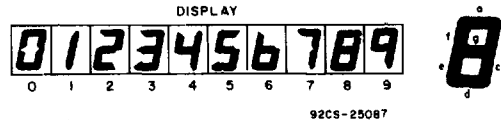
# CD54/74HC4543 CD54/74HCT4543

## High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

### BCD-to-7 Segment Latch/ Decoder/Driver for LCDs



**Type Features:**

- Input latches for BCD code storage
- Blanking capability
- Phase input for complementing outputs

The RCA CD54/74HC4543 and CD54/74HCT4543 high-speed silicon-gate devices are BCD-to-7 segment latch/decoder/drivers designed primarily for directly driving liquid-crystal displays. They have an active-high disable input (LD), an active high blanking input (BI) and a phase input (PH) to which a square wave is applied for liquid-crystal applications. This square wave is also applied to the backplane of the liquid-crystal display.

These devices can also be used, in conjunction with current amplifying devices, for driving LEDs, incandescent, fluorescent, and gas-discharge displays. For these applications the phase input provides a means for obtaining active-high or active-low segment outputs. (See Function Table.)

The CD54HC/HCT4543 are supplied in 16-lead ceramic dual-in-line frit-seal packages (F suffix). The CD74HC/HCT-4543 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

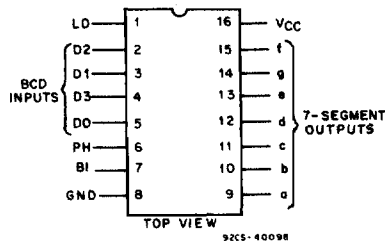
**Family Features:**

- Fanout (over temperature range):  
Standard outputs - 10 LSTTL loads  
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:  
CD74HC/HCT: -40 to +85° C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:  
2 to 6 V operation  
High noise immunity:  
 $N_{IL}=30\%$ ,  $N_{IH}=30\%$  of  $V_{CC}$ ; @  $V_{CC}=5 V$
- CD54HCT/CD74HCT types:  
4.5 to 5.5 V operation  
Direct LSTTL input logic compatibility  
 $V_{IL}=0.8 V \text{ max.}$ ,  $V_{IH}=2 V \text{ min.}$   
CMOS input compatibility  
 $I_L \leq 1 \mu A$  @  $V_{OL}$ ,  $V_{OH}$

FUNCTION TABLE

INPUTS					OUTPUTS							DISPLAY			
LD	BI	PH	D3	D2	D1	D0	a	b	c	d	e		f	g	
X	H	L	L	L	X	X	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	L	H	H	H	L	L	L	L	L	1
H	L	L	L	L	L	H	L	H	L	H	L	L	L	H	2
H	L	L	L	L	L	H	H	H	H	L	L	L	H	H	3
H	L	L	L	L	H	L	L	L	H	L	L	L	H	H	4
H	L	L	L	L	H	L	L	L	H	L	L	L	H	H	5
H	L	L	L	L	H	H	L	L	H	L	L	L	H	H	6
H	L	L	L	L	H	H	H	L	L	L	L	L	L	L	7
H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	8
H	L	L	L	L	H	L	L	L	H	H	L	L	L	L	9
H	L	L	L	L	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	L	L	H	H	L	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	L	L	L	L	L	L	L	L	..
as above	H		as above												as above

..Depends upon the BCD code previously applied when LD = High



TERMINAL ASSIGNMENT

# CD54/74HC4543 CD54/74HCT4543

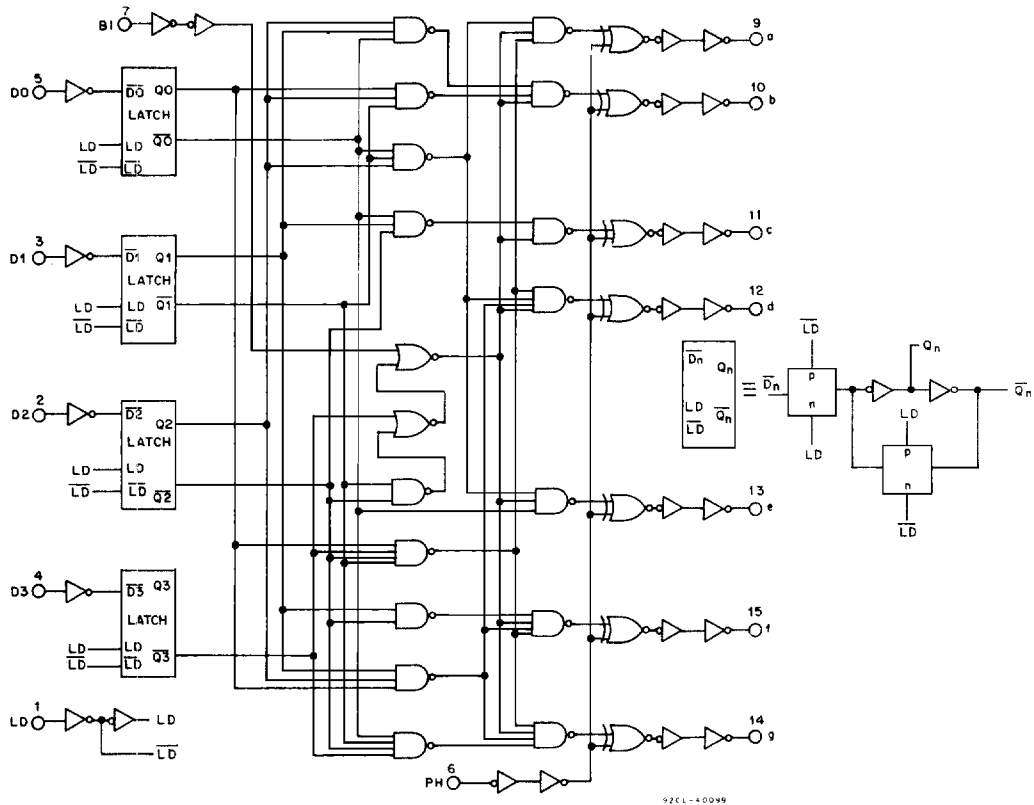


Fig. 1 - Logic diagram.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

**DC SUPPLY-VOLTAGE, ( $V_{CC}$ ):**

(Voltages referenced to ground) .....	-0.5 to +7 V
DC INPUT DIODE CURRENT, $I_{IK}$ (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) .....	$\pm 20$ mA
DC OUTPUT DIODE CURRENT, $I_{OK}$ (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) .....	$\pm 20$ mA
DC DRAIN CURRENT, PER OUTPUT ( $I_o$ ) (FOR $-0.5$ V $< V_o < V_{CC} + 0.5$ V) .....	$\pm 25$ mA
DC $V_{CC}$ OR GROUND CURRENT ( $I_{CC}$ ) .....	$\pm 50$ mA

**POWER DISSIPATION PER PACKAGE ( $P_o$ ):**

For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) .....	500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) .....	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F,H) .....	500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F,H) .....	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M) .....	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M) .....	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ ):**

PACKAGE TYPE F,H .....	-55 to $+125^\circ$ C
PACKAGE TYPE E,M .....	-40 to $+85^\circ$ C

**STORAGE TEMPERATURE ( $T_{stg}$ ) .....**

.....	-65 to $+150^\circ$ C
-------	-----------------------

**LEAD TEMPERATURE (DURING SOLDERING):**

At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max. ....	$+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only .....	$+300^\circ$ C

# CD54/74HC4543

# CD54/74HCT4543

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> =Full Package Temperature Range) V <sub>CC</sub> .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0	V <sub>CC</sub>	V
Operating Temperature, T <sub>A</sub> :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t <sub>r</sub> , t <sub>f</sub> :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

\*Unless otherwise specified, all voltages are referenced to Ground.

### SWITCHING CHARACTERISTICS (V<sub>CC</sub>=5 V, T<sub>A</sub>=25° C, Input t<sub>r</sub>, t<sub>f</sub>=6 ns)

CHARACTERISTIC	C <sub>L</sub> (pF)	TYPICAL VALUES		UNITS	
		HC	HCT		
Propagation Delay:				ns	
D <sub>n</sub> to Output	15	28	33		
LD to Output	15	31	32		
BI to Output	15	22	27		
PH to Output	15	17	27		
Power Dissipation Capacitance*	—	52	54		pF

\*C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$$

where f<sub>i</sub> = input frequency  
 f<sub>o</sub> = output frequency  
 C<sub>L</sub> = output load capacitance  
 V<sub>CC</sub> = supply voltage.

### PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V <sub>CC</sub> (V)	LIMITS										UNITS		
		25° C				-40° C to +85° C				-55° C to +125° C				
		HC		HCT		74HC		74HCT		54HC			54HCT	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.
Setup Time, t <sub>su</sub>	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
D <sub>n</sub> to LD	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time, t <sub>h</sub>	2	30	—	—	—	40	—	—	—	45	—	—	—	
D <sub>n</sub> to LD	4.5	6	—	8	—	8	—	10	—	9	—	12	—	
	6	5	—	—	—	7	—	—	—	8	—	—	—	
Latch Disable Pulse Width, t <sub>w</sub>	2	50	—	—	—	65	—	—	—	75	—	—	—	
	4.5	10	—	10	—	13	—	13	—	15	—	15	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	

# CD54/74HC4543

## CD54/74HCT4543

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4543/CD54HC4543										CD74HCT4543/CD54HCT4543								UNITS			
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES			54HCT TYPES		
	V <sub>I</sub> V	I <sub>O</sub> mA	V <sub>CC</sub> V	+25°C			-40/ +85°C		-55/ +125°C			V <sub>I</sub> V	V <sub>CC</sub> V	+25°C			-40/ +85°C			-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min			Max	Min	Max	Min	Max				
High-Level Input Voltage	V <sub>IH</sub>		2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5										
			6	4.2	—	—	4.2	—	4.2	—												
Low-Level Input Voltage	V <sub>IL</sub>		2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5										
			6	—	—	1.8	—	1.8	—	1.8	—											
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IL</sub> or -0.02	2	1.9	—	—	1.9	—	1.9	—	V <sub>IL</sub> or V <sub>IH</sub>	4.5	4.4	—	—	4.4	—	4.4	—	4.4	V	
CMOS Loads	V <sub>IH</sub>		6	5.9	—	—	5.9	—	5.9	—												
TTL Loads	V <sub>IL</sub>										V <sub>IL</sub> or V <sub>IH</sub>	4.5	3.98	—	—	3.84	—	3.7	—		V	
Non-Standard Output	V <sub>IH</sub>		-1.3	6	5.48	—	—	5.34	—	5.2												
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IL</sub> or 0.02	2	—	—	0.1	—	0.1	—	0.1	V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.1	—	0.1	—	0.1	—	V	
CMOS Loads	V <sub>IH</sub>		6	—	—	0.1	—	0.1	—	0.1												
TTL Loads	V <sub>IL</sub>										V <sub>IL</sub> or V <sub>IH</sub>	4.5	—	—	0.26	—	0.33	—	0.4	—	V	
Non-Standard Output	V <sub>IH</sub>		1.3	6	—	—	0.26	—	0.33	—												
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or Gnd	6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V <sub>CC</sub> & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or Gnd	0	6	—	—	8	—	80	—	160	V <sub>CC</sub> or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per Input pin: 1 unit load	ΔI <sub>CC</sub> *											V <sub>CC</sub> -2.1 to 5.5	—	100	360	—	450	—	490	—	μA	

\*For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

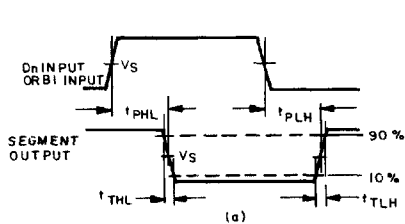
Input	Unit Loads*
D0, D1, D2	1
D3, BI	0.5
PH	1.25
LD	1.5

\*Unit Load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

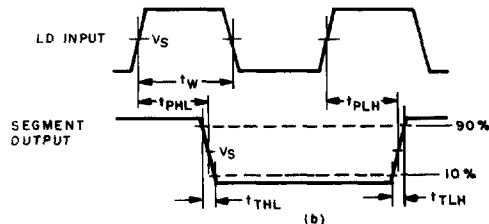
# CD54/74HC4543 CD54/74HCT4543

SWITCHING CHARACTERISTICS (C<sub>L</sub>=50 pF, Input t<sub>r</sub>,t<sub>f</sub>=6 ns)

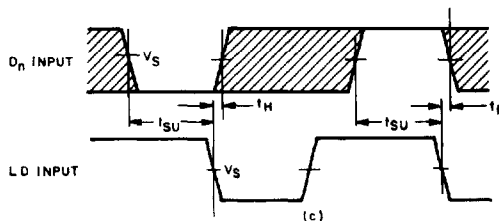
CHARACTERISTIC	V <sub>CC</sub>	LIMITS										UNITS			
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC			54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.	
Propagation Delay, D <sub>n</sub> to Output	t <sub>PLH</sub>	2	—	340	—	—	—	425	—	—	—	510	—	—	ns
	t <sub>PHL</sub>	4.5	—	68	—	80	—	85	—	100	—	102	—	120	
LD to Output	t <sub>PLH</sub>	2	—	370	—	—	—	465	—	—	—	555	—	—	ns
	t <sub>PHL</sub>	4.5	—	74	—	77	—	93	—	96	—	111	—	116	
BI to Output	t <sub>PLH</sub>	2	—	265	—	—	—	330	—	—	—	400	—	—	ns
	t <sub>PHL</sub>	4.5	—	53	—	66	—	66	—	83	—	80	—	99	
PH to Output	t <sub>PLH</sub>	2	—	200	—	—	—	250	—	—	—	300	—	—	ns
	t <sub>PHL</sub>	4.5	—	40	—	66	—	50	—	83	—	60	—	99	
Transition Time	t <sub>TLH</sub>	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
	t <sub>THL</sub>	4.5	—	50	—	50	—	63	—	63	—	75	—	75	
Input Capacitance	C <sub>i</sub>		—	10	—	10	—	10	—	10	—	10	—	10	pF



(a) WAVEFORMS SHOWING THE ADDRESS AND BLANKING (D<sub>n</sub>, BI) TO OUTPUT PROPAGATION DELAYS AND THE OUTPUT TRANSITION TIMES.



(b) WAVEFORMS SHOWING THE LATCH DISABLE INPUT (LD) TO OUTPUT PROPAGATION DELAYS AND THE OUTPUT TRANSITION TIMES.



NOTE  
THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE.

(c) WAVEFORMS SHOWING THE ADDRESS (D<sub>n</sub>) TO LATCH DISABLE (LD) INPUT SET-UP AND HOLD TIMES

92CM-40105

	54/74HC	54/74HCT
Input Level	V <sub>CC</sub>	3 V
Switching Voltage, V <sub>s</sub>	50% V <sub>CC</sub>	1.3 V

Fig. 2 - AC waveforms.

# CD54/74HC4543 CD54/74HCT4543

## APPLICATION CIRCUITS

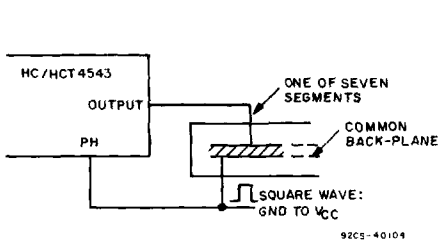


Fig. 3 - Connection to liquid-crystal (LCD) display readout.

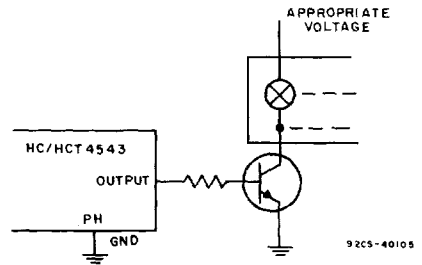


Fig. 4 - Connection to incandescent display readout.

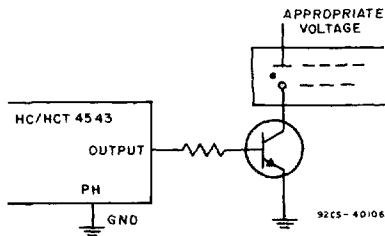


Fig. 5 - Connection to gas-discharge display readout.

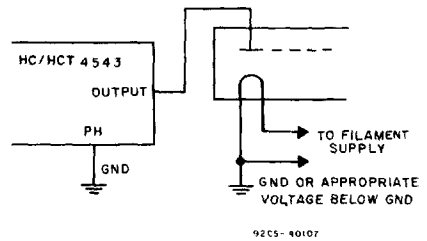


Fig. 6 - Connection to fluorescent display readout.