ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

T-51-09-12

1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter. The AD7541A is a direct replacement for the industry standard AD7541, offering improved performance in the areas of latch-up, lower gain error and gain temperature coefficient.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
–1	AD7541AS(X)/883B
–2	AD7541AT(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-18	18-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted. Pin numbers refer to DIP package.)

V_{DD} (Pin 16) to GND . . . . . +17V
V_{REF} (Pin 17) to GND . . . . . ±25V
V_{RFB} (Pin 18) to GND . . . . . ±25V
Digital Input Voltage (Pin 4–Pin 15) to GND . . . . . −0.3V, V_{DD}
V_{PIN1}, V_{PIN2} to GND . . . . . −0.3V to V_{DD}
Power Dissipation
  Up to +75°C 450mW
  Derates above +75°C . . . . . 6mW/°C
Operating Temperature Range . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-18 and E-20A
θ_{JA} = 120°C/W for Q-18 and E-20A

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Test	Symbol	Device	Design Limit @ +125°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	–1,2	12					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits, T_{min} to T_{max}	± LSB
		–2	1/2	1	1/2	1/2		
Gain Error[2]	AE	–1	8	6	8			± LSB max
		–2	5	6	5	3		
Gain Tempco	TC_{AE}	–1,2	5					± ppm/°C max
Power Supply Rejection	PSRR	–1,2	0.02	0.01	0.02		ΔV_{DD} = ± 5%	± % per % max
Output Leakage Current								
Pin 1	I_{OUT1}	–1,2	200	5	200		Digital Inputs = 0V	± nA max
Pin 2	I_{OUT2}	–1,2	200	5	200		Digital Inputs = V_{DD}	± nA max
Output Current Settling Time		–1,2	0.6				To ± 1/2LSB, $R_{OUT}1$ = 100Ω, C_{OUT1} = 13pF Digital Inputs = V_{IH} to V_{IL} or V_{IL} to V_{IH}	µs typ
Feedthrough Error[3]	FT	–1,2	1				V_{REF} = ± 10V 10kHz Sinewave T_A = +25°C	mV p-p typ
Reference Input Resistance	R_{IN}	–1,2	7	7	7			kΩ min
		–1,2	18	18	18			kΩ max
Digital Input High Voltage	V_{IH}	–1,2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	–1,2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	–1,2	1	1	1		V_{IN} = 0V or V_{DD}	± µA max
Digital Input Capacitance	C_{IN}	–1,2	8					pF max
Output Capacitance								
Pin 1	C_{OUT1}	–1,2	200				Digital Inputs = V_{IH}	pF max
Pin 2	C_{OUT2}	–1,2	70				Digital Inputs = V_{IH}	pF max
Pin 1	C_{OUT1}	–1,2	70				Digital Inputs = V_{IL}	pF max
Pin 2	C_{OUT2}	–1,2	200				Digital Inputs = V_{IL}	pF max
Supply Current from V_{DD}	I_{DD}	–1,2	2	2	2		Digital Inputs = V_{IH} or V_{IL}	mA max
			500	100	500		Digital Inputs = 0V or V_{DD}	µA max

NOTES
[1] V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise stated.
[2] Measured using internal feedback resistor and includes effect of leakage current and gain TC.
[3] Feedthrough error can be reduced by connecting the lid of the ceramic package to ground.

Table 1.

REV. B

3.2.1 Functional Block Diagram and Terminal Assignments.

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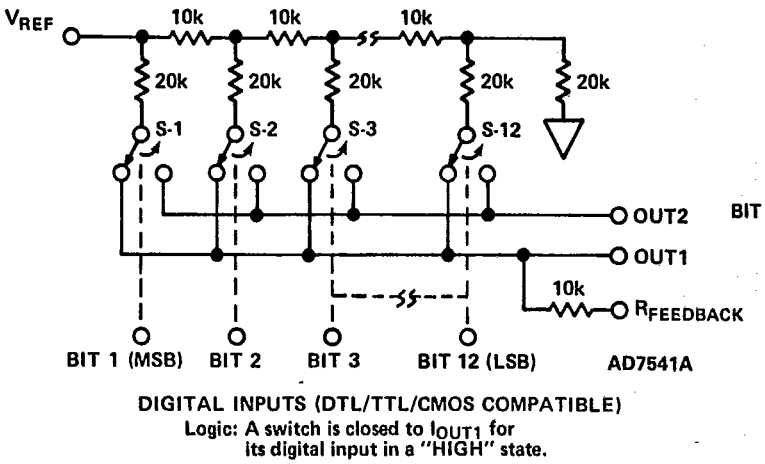
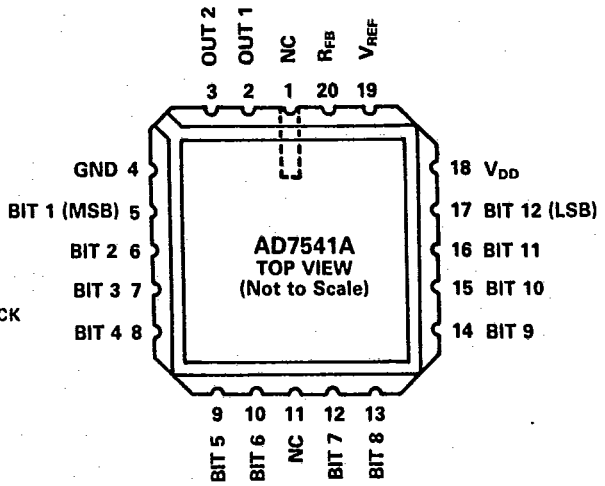


DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

E Package (LCC)

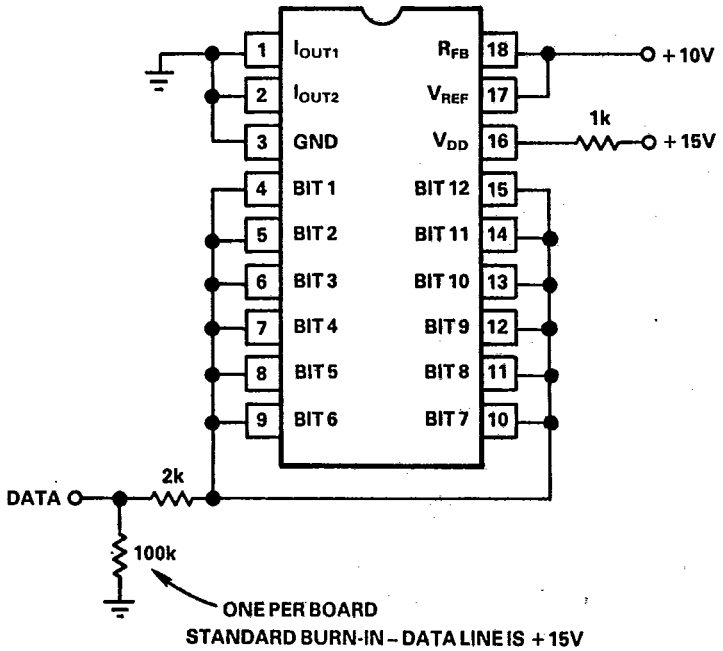


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



STANDARD BURN-IN – DATA LINE IS +15V