REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made changes to 3.3, 4.2, 4.3.1, and 4.3.2. Made changes to table I. Editorial changes throughout.	90-03-08	M. A. Frye
B	Add device type 07. Add vendors CAGEs 1ES66 and 54186. Editorial changes throughout.	93-01-22	M. A. Frye
C	Update boilerplate and make editorial changes throughout. - ro	98-07-06	Raymond Monnin
D	Update drawing to current requirements. Editorial changes throughout. – drw	04-01-07	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	D	D	D																	
SHEET	15	16	17																	

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Marcia B. Kelleher

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-01-28

REVISION LEVEL
D

MICROCIRCUIT, CMOS, 12-BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87702**

SHEET 1 OF 17

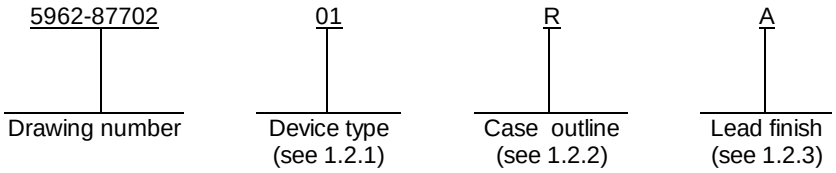
DSCC FORM 2233
APR 97

5962-E557-03

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7545S	CMOS 12-bit buffered DAC
02	7545T	CMOS 12-bit buffered DAC
03	7545U	CMOS 12-bit buffered DAC
04	7545AU	CMOS 12-bit buffered DAC
05	7545B	CMOS 12-bit buffered DAC
06	7545A	CMOS 12-bit buffered DAC
07	7545S	CMOS 12-bit buffered DAC

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}) ..... +5 V dc to +15 V dc
V_{REF} to GND ..... -0.3 V dc to +17 V dc
Digital input voltage to DGND ..... -0.3 V dc to V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25 V dc
V pin 1 to DGND ..... -0.3 V dc to V_{DD}
AGND to DGND ..... -0.3 V dc to V_{DD}
Power dissipation (P_D):
  Up to +75°C ..... 450 mW
  Derates above +75°C ..... 6 mW/°C
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance junction-to-ambient (θ_{JA}):
  Case R ..... +120°C/W
  Case 2 ..... +120°C/W
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Operating ambient temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Mode selection. The mode selection shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C. It is not included in PDA.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	V_{DD} = +5 V	1, 2, 3	All	12		Bits
		V_{DD} = +15 V			12		
Relative accuracy	RA	V_{DD} = +5 V	1, 2, 3	01, 07		±2	LSB
			1	02		±2	
			2, 3			±1	
		V_{DD} = +5 V, T_A = +25°C 2/	12	02		±1	
		V_{DD} = +5 V	1	03, 04		±2	
				05, 06		±0.5	
			2, 3	03, 04, 05, 06		±0.5	
		V_{DD} = +5 V, T_A = +25°C 2/	12	03, 04, 05, 06		±0.5	
		V_{DD} = +15 V	1, 2, 3	01, 07		±2	
			1	02		±2	
			2, 3			±1	
		V_{DD} = +15 V, T_A = +25°C 2/	12	02		±1	
		V_{DD} = +15 V	1	03, 04		±2	
				05, 06		±0.5	
		V_{DD} = +15 V 2/	2, 3	03, 04, 05, 06		±0.5	
			12			±0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Differential nonlinearity	DNL	V_{DD} = +5 V, 10-bit monotonic	1, 2, 3	01, 07		±4	LSB
		V_{DD} = +5 V, 12-bit monotonic	1	02, 03, 04		±4	
				05, 06		±1	
		V_{DD} = +5 V, 2/ 12-bit monotonic	2, 3	02, 03, 04, 05, 06		±1	
			12			±1	
		V_{DD} = +15 V, 10-bit monotonic	1, 2, 3	01, 07		±4	
		V_{DD} = +15 V, 12-bit monotonic	1	02, 03, 04		±4	
				05, 06		±1	
		V_{DD} = +15 V, 2/ 12-bit monotonic	2, 3	02, 03, 04, 05, 06		±1	
			12			±1	
Power supply rejection	PSRR	V_{DD} = +5 V, ΔV_{DD} = ±5 %	1	01, 02, 03, 04, 07		.015	±% / %
			2, 3			.03	
			1	05, 06		.002	
			2, 3			.004	
		V_{DD} = +15 V, ΔV_{DD} = ±5 %	1	01, 02, 03, 04, 07		.01	
			2, 3			.02	
			1	05, 06		.002	
			2, 3			.004	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain error 3/	AE	V_{DD} = +5 V, DAC register loaded with 1111 1111 1111	1, 2, 3	01, 07		±20	LSB
			1	02		±20	
			2, 3			±10	
		V_{DD} = +5 V, T_A = +25°C 2/ DAC register loaded with 1111 1111 1111	12	02		±10	
		V_{DD} = +5 V, DAC register loaded with 1111 1111 1111	1	03		±20	
				05		±3	
			2, 3	03		±6	
				05		±4	
		V_{DD} = +5 V, T_A = +25°C 2/ DAC register loaded with 1111 1111 1111	12	03		±5	
				05		±3	
		V_{DD} = +5 V, DAC register loaded with 1111 1111 1111	1	04		±20	
				06		±1	
			2, 3	04, 06		±2	
		V_{DD} = +5 V, T_A = +25°C 2/ DAC register loaded with 1111 1111 1111	12	04, 06		±1	
		V_{DD} = +15 V, DAC register loaded with 1111 1111 1111	1, 2, 3	01, 07		±25	
			1	02		±25	
			2, 3			±15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain error 3/	AE	V_{DD} = +15 V, T_A = +25°C, DAC register loaded with 1111 1111 1111 2/	12	02		±15	LSB
		V_{DD} = +15 V, DAC register loaded with 1111 1111 1111	1	03		±25	
				05		±3	
			2, 3	03		±10	
				05		±4	
		V_{DD} = +15 V, T_A = +25°C, DAC register loaded with 1111 1111 1111 2/	12	03		±10	
				05		±3	
		V_{DD} = +15 V, DAC register loaded with 1111 1111 1111	1	04		±25	
				06		±1	
			2, 3	04		±7	
				06		±2	
		V_{DD} = +15 V, T_A = +25°C, DAC register loaded with 1111 1111 1111 2/	12	04		±6	
				06		±1	
Output leakage current Pin 1	I_{OUT1}	V_{DD} = +5 V, DB0 to DB11 = 0 V, WR, CS = 0 V	1	All		±10	nA
			2, 3			±200	
		V_{DD} = +15 V, DB0 to DB11 = 0 V, WR, CS = 0 V	1	All		±10	
			2, 3			±200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Referenced input resistance, pin 19 to ground	R_{IN}	V_{DD} = +5 V	1, 2, 3	01, 02, 03, 04, 07	7	25	kΩ
				05, 06	7	15	
		V_{DD} = +15 V	1, 2, 3	01, 02, 03, 04, 07	7	25	
				05, 06	7	15	
Digital input high voltage	V_{IH}	V_{DD} = +5 V	1, 2, 3	All	2.4		V
		V_{DD} = +15 V			13.5		
Digital input low voltage	V_{IL}	V_{DD} = +5 V	1, 2, 3	All		0.8	V
		V_{DD} = +15 V				1.5	
Digital input leakage current	I_{IN}	V_{DD} = +5 V	1	All		±1	µA
			2, 3			±10	
		V_{DD} = +15 V	1			±1	
			2, 3			±10	
Supply current from V_{DD}	I_{DD}	V_{DD} = +5 V, all digital inputs V_{IL} or V_{IH}	1, 2, 3	All		2	mA
		V_{DD} = +15 V, all digital inputs V_{IL} or V_{IH}				2	
		V_{DD} = +5 V, all digital inputs = 0 or V_{DD}	1	01, 02, 03, 04, 07		100	µA
			2, 3			500	
			1, 2, 3	05, 06		100	
		V_{DD} = +15 V, all digital inputs = 0 or V_{DD}	1	01, 02, 03, 04, 07		100	
			2, 3			500	
			1, 2, 3	05, 06		100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain temperature coefficient	TCAE	V_{DD} = +5 V 4/	1, 2, 3	All		±5	ppm/°C
		V_{DD} = +15 V 4/		01, 02, 03, 04, 07		±10	
				05, 06		±5	
Feedthrough error	FT	V_{DD} = +5 V, 4/ 5/ V_{REF} = ±10 V, 10 kHz sinewave	4, 5, 6	All		10	mV_{P-P}
		V_{DD} = +15 V, 4/ 5/ V_{REF} = ±10 V, 10 kHz sinewave				10	
Digital input capacitance	C_{IN}	V_{DD} = +5 V, 6/ V_{IN} = 0 V, T_A = +25°C, DB0 to DB11	4	01, 02, 03, 04, 07		5	pF
				05, 06		8	
		V_{DD} = +5 V, T_A = +25°C, $\overline{WR}$, $\overline{CS}$		All		20	
		V_{DD} = +15 V, 6/ V_{IN} = 0 V, T_A = +25°C, DB0 to DB11		01, 02, 03, 04, 07		5	
				05, 06		8	
		V_{DD} = +15 V, 6/ T_A = +25°C, $\overline{WR}$, $\overline{CS}$		All		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance	C_{OUT1}	V_{DD} = +5 V, 4/ DB0 to DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V, T_A = +25°C	4	All		70	pF
		V_{DD} = +15 V, 4/ DB0 to DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V, T_A = +25°C				70	
Output capacitance	C_{OUT2}	V_{DD} = +5 V, 4/ DB0 to DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0 V, T_A = +25°C	4	All		200	pF
		V_{DD} = +15 V, 4/ DB0 to DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0 V, T_A = +25°C				200	
Chip select to write setup time	t_{CS}	V_{DD} = +5 V 7/	9, 10, 11	01, 02, 03, 04	170		ns
				05, 06, 07	280		
		V_{DD} = +15 V 7/		01, 02, 03, 04	95		
				05, 06, 07	180		
Chip select to write hold time	t_{CH}	V_{DD} = +5 V 7/	9, 10, 11	All	0		ns
		V_{DD} = +15 V 7/			0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write pulse width	t_{WR}	V_{DD} = +5 V, 7/	9, 10, 11	01, 02, 03, 04	170		ns
		$t_{CS} \ge t_{WR}$, $t_{CH} \ge 0$		05, 06, 07	250		
		V_{DD} = +15 V, 7/		01, 02, 03, 04	95		
		$t_{CS} \ge t_{WR}$, $t_{CH} \ge 0$		05, 06, 07	160		
Data setup time	t_{DS}	V_{DD} = +5 V 7/	9, 10, 11	All	150		ns
		V_{DD} = +15 V 7/		01, 02, 03, 04	80		
				05, 06, 07	100		
Data hold time	t_{DH}	V_{DD} = +5 V 7/	9, 10, 11	01, 02, 03, 04	5		ns
				05, 06, 07	10		
		V_{DD} = +15 V 7/		01, 02, 03, 04	5		
				05, 06, 07	10		

1/ V_{OUT1} = 0 V, V_{REF} = +10 V, AGND = DGND, unless otherwise specified.

2/ See 4.3.1c.

3/ Measured using internal feedback resistor and includes effect of 5 ppm maximum gain T_C.

4/ These parameters may be guaranteed, if not tested, to the limits specified in table I herein.

5/ Feedthrough error can be reduced by connecting the metal lid to ground.

6/ Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance.

7/ Timing in accordance with figure 4.

Device types	All
Case outlines	R and 2
Terminal number	Terminal symbol
1	OUT1
2	AGND
3	DGND
4	DB11(MSB)
5	DB10
6	DB9
7	DB8
8	DB7
9	DB6
10	DB5
11	DB4
12	DB3
13	DB2
14	DB1
15	DB0 (LSB)
16	$\overline{CS}$
17	$\overline{WR}$
18	V_{DD}
19	V_{REF}
20	RFB

FIGURE 1. Terminal connections.

Write mode	Hold mode
$\overline{CS}$ and $\overline{WR}$ low DAC responds to data bus (DB0 to DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus(DB0 to DB11) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed high state.

FIGURE 2. Mode selection.

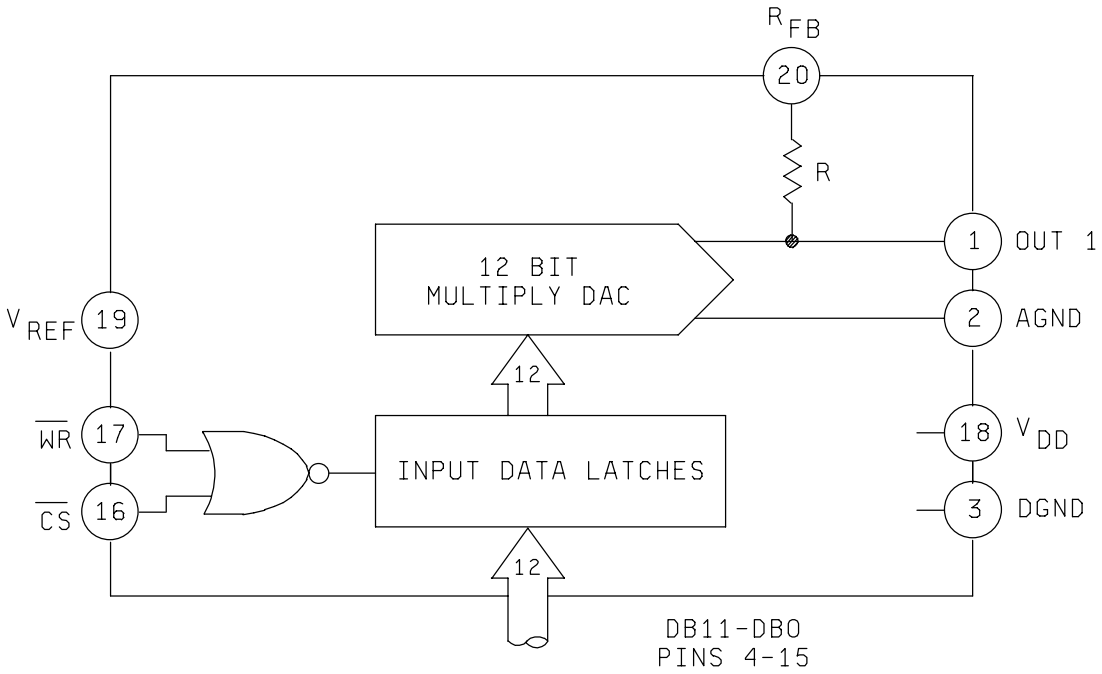
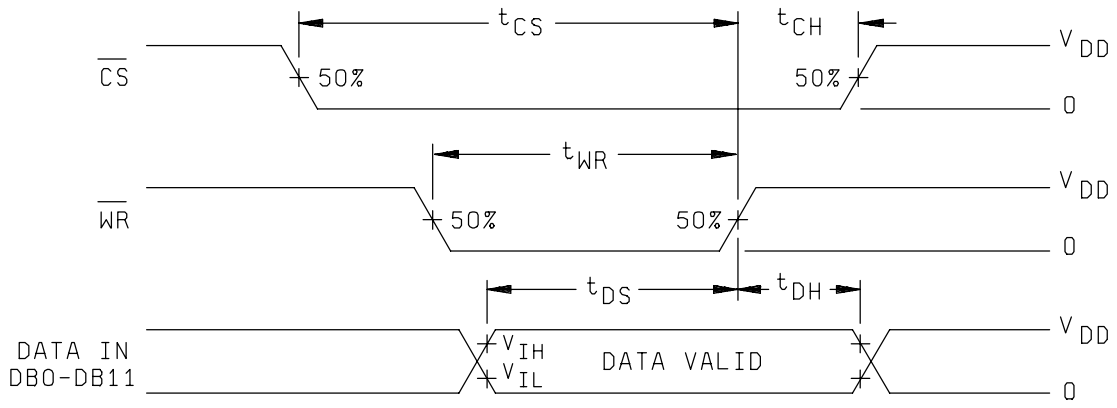


FIGURE 3. Logic diagram.



NOTES:

V_{DD} = +5 V; $t_r = t_f$ = 20 ns
V_{DD} = +15 V; $t_r = t_f$ = 40 ns
All input signal rise and fall times measured from 10 to 90 percent of V_{DD}.
Timing measurement reference level is $(V_{IH} + V_{IL}) / 2$.

FIGURE 4. Write cycle timing diagram.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3,12
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9**, 10***, 11***, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroup 9, if not tested, shall be guaranteed to the specified limits in table I for device type 07.
*** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-01-07

Approved sources of supply for SMD 5962-87702 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8770201RA	24355	AD7545SQ/883B
	1ES66	MX7545SQ/883B
5962-87702012A	3/	AD7545SE/883B
5962-87702012C	1ES66	MX7545SE/883B
5962-8770202RA	24355	AD7545TQ/883B
	1ES66	MX7545TQ/883B
5962-87702022A	3/	AD7545TE/883B
5962-87702022C	1ES66	MX7545TE/883B
5962-8770203RA	24355	AD7545UQ/883B
	1ES66	MX7545UQ/883B
5962-87702032A	3/	AD7545UE/883B
5962-87702032C	1ES66	MX7545UE/883B
5962-8770204RA	24355	AD7545AUQ/883B
	1ES66	MX7545AUQ/883B
5962-87702042A	24355	AD7545AUE/883B
5962-8770205RA	3/	PM7545BR/883
5962-87702052A	3/	PM7545BRC/883
5962-8770206RA	3/	PM7545AR/883
5962-87702062A	3/	PM7545ARC/883
5962-8770207RA	3/	MP7545SD/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
1ES66	Maxim Integrated Products 120 San Gabriel Drive Sunnyvale, CA 94086
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Bay F-1 Raheen Industrial Estate Limerick, Ireland

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.