DS1844
Quad Digital Potentiometer

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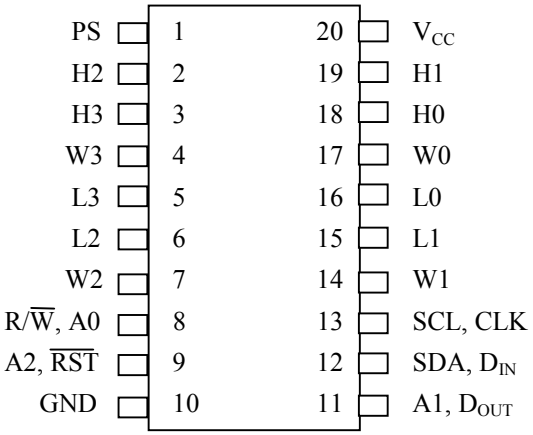
FEATURES

- Four independent, digitally controlled 64-position potentiometers
- Two interface control options
  - 5-wire serial
  - 2-wire addressable
- Standard resistance values
  - DS1844-010 10 kΩ
  - DS1844-050 50 kΩ
  - DS1844-100 100 kΩ
- Mixed resistor value combinations (contact factory for availability)
- Operating Temperature Range
  - Industrial: -40°C to +85°C

PIN ASSIGNMENT



20-Pin DIP (300-mil)
20-Pin SOIC (300-mil)
20-Pin TSSOP (173-mil)

PIN DESCRIPTION

V_{CC}	-	2.7V to 5.5V
PS	-	Port Select
A0, A1, A2	-	Device Select Pins (2-Wire)
SDA	-	Serial Data I/O (2-Wire)
SCL	-	Serial Clock (2-Wire)
R/$\overline{W}$	-	Read/Write enable (5-Wire)
$\overline{RST}$	-	Serial Port Reset Input (5-Wire)
D_{IN}	-	Serial Port Data Input (5-Wire)
CLK	-	Serial Port Clock Input (5-Wire)
D_{OUT}	-	Cascade Data Output (5-Wire)
H_0-H_3	-	High-end Terminal of Pot
L_0-L_3	-	Low-end Terminal of Pot
W_0-W_3	-	Wiper Terminal of Pot
GND	-	Ground

DESCRIPTION

The DS1844 Quad Digital Potentiometer is a four-channel, digitally controlled linear potentiometer. Each potentiometer is comprised of 63 equi-resistive sections and has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low-side terminals, L_X. The wiper position on the resistor ladder is selected via an 8-bit register value. Communication and control of the device are supported by two types of serial interface. These include a 5-wire I/O shift register interface and a 2-wire addressable interface.

The DS1844 is available in standard 10 kΩ, 50 kΩ, and 100 kΩ versions. Mixed resistor combinations are also available through custom setups. The DS1844 is specified to operate over the industrial temperature range: -40°C to +85°C. Packages for the DS1844 include 20-pin DIPs, SOICs, and TSSOPs.

OPERATION

The DS1844 contains four 64-position potentiometers. Each potentiometer is independent and has three accessible terminals, which include H_X, L_X, and W_X. Each potentiometer is comprised of 63 individual resistor elements. Between each resistor element is a tap-point that is multiplexed to the wiper terminal, W_X. Additionally, the wiper terminal can be multiplexed directly to the end-terminals, H_X and L_X.

The DS1844 supports two interface control options. Both options allow for the direct placement of the wiper position on the resistor ladder. Each wiper has an associated 6-bit register used to hold its positional value.

The DS1844 is a volatile device and will always power-up with the wiper positions set to mid-tap (position 32-decimal). The end-terminal H_X will have wiper position value 63-decimal and the L_X terminal will have wiper position value 0-decimal. Because the DS1844 is a 64-position device only 6 bits of data are necessary to write a wiper's value. However, communication with the DS1844 will require using a full 8 bits, with the remaining 2 bits specifying the potentiometer selected. A discussion of proper communication protocol is provided under the section entitled Serial Port Operation. A block diagram of the DS1844 is shown in Figure 1.

SERIAL PORT OPERATION

As stated, the DS1844 can support two types of serial interface control. This includes a 5-wire serial interface and a 2-wire addressable interface. The type interface supported during operation is selectable via the port select input pin, PS. Additionally, certain pins provide dual functionality dependent on the serial port selected. The pin description table lists pin functionality according to the interface selected.

5-Wire Serial Port Control

The 5-wire serial interface provides an 8-bit I/O shift register for loading and reading wiper data. The 5-wire serial interface control is selected when the port select input, PS, is in a low state. This interface is controlled by the signals $\overline{RST}$, DIN, DOUT, CLK, and R/$\overline{W}$. Timing diagrams for the 5-wire serial port can be found in Figure 3. Timing information for the 5-wire serial port is provided in the AC Electrical Characteristics table for 5-wire serial communications.

Data is loaded MSB first and in multiples of 8 bits. The 8-bit data to specify wiper position has the format or protocol as that shown in Figure 2. The 8-bit data is divided into potentiometer select data and wiper position value. The 6 least significant bits of data specify the wiper position value while the 2 most significant bits specify the potentiometer to be loaded. This allows the interface control logic/protocol to provide order independent potentiometer loading, as well as variable-length data loads.

As stated earlier, the 5-wire serial port is selected when the PS input is in a low state. If the device will only be used in the 5-wire mode, the PS input can be tied directly to ground. Communication via the 5-wire interface is enabled when $\overline{RST}$ is in a high state. A low-to-high transition on the $\overline{RST}$ indicates the start of a communication transaction with the DS1844. While $\overline{RST}$ is high, data can be read or written to the part. Data will be read or written dependent on the state of the read-write enable input, R/$\overline{W}$. The state of R/$\overline{W}$ must be stable before a low-to-high transition on $\overline{RST}$. Once the $\overline{RST}$ input has begun a communication transaction, the serial port will ignore any transitions on the R/$\overline{W}$ input.

When *writing* data, the R/$\overline{W}$ input should be in a *low state*. Once $\overline{RST}$ has activated the port, a data bit is latched (or valid) on the low-to-high transition of the CLK signal. Once, eight low-to-high transitions have occurred on the CLK input, the associated 8-bit data block will be loaded as the wiper's value on the falling edge of the eighth clock pulse. Potentiometer wiper values can be loaded in any order. Also, potentiometer wiper data can be loaded 1, 2, 3, or 4 bytes at a time. When $\overline{RST}$ transitions from high to low, the 5-wire port will be disabled.

While $\overline{RST}$ is high and R/$\overline{W}$ is low, (the write or load state) the cascade data output, D_{OUT} will be inhibited; preventing the passing of data from D_{IN} to D_{OUT} . However, when $\overline{RST}$ is low data is passed directly from D_{IN} to D_{OUT} .

When *reading* data, the R/$\overline{W}$ input should be in a high state. Once $\overline{RST}$ has enabled the port, data can be clocked out of the device and will appear on the D_{OUT} terminal. A data bit will be valid on the falling edge of a clock pulse after a maximum time period of 20 ns (of that falling edge). Data will appear on D_{OUT} most significant bit (MSB) first and starting with potentiometer-0, followed by potentiometer-1 and so forth.

2-Wire Addressable Serial Port Control

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1844 operates as a slave on the two-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The 2-wire serial port is selected when the port select input, PS, is in a high-state. The following I/O terminals control the 2-wire serial port: SDA, SCL, A0, A1, A2, PS=1. Timing diagrams for the 2-wire serial port can be found in Figures 4 through 8. Timing information for the 2-wire serial port is provided in the AC Electrical Characteristics table for 2-wire serial communications.

The following bus protocol has been defined (See Figure 4).

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figure 4 details how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a 9th bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS1844 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. Data transfer from a slave transmitter to a master receiver. The 1st byte (the command/control byte) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1844 may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCL, respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address and direction bit.

2. Slave transmitter mode: The 1st byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1844 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A command/control byte is the 1st byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the DS1844, this is set as ***0101*** binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address (A2, A1, A0). They are used by the master device to select which of eight devices is to be accessed. When reading or writing the DS1844, the device-select bits must match the device-select pins (A2, A1, A0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1 a read operation is selected, and when set to a 0 a write operation is selected. Figure 5 shows the command/control byte structure for the DS1844.

Following the START condition, the DS1844 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 0101 control code, the appropriate device address bits, and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

COMMAND AND PROTOCOL

The command and protocol structure of the DS1844 allows the user to read or write the potentiometer(s). Additionally, the 2-wire command/protocol structure of the DS1844 will support eight different devices and a maximum of 32 channels that can be uniquely controlled. The command structures for the device are presented in Figures 6 and 7. Potentiometer data values and control and command values are always transmitted most significant bit (MSB) first. During communications, the receiving unit always generates the acknowledgement.

Reading the DS1844

As shown in Figure 6, the DS1844 provides one ***read command operation***. This operation allows the user to read all potentiometers. Specifically, the R/W bit of the command/control byte is set equal to a 1 for a read operation. Communication to read the DS1844 begins with a START condition which is issued by the master device. The command/control byte from the master device will follow the START condition. Once the command/control byte has been received by the DS1844, the part will respond with an ACKNOWLEDGE. The read/write bit of the command/control byte, as stated, should be set equal to 1 for reading the DS1844.

When the master has received the ACKNOWLEDGE from the DS1844, the master can then begin to receive potentiometer wiper data. The value of the potentiometer-0 wiper position will be the first returned from the DS1844, followed by potentiometer-1 and so forth. Once the 8 bits of the potentiometer-0 wiper position have been transmitted, the master will need to issue an ACKNOWLEDGE, unless it is the only byte to be read, in which case the master issues a NOT ACKNOWLEDGE. If desired the master may stop the communication transfer at this point by issuing the STOP condition. However, if the value of the remaining potentiometers is needed, transfer can continue by clocking the 8 bits of the potentiometer-1 value, followed by an ACKNOWLEDGE, and so forth. Final communication transfer is terminated by issuing the STOP command. Again, the flow of the read operation is presented in Figure 6.

Writing the DS1844

A data flow diagram for writing the DS1844 is shown in Figure 7. The DS1844 has one write command that is used to change the position(s) of the wiper. The 2-wire serial interface write structure is similar to that of the 5-wire serial write. However, there are differences.

All the write operations begin with a START condition. Following the START condition, the master device will issue the command/control byte. The read/write bit of the command/control byte will be set to

0 for writing the DS1844. Once the command/control byte has been issued and the master receives the acknowledgment from the DS1844, potentiometer wiper data is transmitted to the DS1844 by the master device.

As in the case of the 5-wire serial protocol, a data byte for the DS1844 will contain *potentiometer select* data and *wiper position value*. The six least significant bits of data specify the wiper position value while the two most significant bits specify the potentiometer to be loaded. When the DS1844 has received the data byte, it will respond with an ACKNOWLEDGE. At this point, the new wiper value for the potentiometer selected will be updated in the DS1844. The master device, after the receipt of the ACKNOWLEDGE, can continue to transmit additional data bytes or if the transaction is complete respond with the STOP condition. Additionally, the DS1844 does not require a specific order for writing a particular potentiometer wiper's data. The 2-wire serial timing diagram is presented in Figure 8.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		+2.7		+5.5	V	1
Resistor Inputs	L,H,W		GND -0.5		V_{CC} +0.5	V	1,12

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC} =2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}				2.5	mA	19
Input Leakage	I_{LI}		-1		+1	µA	
Wiper Resistance	R_W			250	500	Ohms	
Wiper Current	I_W				1	mA	
Input Logic 1	V_{IH}		$0.7V_{CC}$		V_{CC}+0.5	V	1,2
Input Logic 0	V_{IL}		GND-0.5		$0.3V_{CC}$	V	1,2
Input Logic levels A0, A1, A2		Input Logic 1 Input Logic 0	$0.7V_{CC}$ GND-0.5		V_{CC}+0.5 $0.3V_{CC}$	V	11
Input Current each I/O pin		$0.4<V_{I/O}<0.9V_{DD}$	-10		+10	µA	
Standby Current 3V 5V	I_{stby}			 15 25	 40 60	µA	4
Low Level Output Voltage (SDA)	V_{OL1}	3 mA sink current	0.0		0.4	V	
	V_{OL2}	6 mA sink current	0.0		0.6	V	
I/O Capacitance	$C_{I/O}$				10	pF	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	22
D_{OUT} Output @ 2.4V	I_{OH}		-1.0			mA	23,24
D_{OUT} Output @ 0.4V	I_{OL}				4	mA	23,24

ANALOG RESISTOR CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
End-to-End Resistor Tolerance			-20		+20	%	25
Absolute Linearity			-0.5		+0.5	LSB	16
Relative Linearity			-0.25		+0.25	LSB	17
-3dB Cutoff frequency	f_{cutoff}					kHz	13
Temperature Coefficent				750		ppm/°C	18

2-WIRE ADDRESSABLE INTERFACE

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Port Select Setup	t_{SETUP}		30			ns	20,22
SCL Clock Frequency	f_{SCL}		0 0		400 100	kHz	*,8 **,22
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3 4.7			µs	*,8 **,22
Hold Time (repeated) START Condition	$t_{HD:STA}$		0.6 4.0			µs	*,5,8 **,22
Low Period of SCL Clock	t_{LOW}		1.3 4.7			µs	*,8 **,22
High Period of SCL Clock	t_{HIGH}		0.6 4.0			µs	*,8 **,22
Data Hold Time	$t_{HD:DAT}$		0 0		0.9	µs	*,6,7, **,22
Data Setup Time	$t_{SU:DAT}$		100 250			ns	*,8 **,22
Rise Time of Both SDA and SCL Signals	t_R		$20+0.1C_B$	300 1000		ns	*,9 **,22
Fall Time of Both SDA and SCL Signals	t_F		$20+0.1C_B$	300 300		ns	*,9 **,22
Setup Time for STOP Condition	$t_{SU:STO}$		0.6 4.0			µs	*, **,22
Capacitive Load for each Bus Line	C_B			400		pF	9

* fast mode
** standard mode

5-WIRE SERIAL INTERFACE

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=2.7V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Port Select Setup	t_{SETUP}	30			ns	14, 21
$R/\overline{W}$ Setup	t_{SETUP}	30			ns	14, 21
Clock Frequency	f_{CLK}	DC		5	MHz	14, 15
Width of CLK Pulse	t_{CH}	50			ns	14, 15
Data Setup Time	t_{DC}	30			ns	14, 15
Data Hold Time	t_{CDH}	0			ns	14, 15
Progapation Delay Time High to Low Level Clock to Output	t_{DV}			40	ns	14, 15
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	14, 15
$\overline{RST}$ Low from Clock Input High	t_{HLT}	50			ns	14, 15
$\overline{RST}$ Inactive	t_{RLT}	125			ns	14, 15
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	14, 15

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{CC} is switched off.
3. I_{CC} specified with SDA pin open.
4. I_{STBY} specified with for V_{CC} equal 3.0V and 5.0V and control port logic pins are driven to the appropriate logic levels. Appropriate logic levels specify that logic inputs are within a 0.5-volt of ground or V_{CC} for the corresponding inactive state.
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{RMAX} + $t_{SU:DAT}$ = 1000+250=1250 ns before the SCL line is released.
9. C_B - total capacitance of one bus line in picofarads, timing referenced to (0.9)(V_{CC}) and (0.1) (V_{CC}).
10. Typical values are for ta = 25°C and nominal supply voltage.

11. Address Inputs, A0, A1, and A2, should be tied to either V_{CC} or GND depending on the desired address selections.

12. Resistor inputs cannot go below GND by more than 0.5 volts or above V_{CC} by more than 0.5 volts.

13. -3dB cutoff frequency characteristics for the DS1844 depend on potentiometer total resistance: DS1844-010; 1 MHz; DS1844-050; 200 kHz; DS1844-100; 100 kHz.

14. See Figure 3, 5-wire timing diagram.

15. For 5-wire control logic and V_{CC} = 5V ±10%, maximum V_{IL} = +0.8V. For V_{CC} = 3.0V ±10%,V_{IL} = +0.6V.

16. Absolute linearity is used to measure expected wiper voltage versus measured wiper voltage as determined by wiper position. The DS1844 is specified to provide an absolute linearity of ± 0.5 LSB.

17. Relative linearity is used to determine the change in wiper voltage between two adjacent wiper positions. The DS1844 is specified to provide a relative linearity of ± 0.25 dB.

18. When used as a rheostat or variable resistor the temperature coefficient applies: 650 ppm/°C. When used as a voltage divider or potentiometer, the effective temperature coefficient approaches 30 ppm/°C.

19. Maximum ICC active current is dependent on clock rates during serial port activity. Maximum ICC active current is specified for 5 MHz clock rates, and worse case input logic levels.

20. t_{SETUP} is the minimum time required for the port select input, PS, to be stable before any activity on SDA or SCL terminals.

21. t_{SETUP} is the minimum time required for the port select input, PS, and/or the R/$\overline{W}$ input to be stable before $\overline{RST}$ becomes active (or goes to a high state).

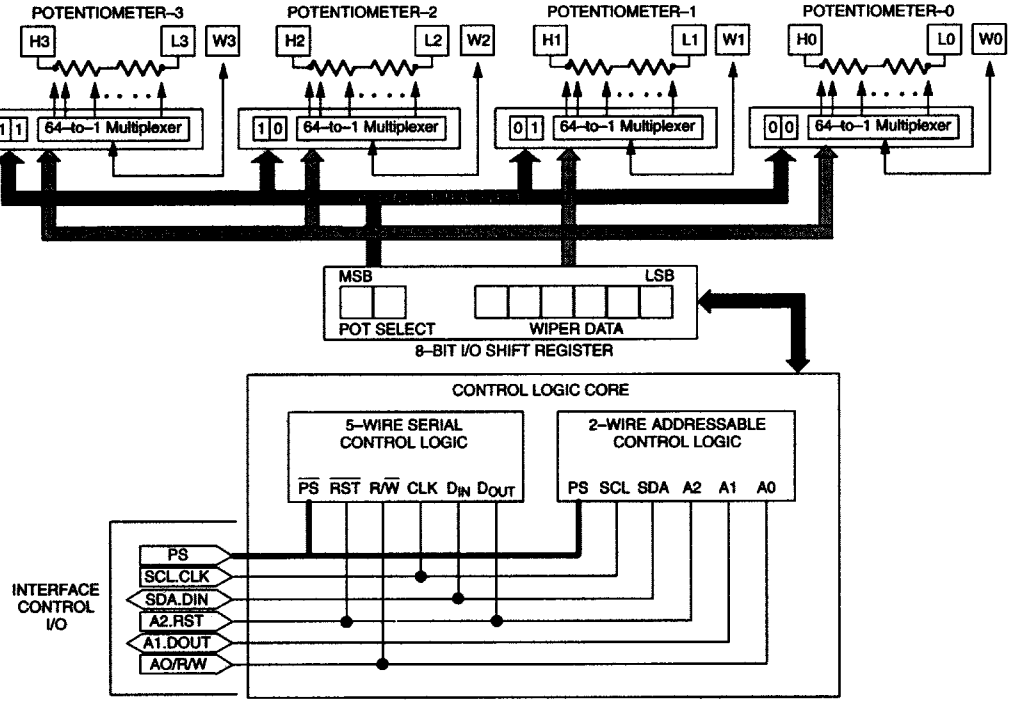
22. See Figure 8, 5-wire timing diagram.

23. Measured with load as shown in Figure 9.

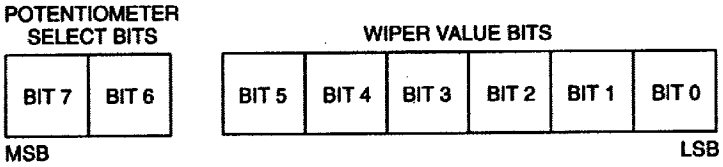
24. Valid for V_{CC} = 5V only.

25. Valid at 25°C only.

DS1844 BLOCK DIAGRAM Figure 1



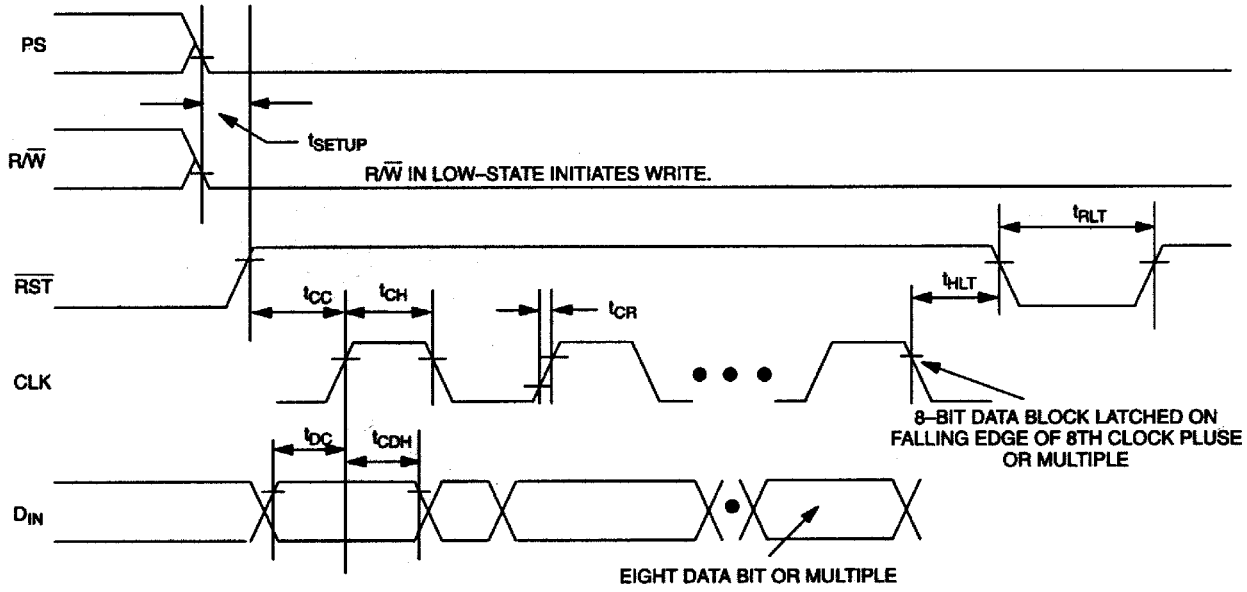
WIPER REGISTER CONFIGURATION Figure 2



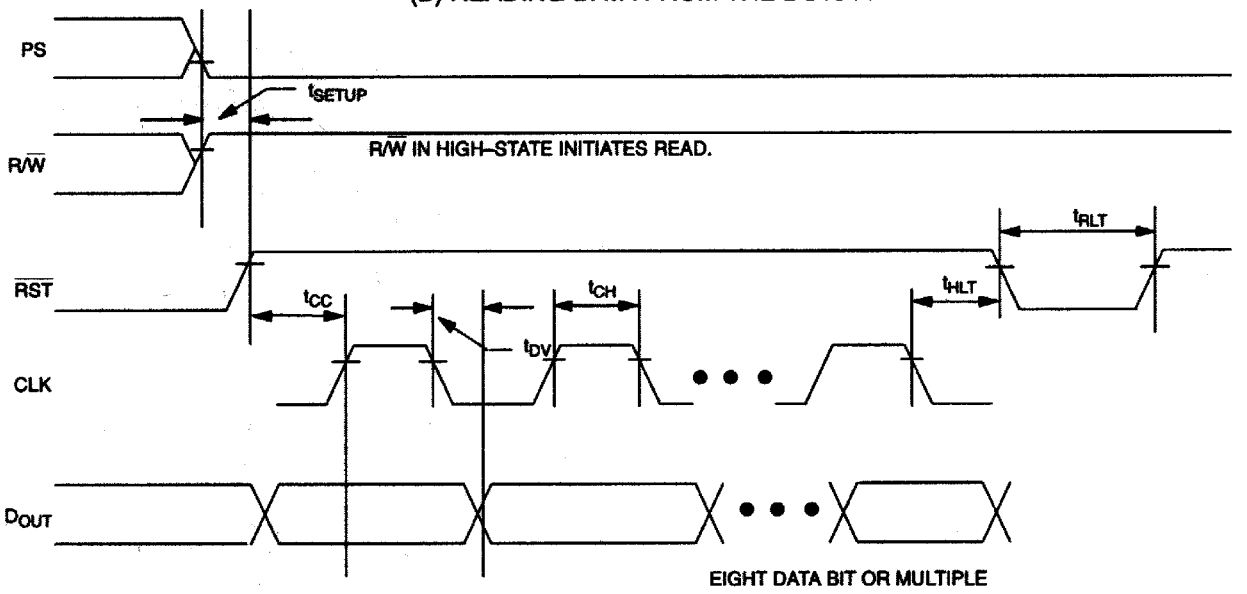
BITS 7, 6
00 – POTENTIOMETER–0 SELECT
01 – POTENTIOMETER–1 SELECT
10 – POTENTIOMETER–2 SELECT
11 – POTENTIOMETER–3 SELECT

5-WIRE SERIAL TIMING DIAGRAM Figure 3 (A), (B)

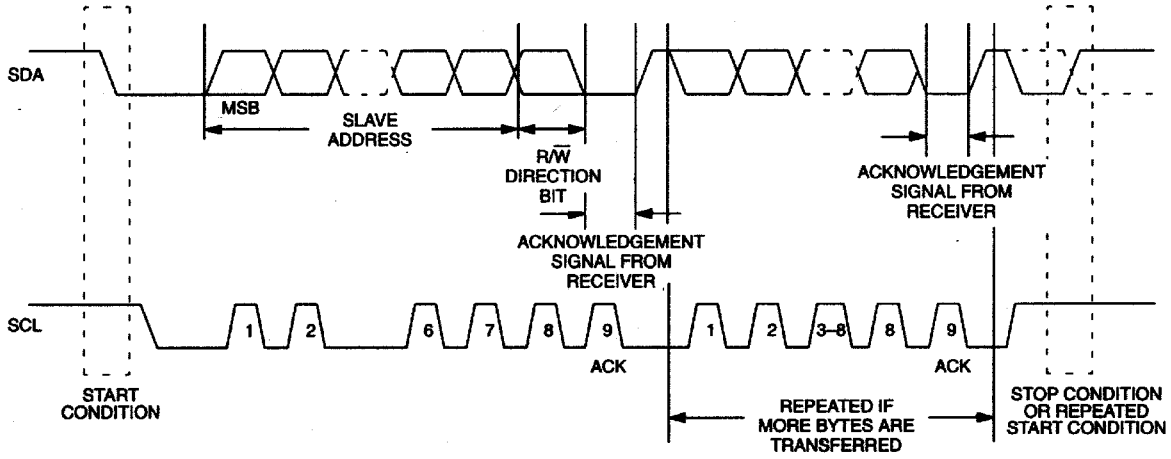
(A) WRITING DATA TO THE DS1844



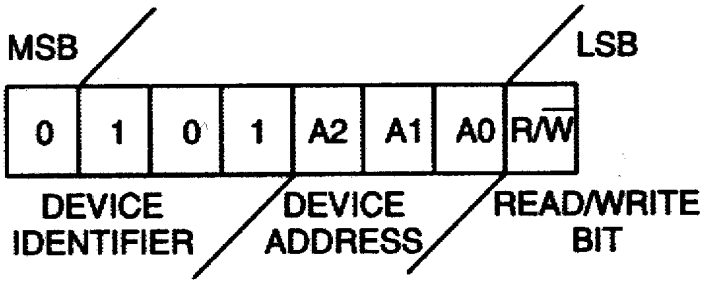
(B) READING DATA FROM THE DS1844



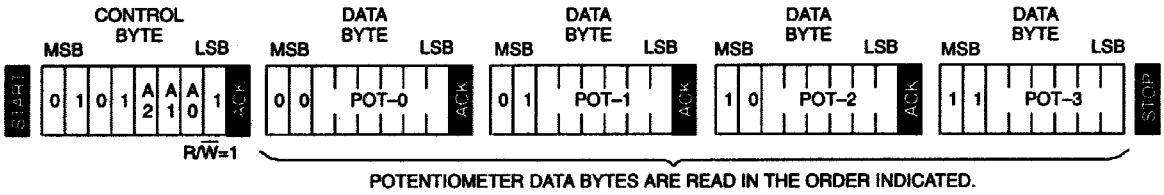
2-WIRE DATA TRANSFER OVERVIEW Figure 4



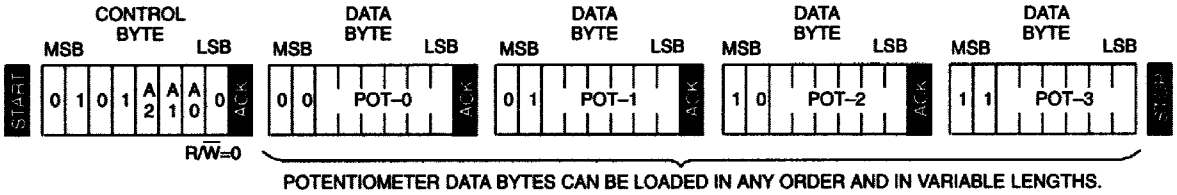
COMMAND/CONTROL BYTE Figure 5



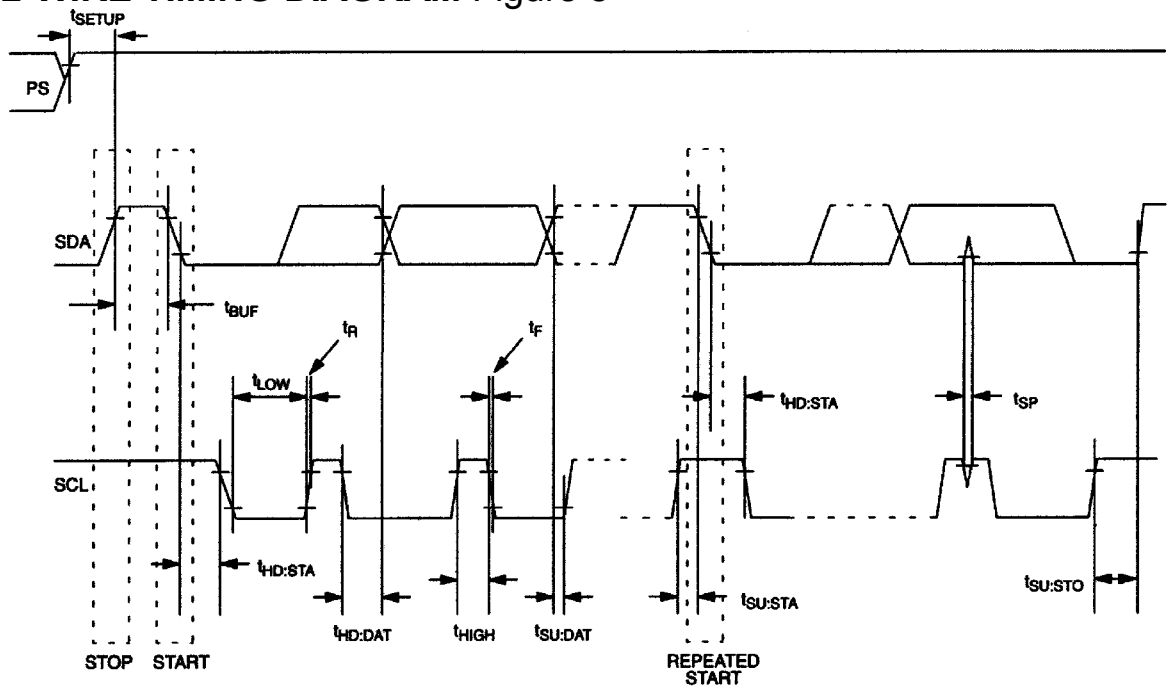
2-WIRE READ PROTOCOL Figure 6



2-WIRE WRITE PROTOCOLS Figure 7



2-WIRE TIMING DIAGRAM Figure 8



DIGITAL OUTPUT LOAD Figure 9