ispGAL™22LV10 Device Datasheet

June 2010

All Devices Discontinued!

Product Change Notification (PCN) #09-10 has been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispGAL22LV10	ispGAL22LV10-4LJ	**Discontinued**	PCN#09-10
	ispGAL22LV10-5LJ		
	ispGAL22LV10-7LJ		
	ispGAL22LV10-10LJ		
	ispGAL22LV10-15LJ		
	ispGAL22LV10-7LJI		
	ispGAL22LV10-10LJI		
	ispGAL22LV10-15LJI		
	ispGAL22LV10-4LK		
	ispGAL22LV10-5LK		
	ispGAL22LV10-7LK		
	ispGAL22LV10-10LK		
	ispGAL22LV10-15LK		
	ispGAL22LV10-7LKI		
	ispGAL22LV10-10LKI		
	ispGAL22LV10-15LKI		

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Internet: http://www.latticesemi.com

ispGAL®22LV10

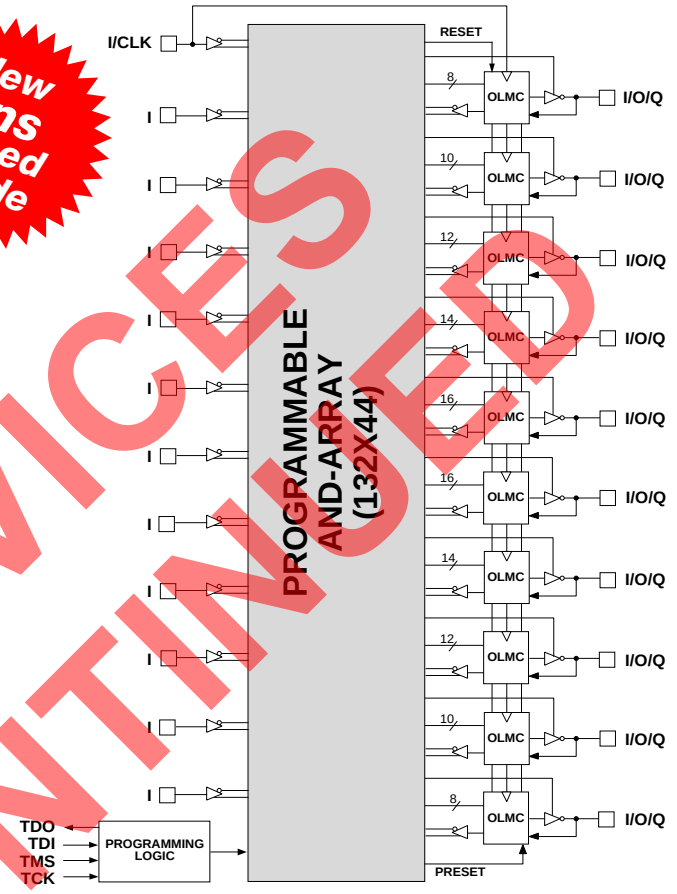
In-System Programmable Low Voltage E²CMOS® PLD Generic Array Logic™

Features

- **IN-SYSTEM PROGRAMMABLE**
  - — IEEE 1149.1 Standard TAP Controller Port Programming
  - — 4-Wire Serial Programming Interface
  - — Minimum 10,000 Program/Erase Cycles
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — 4 ns Maximum Propagation Delay
  - — Fmax = 250 MHz
  - — 3 ns Maximum from Clock Input to Data Output
  - — UltraMOS® Advanced CMOS Technology
- **3.3V LOW VOLTAGE 22V10 ARCHITECTURE**
  - — JEDEC-Compatible 3.3V Interface Standard
  - — 5V Tolerant Inputs and I/O
  - — I/O Interfaces with Standard 5V TTL Devices
- **ACTIVE PULL-UPS ON ALL LOGIC INPUT AND I/O PINS**
- **COMPATIBLE WITH STANDARD 22LV10/22V10 DEVICES**
  - — Function/Fuse-Map Compatible with 22LV10/22V10 Devices
  - — Parametric Compatible with 22LV10
- **E² CELL TECHNOLOGY**
  - — In-System Programmable Logic
  - — 100% Tested/100% Yields
  - — High Speed Electrical Erasure (<100ms)
  - — 20 Year Data Retention
- **APPLICATIONS INCLUDE:**
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Software-Driven Hardware Configuration
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

New 4ns Speed Grade

Functional Block Diagram



Description

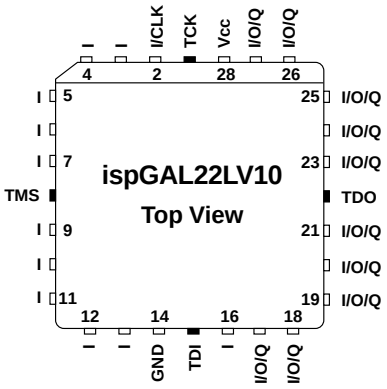
The ispGAL22LV10 is manufactured using Lattice Semiconductor's advanced 3.3V E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology. The ispGAL22LV10 can interface with both 3.3V and 5V signal levels.

The ispGAL22LV10 is fully function/fuse map compatible with the GAL®22LV10 and GAL22V10. Further, the ispGAL22LV10 is parametric compatible with the GAL22LV10. The ispGAL22LV10 also shares the same 28-pin PLCC package pin-out as the GAL22LV10.

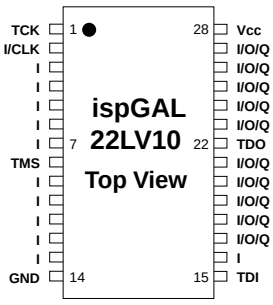
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 10,000 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



SSOP



LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; http://www.latticesemi.com

December 1999

Ordering Information

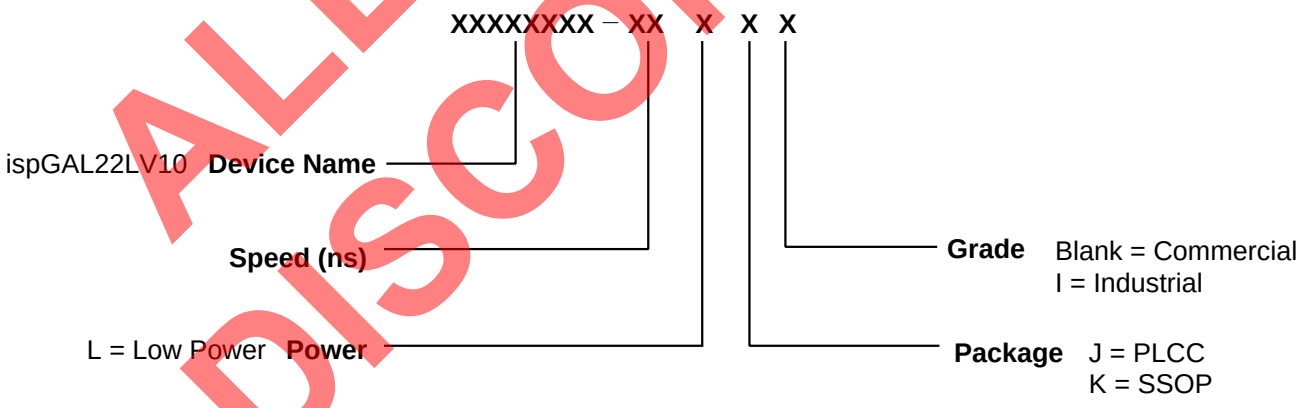
Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	3	3	130	ispGAL22LV10-4LJ	28-Lead PLCC
				ispGAL22LV10-4LK	28-Lead SSOP
5	3.5	3.5	130	ispGAL22LV10-5LJ	28-Lead PLCC
				ispGAL22LV10-5LK	28-Lead SSOP
7.5	5	5	130	ispGAL22LV10-7LJ	28-Lead PLCC
				ispGAL22LV10-7LK	28-Lead SSOP
10	7	6.5	130	ispGAL22LV10-10LJ	28-Lead PLCC
				ispGAL22LV10-10LK	28-Lead SSOP
15	10	8	130	ispGAL22LV10-15LJ	28-Lead PLCC
				ispGAL22LV10-15LK	28-Lead SSOP

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	5	160	ispGAL22LV10-7LJI	28-Lead PLCC
				ispGAL22LV10-7LKI	28-Lead SSOP
10	7	6.5	160	ispGAL22LV10-10LJI	28-Lead PLCC
				ispGAL22LV10-10LKI	28-Lead SSOP
15	10	8	160	ispGAL22LV10-15LJI	28-Lead PLCC
				ispGAL22LV10-15LKI	28-Lead SSOP

Part Number Description



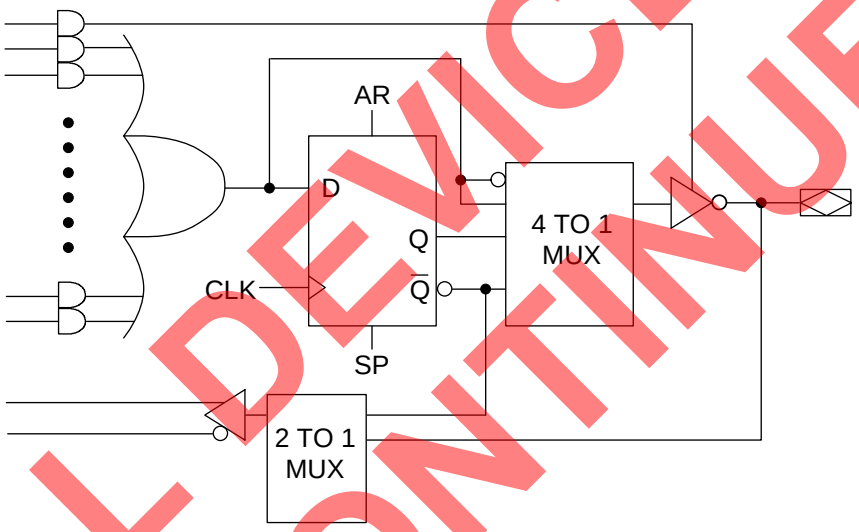
Output Logic Macrocell (OLMC)

The ispGAL22LV10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 17 and 27), two have ten product terms (pins 18 and 26), two have twelve product terms (pins 19 and 25), two have fourteen product terms (pins 20 and 24), and two OLMCs have sixteen product terms (pins 21 and 23). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The ispGAL22LV10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



ispGAL22LV10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the ispGAL22LV10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (S0 and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

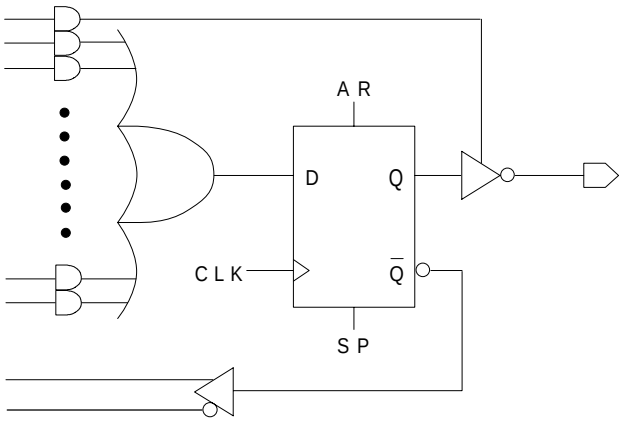
In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

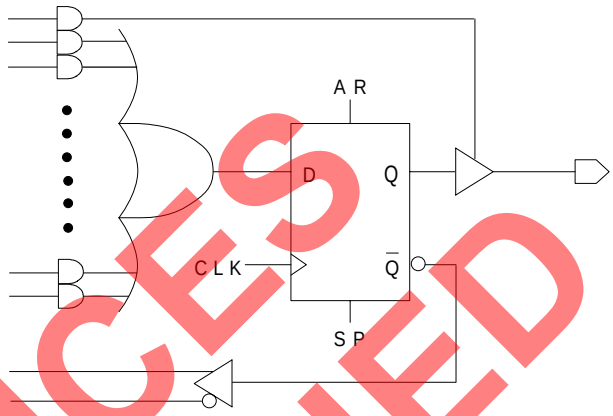
In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Registered Mode



ACTIVE LOW

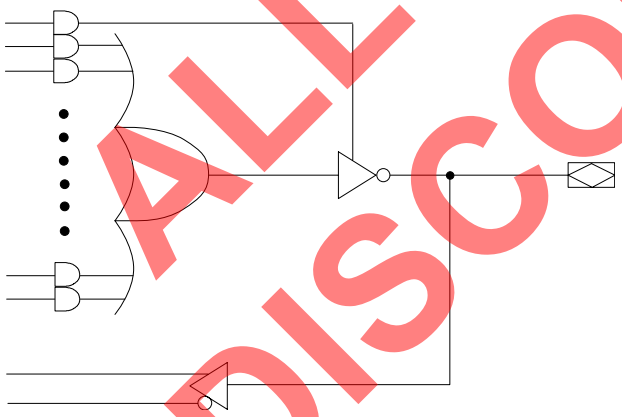
$S_0 = 0$
$S_1 = 0$



ACTIVE HIGH

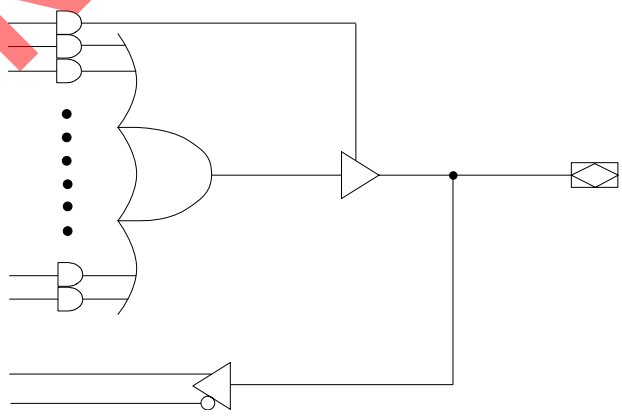
$S_0 = 1$
$S_1 = 0$

Combinatorial Mode



ACTIVE LOW

$S_0 = 0$
$S_1 = 1$

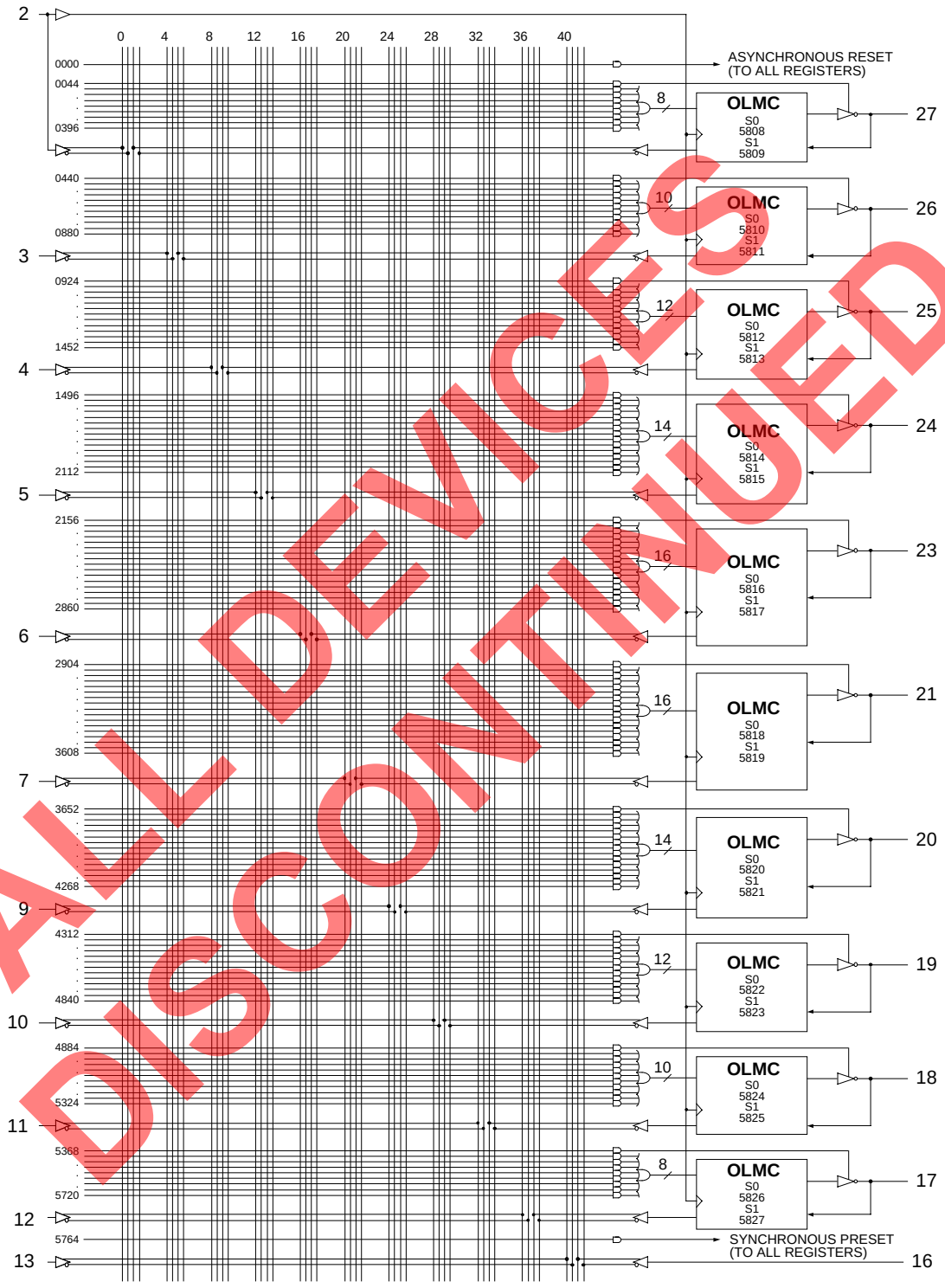


ACTIVE HIGH

$S_0 = 1$
$S_1 = 1$

ispGAL22LV10 Logic Diagram/JEDEC Fuse Map

PLCC & SSOP Package Pinout



5828, 5829 ... Electronic Signature ... 5890, 5891							
Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
MSB							LSB

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... -0.5 to +4.6V
Input and I/O voltage applied ..... -0.5 to +5.6V
Off-state output voltage applied ..... -0.5 to +4.6V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss - 0.3	—	0.8	V
V_{IH}	Input or I/O High Voltage		2.0	—	5.25	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	-150	µA
I_{IH}	Input or I/O High Leakage Current	$(Vcc-0.2)V \le V_{IN} \le V_{CC}$	—	—	10	µA
	Input or I/O High Leakage Current	$Vcc \le V_{IN} \le 5.25V$	—	—	2	mA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.4	V
		I_{OL} = 500µA Vin = V_{IL} or V_{IH}	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100µA Vin = V_{IL} or V_{IH}	Vcc-0.2V	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OL-ISP}	Low Level Output Current TDO		—	—	4	mA
I_{OH}	High Level Output Current		—	—	–8	mA
I_{OH-ISP}	High Level Output Current TDO		—	—	–2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 3.3V V_{OUT} = 0.5V T_A = 25°C	-30	—	-80	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	90	130	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0V V_{IH} = 3.0V Unused Inputs at V_{IL} f_{toggle} = 1MHz Outputs Open	—	90	160	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 3.3V and TA = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM -4 MIN.	COM -4 MAX.	COM -5 MIN.	COM -5 MAX.	COM/IND -7 MIN.	COM/IND -7 MAX.	COM/IND -10 MIN.	COM/IND -10 MAX.	COM/IND -15 MIN.	COM/IND -15 MAX.	UNITS
t_{pd}[2]	A	Input or I/O to Comb. Output	1	4	1	5	1	7.5	1	10	1	15	ns
t_{co}[2]	A	Clock to Output Delay	1	3	1	3.5	1	5	1	6.5	—	8	ns
t_{cf}[3]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk↑	3	—	3.5	—	5	—	7	—	10	—	ns
t_{h}	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	0	—	ns
f_{max}[4]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	143	—	100	—	74	—	55.5	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	182	—	166	—	133	—	105	—	80	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	166	—	111	—	83.3	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	2	—	2.5	—	3	—	4	—	6	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	2	—	2.5	—	3	—	4	—	6	—	ns
t_{en}	B	Input or I/O to Output Enabled	1	5	1	6	1	7.5	1	10	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	1	5	1	6	1	7.5	1	10	—	15	ns
t_{ar}	A	Input or I/O to Asynch. Reset of Reg.	1	4.5	1	5.5	1	9	1	13	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	4.5	—	5.5	—	7	—	8	—	15	—	ns
t_{arr}	—	Asynch. Reset to Clk↑ Recovery Time	3.5	—	4	—	5	—	8	—	10	—	ns
t_{spr}	—	Synch. Preset to Clk↑ Recovery Time	3.5	—	4	—	5	—	10	—	10	—	ns

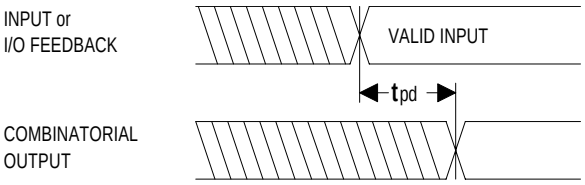
1) Refer to **Switching Test Conditions** section.
2) Minimum values for **t**pd and **t**co are not 100% tested but established by characterization.
3) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
4) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Note: Maximum clock input rise and fall time between 10% to 90% of Vout = 2ns.

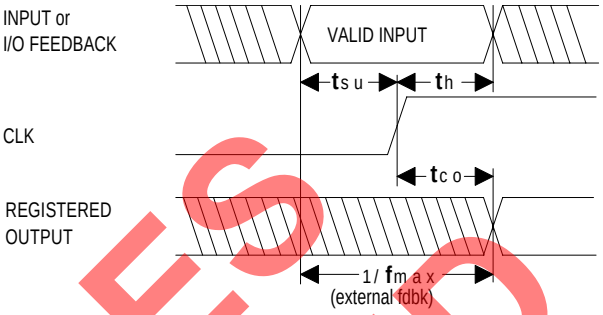
Capacitance (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_I	Input Capacitance	4	pF	V_{CC} = 3.3V, V_I = 0V
$C_{I/O}$	I/O Capacitance	5	pF	V_{CC} = 3.3V, $V_{I/O}$ = 0V

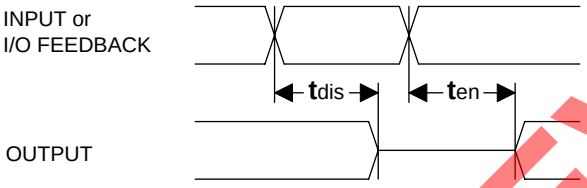
Switching Waveforms



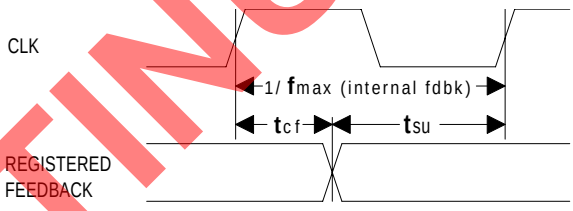
Combinatorial Output



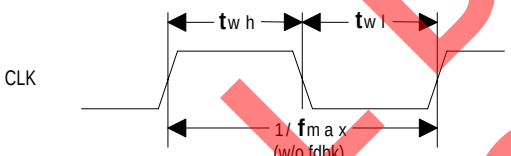
Registered Output



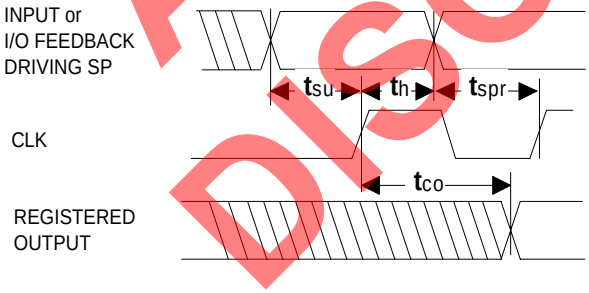
Input or I/O to Output Enable/Disable



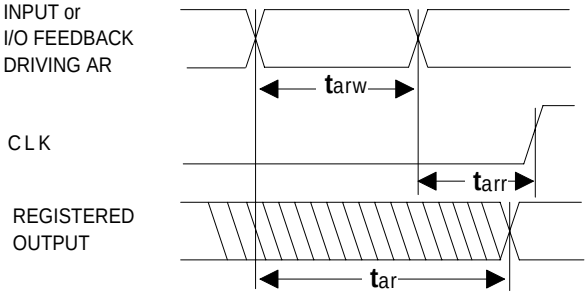
fmax with Feedback



Clock Width

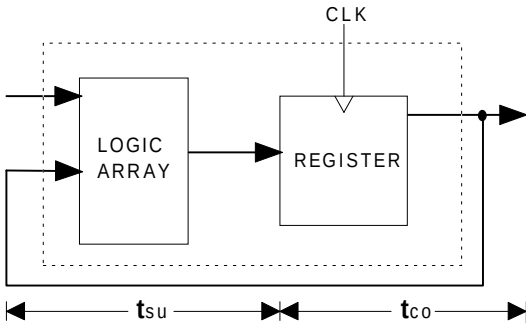


Synchronous Preset



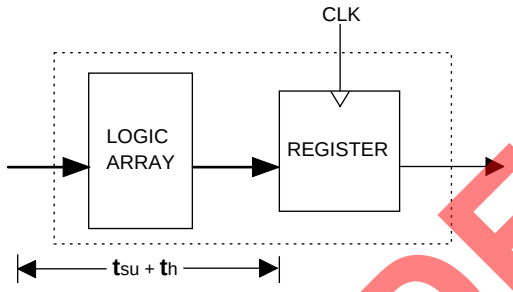
Asynchronous Reset

fmax Descriptions



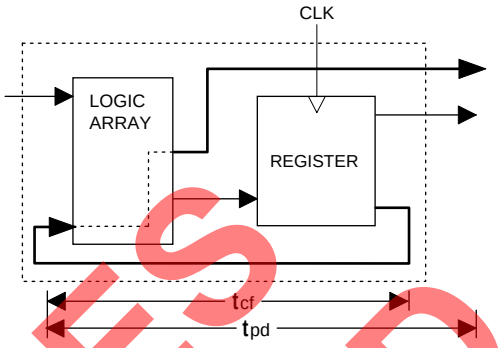
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/twh + twl. This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

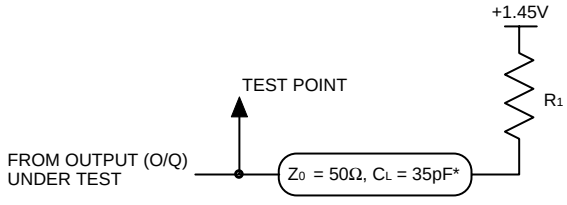
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1.5ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Output Load Conditions (see figure)

Test Condition		R1	CL
A		50Ω	35pF
B	High Z to Active High at 1.9V	50Ω	35pF
	High Z to Active Low at 1.0V	50Ω	35pF
C	Active High to High Z at 1.9V	50Ω	35pF
	Active Low to High Z at 1.0V	50Ω	35pF



*C_L includes test fixture and probe capacitance.

Electronic Signature

An electronic signature (ES) is provided in every ispGAL22LV10 device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice Semiconductor 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically an ispGAL22LV10 and a ispGAL22LV10-UES (UES = User Electronic Signature) or ispGAL22LV10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the ispGAL22LV10 contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the ispGAL22LV10 device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

Security Cell

A security cell is provided in every ispGAL22LV10 device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

ispGAL22LV10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch.

Device Programming

The ispGAL22LV10 device uses a standard 22V10 JEDEC fusemap file to describe the device programming information. Any third party logic compiler can produce the JEDEC file for this device.

In-System Programmability

The ispGAL22LV10 device features In-System Programmable technology. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming. The interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. For details on the operation of the internal state machine and programming of ispGAL22LV10 devices please refer to the ISP Architecture and Programming section in this Data Book.

Output Register Preload

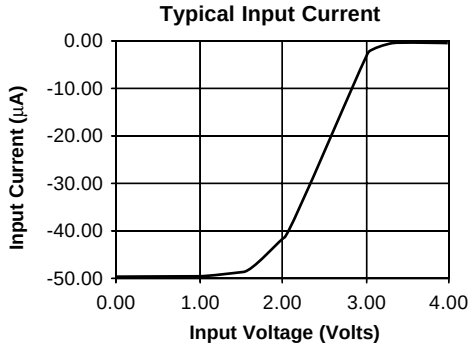
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The ispGAL22LV10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

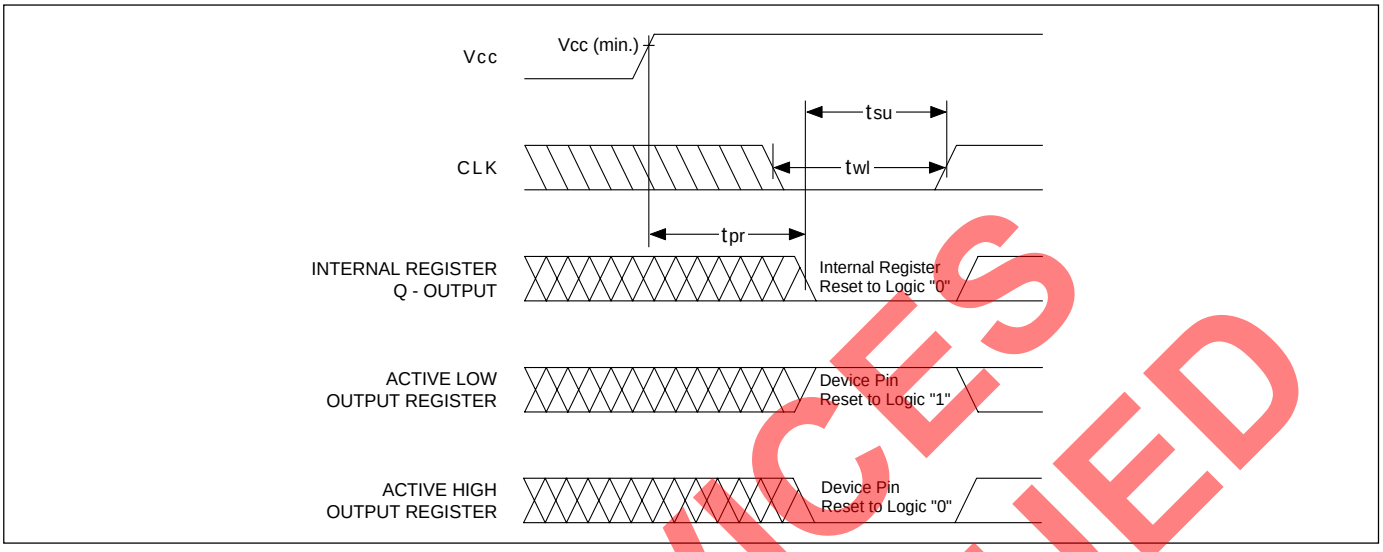
Input Buffers

ispGAL22LV10 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

All input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

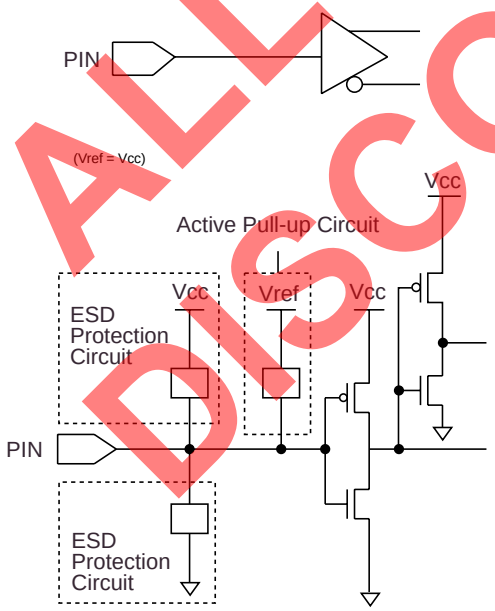


Power-Up Reset

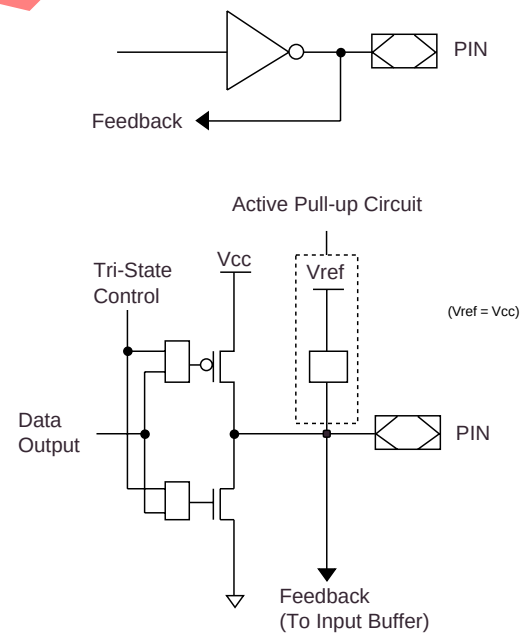


Circuitry within the ispGAL22LV10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the ispGAL22LV10. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



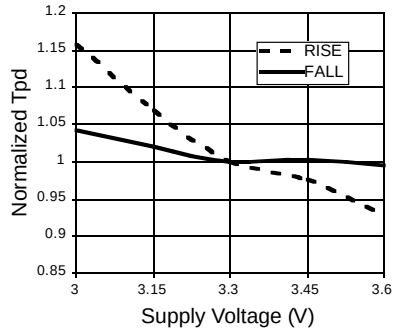
Input



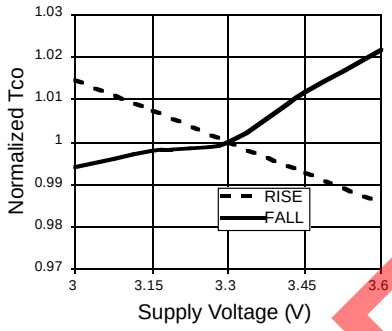
Output

ispGAL22LV10: Typical AC and DC Characteristic Diagrams

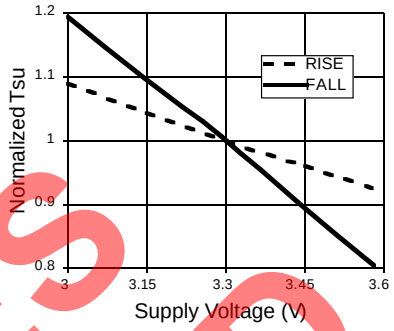
Normalized Tpd vs Vcc



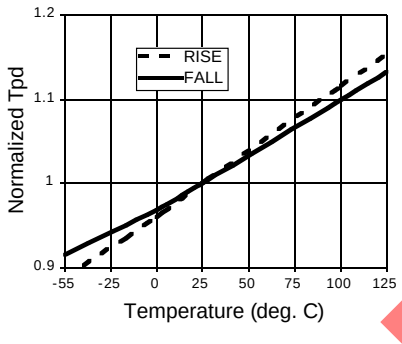
Normalized Tco vs Vcc



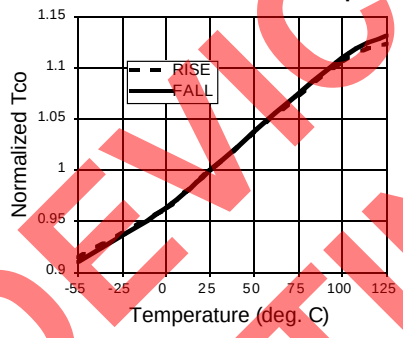
Normalized Tsu vs Vcc



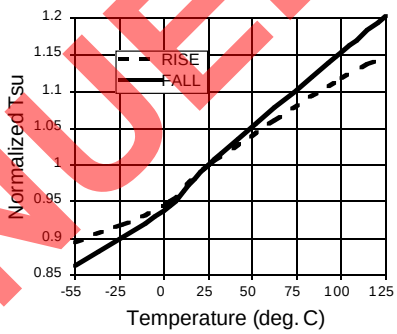
Normalized Tpd vs Temp



Normalized Tco vs Temp

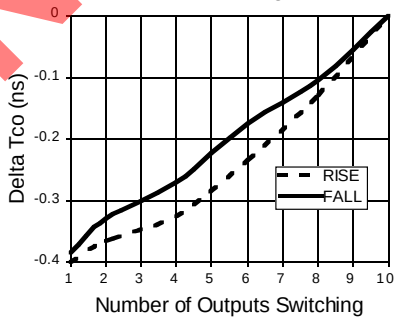


Normalized Tsu vs Temp

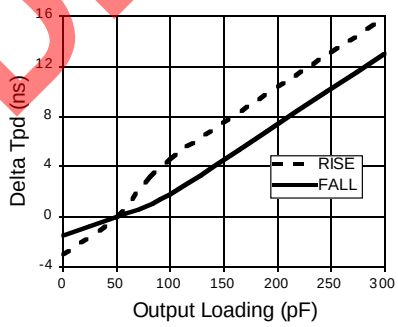


Delta Tpd vs # of Outputs Switching

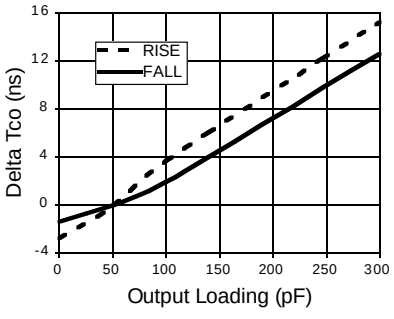
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

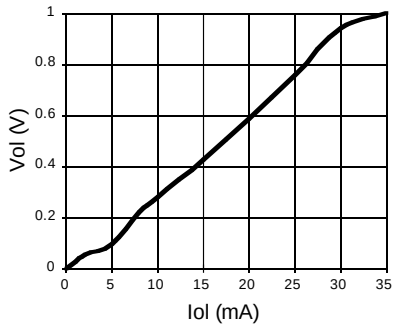


Delta Tco vs Output Loading

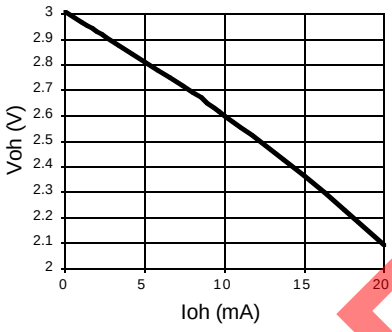


ispGAL22LV10: Typical AC and DC Characteristic Diagrams

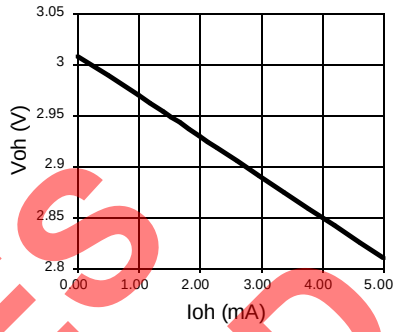
Vol vs Iol



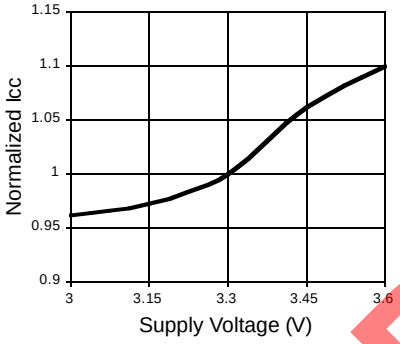
Voh vs Ioh



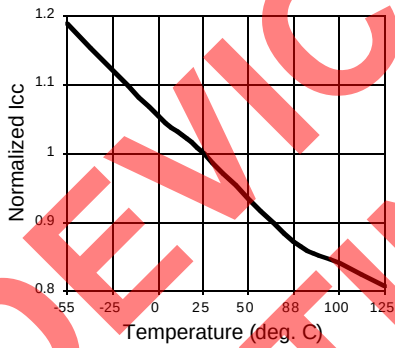
Voh vs Ioh



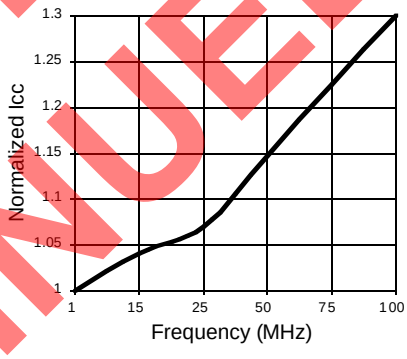
Normalized Icc vs Vcc



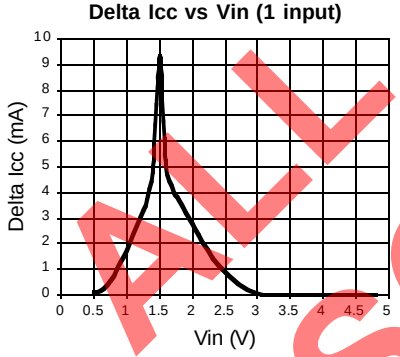
Normalized Icc vs Temp



Normalized Icc vs Freq



Delta Icc vs Vin (1 input)



Input Clamp (Vik vs Iik)