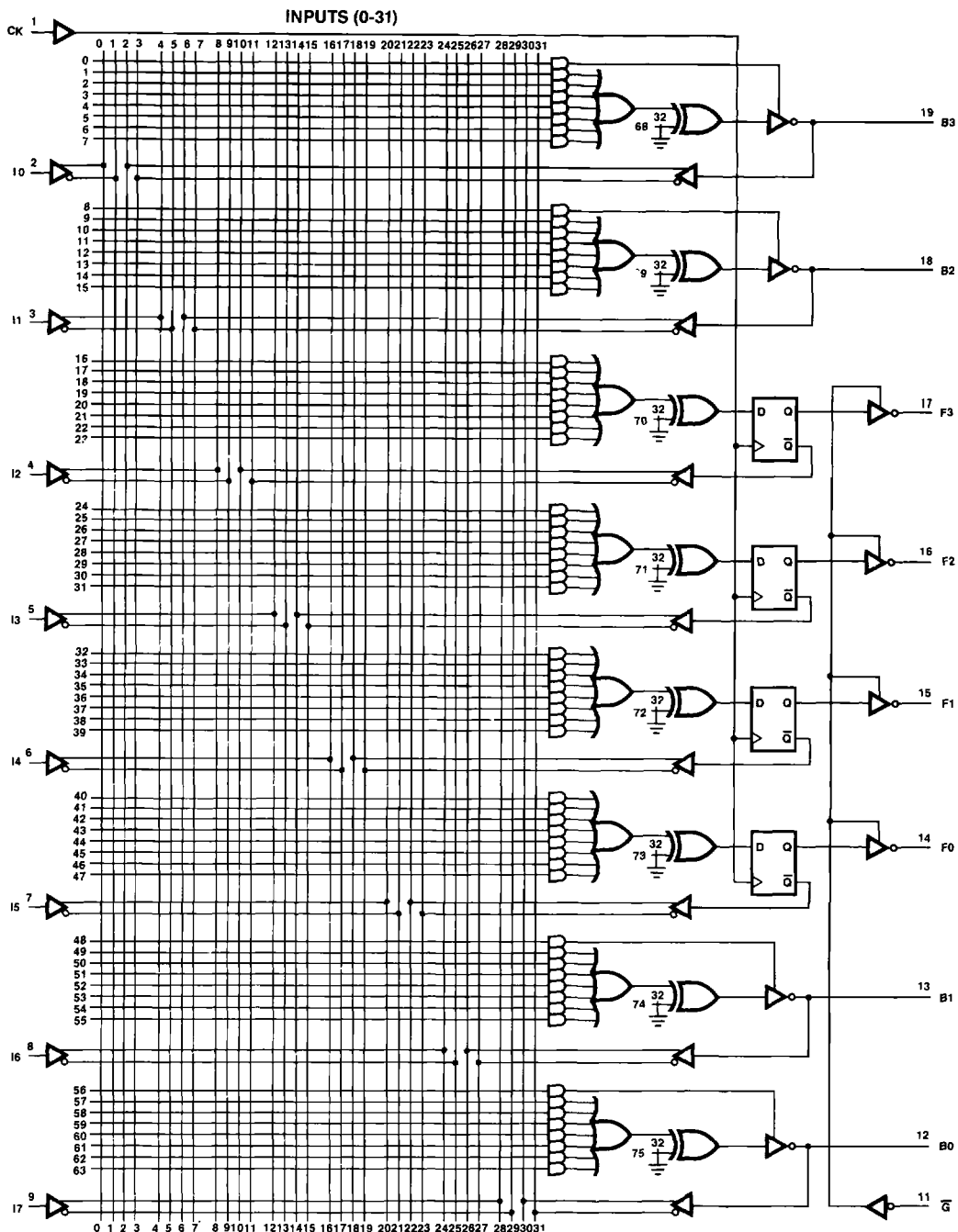


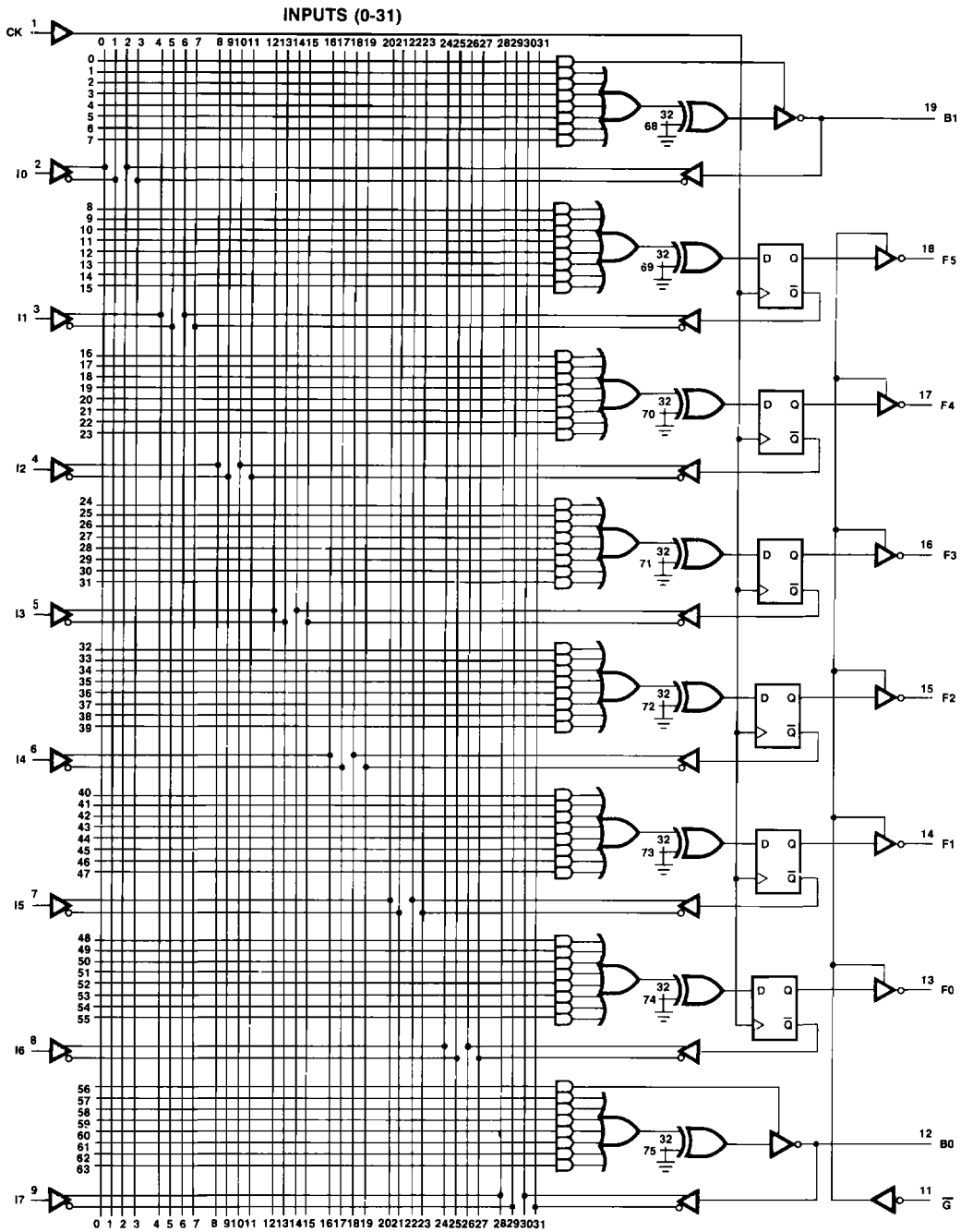
HPL-16RC4

Functional Diagram



HPL-16RC6

Functional Diagram

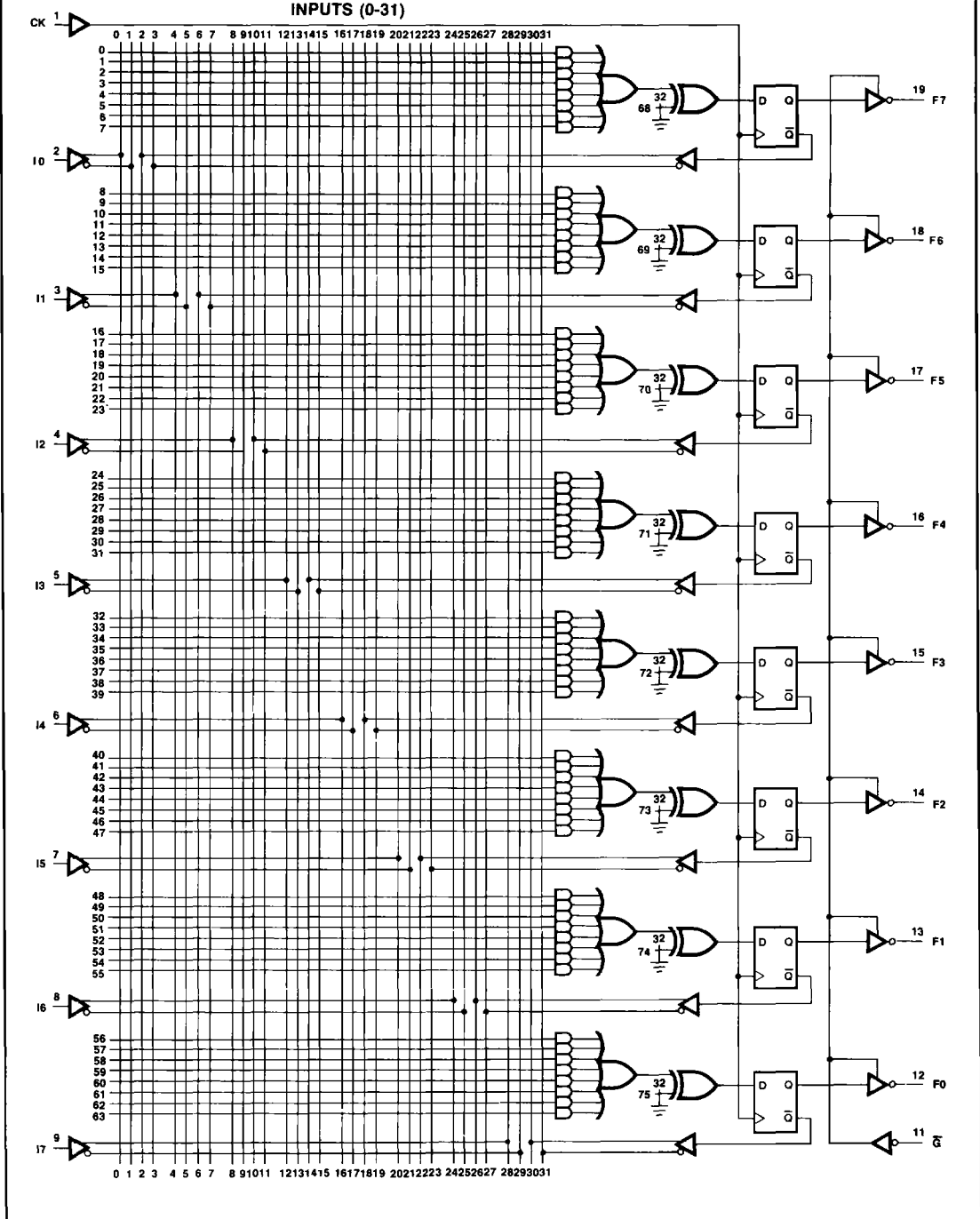


HPL-16RC8/6/4

7
CMOS
HPL

HPL-16RC8

Functional Diagram



Specifications HPL-16RC8, 6, 4

HPL-16RC8/6/4

Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage | +7.0 Volts |
| Input, Output or I/O Voltage Applied | GND -0.3V to VCC +0.3V |
| Storage Temperature Range | -65°C to +150°C |
| Maximum Package Power Dissipation | 1 Watt |
| θ_{jc} | 16°C/W (CERDIP Package), 19°C/W (LCC Package) |
| θ_{ja} | 70°C/W (CERDIP Package), 76°C/W (LCC Package) |
| Gate Count | 1500 Gates |
| Junction Temperature | +150°C |
| Lead Temperature (Soldering, Ten Seconds) | +275°C |

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

| | |
|-------------------------------|-----------------|
| Operating Voltage Range | +4.5V to +5.5V |
| Operating Temperature Range | |
| HPL-16RC8,6,4-5 | 0°C to +70°C |
| HPL-16RC8,6,4-9 | -40°C to +85°C |
| HPL-16RC8,6,4-8 | -55°C to +125°C |

D.C. Electrical Specifications

(Operating)

| | |
|-----------------|--|
| HPL-16RC8,6,4-5 | (VCC = 5.0V ± 10%, TA = 0°C to +75°C) |
| HPL-16RC8,6,4-9 | (VCC = 5.0V ± 10%, TA = -40°C to +85°C) |
| HPL-16RC8,6,4-8 | (VCC = 5.0V ± 10%, TA = -55°C to +125°C) |

| SYMBOL | PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS ① |
|------------------|--------------------------------|-----|---------|--------|---|
| I _{IH} | Dedicated Input Current | "1" | +1 | μA | V _{IH} = VCC MAX |
| I _{IL} | Input Current | "0" | -1 | μA | V _{IL} = 0V VCC = VCC MAX |
| IF _{ZH} | Output Current | "1" | +10 | μA | V _{FH} = VCC MAX |
| IF _{ZL} | Hi-Z State | "0" | -10 | μA | V _{FL} = 0V VCC = VCC MAX |
| IB _{ZH} | Bidirectional Hi-Z Current | "1" | +10 | μA | V _{BH} = VCC MAX |
| IB _{ZL} | | "0" | -10 | μA | V _{BL} = 0V VCC = VCC MAX |
| V _{IH} | Input Threshold Voltage ② | "1" | 2.0 | V | VCC = VCC MAX |
| V _{IL} | | "0" | 0.8 | V | VCC = VCC MIN |
| VO _{H1} | Output Voltage ② | "1" | 3.0 | V | I _{OH1} = -5.0 mA |
| VO _{H2} | | "1" | VCC-0.4 | V | I _{OH2} = -1.0 mA VCC MIN, V _{IL} MAX, V _{IH} MIN |
| V _{OL} | Output Voltage | "0" | 0.4 | V | I _{OL} = +5.0 mA |
| ICCSB | Standby Power Supply Current | | 150 | μA | V _I = VCC or GND I _F = 0μA, VCC = VCC MAX |
| ICCP | Operating Power Supply Current | | 7 | mA/MHz | V _I = VCC or GND I _F = 0μA, VCC = VCC MAX |

- ① These specifications apply to both Input (I) and Bidirectional (B) Pins.
- ② These specifications apply to both Output (F) and Bidirectional (B) Pins.
- ③ All DC parameters tested under worst case conditions.

Capacitance TA = +25°C

| SYMBOL | PARAMETER | MAX | UNITS | TEST CONDITIONS |
|--------|---------------------------|-----|-------|--|
| CI | Input Capacitance | 5 | pF | V _I = VCC or GND, f = 1 MHz |
| CF | Output Capacitance | 10 | pF | V _F = VCC or GND, f = 1MHz |
| CB | Bidirectional Capacitance | 12 | pF | V _B = VCC or GND, f = 1 MHz |

*NOTE: Sampled and guaranteed — but not 100% tested

7

CMOS HPL

Specifications HPL-16RC8, 6, 4

A.C. Switching Specifications ① (Operating)

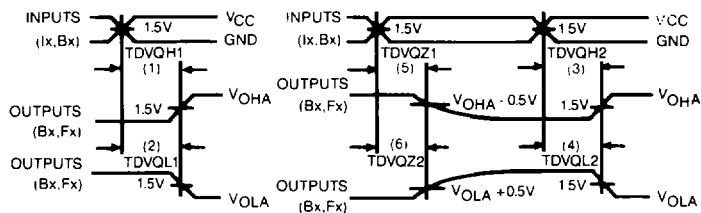
HPL-16RC8,6,4-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
 HPL-16RC8,6,4-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
 HPL-16RC8,6,4-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

| SYMBOL | | | HPL-16RC8,6,4-5 | | HPL-16RC8,6,4-9 | | HPL-16RC8,6,4-8 | | |
|-----------------|------------|---|-----------------|-----|-----------------|-----|-----------------|-----|-------|
| JEDEC STANDARD | OLD SYMBOL | PARAMETER | MIN | MAX | MIN | MAX | MIN | MAX | UNITS |
| (1) TDVQH1 | TPD | Propagation delay Input or I/O to Active High Output | - | 125 | - | 125 | - | 125 | ns |
| (2) TDVQL1 | TPD | Propagation delay Input or I/O to Active Low Output | - | 125 | - | 125 | - | 125 | ns |
| (3) TDVQH2 ① | TPZX | Enable Access Time to Active High Output - Product Term Controlled | TDVQZ1 | 125 | TDVQZ1 | 125 | TDVQZ1 | 125 | ns |
| (4) TDVQL2 ① | TPZX | Enable Access Time to Active Low Output-Product Term Controlled | TDVQZ2 | 125 | TDVQZ2 | 125 | TDVQZ2 | 125 | ns |
| (5) TDVQZ1 | TPXZ | Disable Access Time from Active High Output-Product Term Controlled | - | 125 | - | 125 | - | 125 | ns |
| (6) TDVQZ2 | TPXZ | Disable Access Time from Active Low Output-Product Term Controlled | - | 125 | - | 125 | - | 125 | ns |
| (7) TCHQH | TCLK | Propagation delay Clock to Active High | - | 60 | - | 60 | - | 60 | ns |
| (8) TCHQL | TCLK | Propagation delay Clock to Active Low | - | 60 | - | 60 | - | 60 | ns |
| (9) TGLQH ① | TPZX | Enable Access Time to Active High Output - Enable Pin Controlled | TGHQZ1 | 60 | TGHQZ1 | 60 | TGHQZ1 | 60 | ns |
| (10) TGLQL ① | TPZX | Enable Access Time to Active Low Output - Enable Pin Controlled | TGHQZ2 | 60 | TGHQZ2 | 60 | TGHQZ2 | 60 | ns |
| (11) TGHQZ1 | TPXZ | Disable Access Time from Active High Output - Enable Pin Controlled | - | 60 | - | 60 | - | 60 | ns |
| (12) TGHQZ2 | TPXZ | Disable Access Time from Active Low Output - Enable Pin Controlled | - | 60 | - | 60 | - | 60 | ns |
| (13) TDVCH | TSU | Data Setup Time | 125 | - | 125 | - | 125 | - | ns |
| (14) TCHDX | TH | Data Hold Time | 0 | - | 0 | - | 0 | - | ns |
| (15) TCHCL | TW | Clock Pulse Width (High) | 25 | - | 25 | - | 25 | - | ns |
| (16) TCLCH | TW | Clock Pulse Width (Low) | 25 | - | 25 | - | 25 | - | ns |
| (17) fMAX | fMAX | Maximum Frequency | - | 5 | - | 5 | - | 5 | MHz |

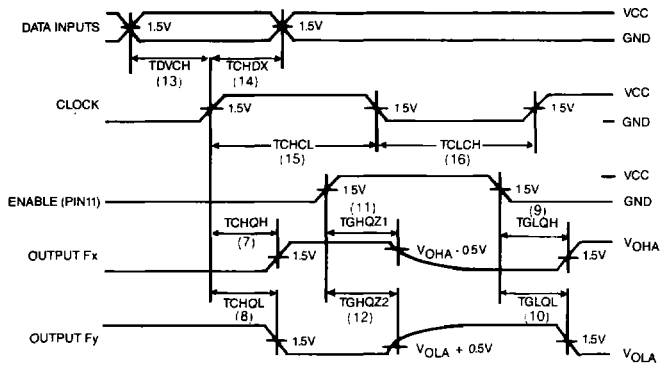
① Enable access time is guaranteed to be greater than disable access time to avoid device contention.

Switching Time Definitions

Asynchronous Outputs



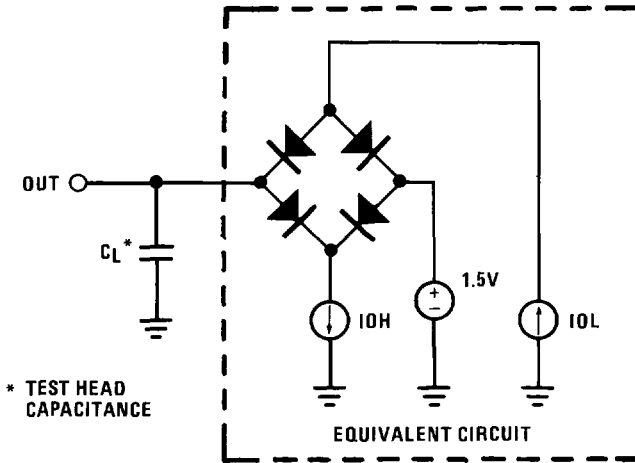
Synchronous Outputs



INPUT CONDITIONS: $t_r, t_f = 5\text{ns}$ (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term or the output enable pin drives the output inactive. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from VOHA or VOLA, the active output level.

A.C. Test Load



* TEST HEAD CAPACITANCE

HPL-16RC8, 6, 4

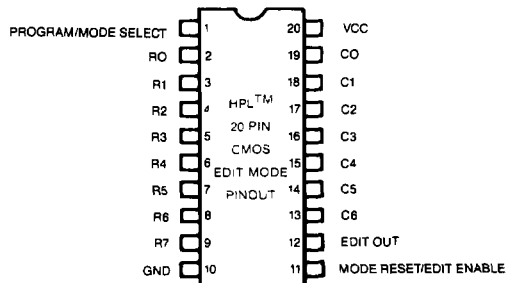
Programming

Following is the programming procedure used for the HPL-16RC8,6,4 programmable logic devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

**TABLE 1
PROGRAMMING SPECIFICATIONS**

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNITS |
|--------|-----------------------------------|--------------------|----------|-------|-------|--------|
| | | | MIN | TYP | MAX | |
| VCCP | VCC Voltage During Programming | | 11.50 | 12.00 | 12.00 | V |
| VCCV | VCC Voltage During Verify | | 4.75 | 5.00 | 5.25 | V |
| ICCP | IC Limit During Programming | | | 100 | 200 | mA |
| VNEG | Edit Enable & Mode Select Voltage | | -5.00 | -5.00 | -7.00 | V |
| INEG | Edit Enable & Mode Select Current | | | | -5.00 | mA |
| VIL | Input Voltage Low | Verify Programming | 0.00 | 0.00 | 0.80 | V |
| VIHV | Input Voltage High | | ① VCCV-2 | VCCV | VCCV | V |
| VIHP | Input Voltage High | | ② VCCP-2 | VCCP | VCCP | V |
| IILP | Input Current Low | VIL = 0.0V | | 0 | 1 | μA |
| IHHV | Input Current High | Verify Programming | | 0 | 0 | μA |
| IHPH | Input Current High | | | | 0 | 1 |
| VSI | Verify voltage | Intact Fuse | 3.00 | 3.30 | | V |
| VSP | Verify voltage | Programmed Fuse | | 0.00 | 0.50 | V |
| TV | Verify Pulse Delay | | 500 | 750 | 1000 | μsec |
| PWP | Programming Width | | 4.5 | 5.0 | 5.5 | msec |
| td | Pulse Seq. Delay | | 1 | 1 | 10 | μsec |
| tr1 | Signal Rise Time | 10% to 90% | 0.01 | 0.1 | | μsec |
| tr2 | VCC Rise Time | 10% to 90% | 0.01 | 0.1 | 5 | μsec |
| tf1 | Signal Fall Time | 90% to 10% | 0.01 | 0.1 | 1 | μsec |
| tf2 | VCC Fall Time | 90% to 10% | 0.01 | 0.1 | 5 | μsec |
| INEG | Mode Select Width | | 1 | 1 | 5 | μsec |
| TPP | Programming Period | | | 5.1 | | msec |
| FL | Fuse Attempts/Link | | 1 | 1 | 2 | cycles |

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC PIN.



**FIGURE 1
EDIT MODE PINOUT
HPL-16RC8, 6, 4**

- NOTES: *
- * While programming the CMOS HPL™ device, no pins should be left floating. EDIT OUT appears as an open drain output during programming. It should be tied to GND through a 1M-ohm resistor.
 - * CMOS HPL outputs are not put into a high impedance state (suitable for row and column address application) until the device is reset and put into the edit mode. For this reason it is recommended that the outputs be left floating until the edit mode is enabled or that the outputs be driven thru a 2k-ohm resistor.
 - * It is suggested that a 0.01μF capacitor be put between VCC and GND to minimize VCC voltage spikes. Also, particular care should be exercised in regard to transients on the MODE SELECT and MODE RESET pins, which could place the device in the incorrect mode.

Programming Procedure

① Set-Up:

- NOTE: Refer to the Figure 1 for the pin definitions, Table 1 for the timing and level definitions, Table 2 for the mode decode, and Tables 3 & 4 for the address decoding.
- During programming, no pins should be left floating.
 - EDIT OUT (Pin 12) should be terminated with a 1 Mohm ($\pm 1\%$) resistor to GND and stray capacitances on this pin should be ≤ 50 pF.
 - Set GND to 0.00 volts.
 - Outputs are only in a high impedance state (and available for addressing of edit mode rows and columns) while in Edit Modes 1 thru 4. Do not apply signals to these pins until a valid Edit Mode is entered.
 - All input and bi-directional pins should be at zero volts nominal with a maximum of 0.3 volts applied.
 - Apply VCCV to the part. No input should ever exceed the level on the VCC PIN.

② Mode Reset/Edit Enable:

- Wait t_d and reset the edit control logic by pulsing the MODE RESET PIN to VNEG.
- Wait t_d and enable Edit mode by applying VNEG to the EDIT ENABLE PIN.

③ Mode Select:

- Wait t_d and select EDIT MODE 1 by pulsing the MODE SELECT PIN to VNEG. Subsequent pulses will increment the mode to 2, 3 and 4 sequentially (sequencing the device beyond mode 4 will result in unpredictable results -- if in doubt, return to STEP 2).
- Verify entry into the proper mode by addressing column 64 and the row indicated in Table 2, waiting T_V and monitoring the EDIT OUT PIN for the proper data.
- Address column 65 and the row indicated in Table 2, wait T_V and monitor the EDIT OUT PIN for the proper data. If both steps 3b and 3c are correct, then the proper mode has been selected.
- To re-enter a mode lower than the current mode, return to step 2. Mode 1 can only be (re-)entered from step 2.

④ Fuse select:

NOTE: The voltage for a logical "1" (VIHP) must not exceed VCCP and must track VCCP as it rises from VCCV in step 5.

- wait t_d and select a row by applying the appropriate address from Table 3.
- Select a column by applying the appropriate address from Table 4.

⑤ Verify Intact Fuse:

NOTE: Skip this step for post-programming verify.

- Wait T_V and monitor EDIT OUT (Pin 12) for VSI.
- If EDIT OUT has indicated less than VSI, the fuse is not intact. Reject this device for a non-blank matrix.

⑥ Program the Fuse:

NOTE: The PROTECT and POLARITY fuses can be accessed from either mode 1 or mode 3 by applying the addresses indicated in Tables 3 & 4.

THE 'PROTECT' FUSE SHOULD NOT BE PROGRAMMED UNTIL ALL OTHER FUSES HAVE BEEN PROGRAMMED AND VERIFIED AS PROGRAMMING THIS FUSE DEFEATS ALL FURTHER VERIFICATION!!

- Wait t_d and raise the VCC PIN to VCCP (allow VIHP to track this rise).
- Wait t_d and pulse the PROGRAM PIN (Pin 1) to VIHP for a duration of PWP.
- Wait t_d and lower the VCC PIN to VCCV (allow VIHP to track this fall)

⑦ Verify Fuse:

- Wait T_V and monitor EDIT OUT for VSP (or VSI if verifying an intact fuse).
- If EDIT OUT has indicated greater than VSP for an attempted programmed fuse, repeat step 6 so that the fuse receives a maximum of FL fusing attempts.

④ Repeat steps 4 through 7 for all addresses in a given mode.....

③ Repeat steps 3 through 8 for all modes.

Programming Waveforms

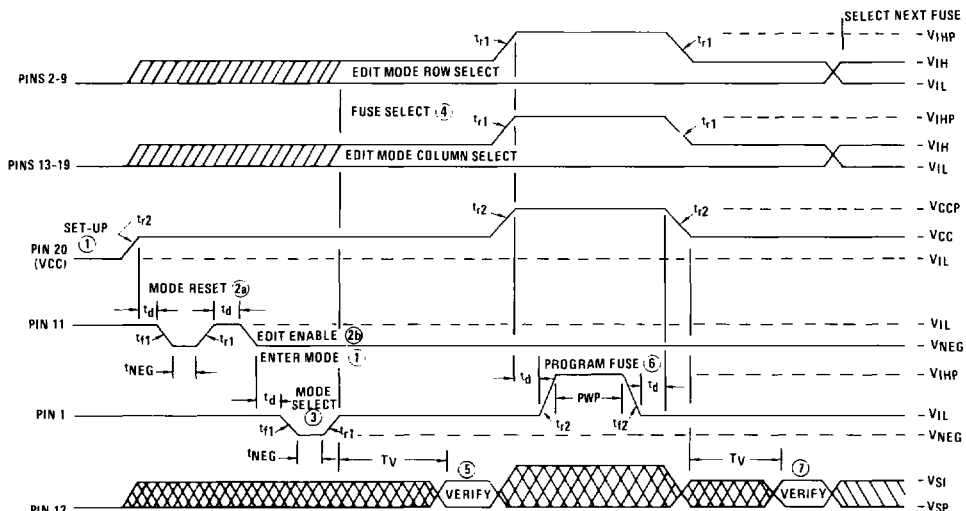


FIGURE 2

NOTE: PINS 13-19 are not necessarily three states and available for application of column address input signals until a valid edit mode is entered. Refer to the edit mode pinout (Figure 1 for further details.

HPL-16RC8, 6, 4

MODE VERIFICATION TABLE 2

| MODE | COLUMN NUMBER | ROW NUMBER | EDIT OUT (PIN 12) LOGICAL LEVEL |
|------|---------------|------------|---------------------------------|
| 1 | 84 | 0 | 0 |
| | 85 | 0 | 0 |
| 2 | 84 | 1 | 0 |
| | 85 | 1 | 1 |
| 3 | 84 | 2 | 1 |
| | 85 | 2 | 0 |
| 4 | 84 | 3 | 1 |
| | 85 | 3 | 1 |

NOTE: *At least two addresses must be checked to verify the proper edit mode.
 *The conversion from the decimal column and row addresses in the table above to the actual pin levels can be made in Tables 3 and 4.

EDIT MODE COLUMN SELECT TABLE 4

| COLUMN NUMBER | C8 | C5 | C4 | C3 | C2 | C1 | C0 | |
|---------------|--------|--------|--------|--------|--------|--------|--------|---------|
| | Pin 13 | Pin 14 | Pin 15 | Pin 16 | Pin 17 | Pin 18 | Pin 19 | |
| 0 | L | L | L | L | L | L | L | |
| 1 | L | L | L | L | L | H | L | |
| 2 | L | L | L | L | L | H | L | |
| 3 | L | L | L | L | L | H | L | |
| 4 | L | L | L | L | L | H | L | |
| 5 | L | L | L | L | L | H | L | |
| 6 | L | L | L | L | L | H | L | |
| 7 | L | L | L | L | L | H | L | |
| 8 | L | L | L | L | L | H | L | |
| 9 | L | L | L | L | L | H | L | |
| 10 | L | L | L | L | L | H | L | |
| 11 | L | L | L | L | L | H | L | |
| 12 | L | L | L | L | L | H | L | |
| 13 | L | L | L | L | L | H | L | |
| 14 | L | L | L | L | L | H | L | |
| 15 | L | L | L | L | L | H | L | |
| 16 | L | L | L | L | L | H | L | |
| 17 | L | L | L | L | L | H | L | |
| 18 | L | L | L | L | L | H | L | |
| 19 | L | L | L | L | L | H | L | |
| 20 | L | L | L | L | L | H | L | |
| 21 | L | L | L | L | L | H | L | |
| 22 | L | L | L | L | L | H | L | |
| 23 | L | L | L | L | L | H | L | |
| 24 | L | L | L | L | L | H | L | |
| 25 | L | L | L | L | L | H | L | |
| 26 | L | L | L | L | L | H | L | |
| 27 | L | L | L | L | L | H | L | |
| 28 | L | L | L | L | L | H | L | |
| 29 | L | L | L | L | L | H | L | |
| 30 | L | L | L | L | L | H | L | |
| 31 | L | L | L | L | L | H | L | |
| 32 | L | L | L | L | L | H | L | |
| 33 | L | L | L | L | L | H | L | |
| 34 | L | L | L | L | L | H | L | |
| 35 | L | L | L | L | L | H | L | |
| 36 | L | L | L | L | L | H | L | |
| 37 | L | L | L | L | L | H | L | |
| 38 | L | L | L | L | L | H | L | |
| 39 | L | L | L | L | L | H | L | |
| 40 | L | L | L | L | L | H | L | |
| 41 | L | L | L | L | L | H | L | |
| 42 | L | L | L | L | L | H | L | |
| 43 | L | L | L | L | L | H | L | |
| 44 | L | L | L | L | L | H | L | |
| 45 | L | L | L | L | L | H | L | |
| 46 | L | L | L | L | L | H | L | |
| 47 | L | L | L | L | L | H | L | |
| 48 | L | L | L | L | L | H | L | |
| 49 | L | L | L | L | L | H | L | |
| 50 | L | L | L | L | L | H | L | |
| 51 | L | L | L | L | L | H | L | |
| 52 | L | L | L | L | L | H | L | |
| 53 | L | L | L | L | L | H | L | |
| 54 | L | L | L | L | L | H | L | |
| 55 | L | L | L | L | L | H | L | |
| 56 | L | L | L | L | L | H | L | |
| 57 | L | L | L | L | L | H | L | |
| 58 | L | L | L | L | L | H | L | |
| 59 | L | L | L | L | L | H | L | |
| 60 | L | L | L | L | L | H | L | |
| 61 | L | L | L | L | L | H | L | |
| 62 | L | L | L | L | L | H | L | |
| 63 | L | L | L | L | L | H | L | |
| 64 | H | L | L | L | L | L | L | MODE |
| 65 | H | L | L | L | L | L | L | VERIFY |
| 68 | H | L | L | L | L | H | L | Pin 19 |
| 69 | H | L | L | L | L | H | L | Pin 18 |
| 70 | H | L | L | L | L | H | L | Pin 17 |
| 71 | H | L | L | L | L | H | L | Pin 16 |
| 72 | H | L | L | L | L | H | L | Pin 15 |
| 73 | H | L | L | L | L | H | L | Pin 14 |
| 74 | H | L | L | L | L | H | L | Pin 13 |
| 75 | H | L | L | L | L | H | L | Pin 12 |
| 76 | H | L | L | L | H | L | L | PROTECT |

LEGEND: L = Logic Low H = Logic High.

EDIT MODE ROW SELECT TABLE 3 HPL-16RC8,6,4

| PROG MODE | ROW NUMBER | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | VARIABLE | | |
|-----------|------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-------|-------|
| | | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | 16RC8 | 16RC6 | 16RC4 |
| 1 | 0 | H | H | H | H | H | H | H | L | R0 | R0 | R0 |
| | 4 | H | H | H | H | H | H | L | H | R1 | R1 | R1 |
| | 8 | H | H | H | H | H | L | H | H | R2 | R2 | R2 |
| | 12 | H | H | H | H | L | H | H | H | R3 | R3 | R3 |
| | 16 | H | H | H | L | H | H | H | H | R4 | R4 | R4 |
| | 20 | H | H | L | H | H | H | H | H | R5 | R5 | R5 |
| | 24 | H | L | H | H | H | H | H | H | R6 | R6 | R6 |
| | 28 | L | H | H | H | H | H | H | H | R7 | R7 | R7 |
| 2 | 1 | L | L | L | L | L | L | L | H | R0 | R0 | R0 |
| | 5 | L | L | L | L | L | L | H | L | R1 | R1 | R1 |
| | 9 | L | L | L | L | L | L | H | L | R2 | R2 | R2 |
| | 13 | L | L | L | L | L | L | H | L | R3 | R3 | R3 |
| | 17 | L | L | L | L | L | L | H | L | R4 | R4 | R4 |
| | 21 | L | L | L | L | L | L | H | L | R5 | R5 | R5 |
| | 25 | L | H | L | L | L | L | L | L | R6 | R6 | R6 |
| | 29 | H | L | L | L | L | L | L | L | R7 | R7 | R7 |
| 3 | 2 | H | H | H | H | H | H | H | L | F7 | B1 | B3 |
| | 6 | H | H | H | H | H | H | L | H | F8 | F5 | B2 |
| | 10 | H | H | H | H | H | L | H | H | F5 | F4 | F3 |
| | 14 | H | H | H | H | L | H | H | H | F4 | F3 | F2 |
| | 18 | H | H | H | L | H | H | H | H | F3 | F2 | F1 |
| | 22 | H | H | L | H | H | H | H | H | F2 | F1 | F0 |
| | 26 | H | L | H | H | H | H | H | H | F1 | F0 | B1 |
| | 30 | L | H | H | H | H | H | H | H | F0 | B0 | B0 |
| 4 | 3 | L | L | L | L | L | L | H | H | F7 | B1 | B3 |
| | 7 | L | L | L | L | L | H | L | H | F6 | F5 | B2 |
| | 11 | L | L | L | L | L | H | L | L | F5 | F4 | F3 |
| | 15 | L | L | L | L | L | H | L | L | F4 | F3 | F2 |
| | 19 | L | L | L | L | L | H | L | L | F3 | F2 | F1 |
| | 23 | L | L | L | L | L | L | L | L | F2 | F1 | F0 |
| | 27 | L | H | L | L | L | L | L | L | F1 | F0 | B1 |
| | 31 | H | L | L | L | L | L | L | L | F0 | B0 | B0 |
| 1 or 3 | 32 | H | H | H | H | H | H | H | H | CONFIGURE | | |

LEGEND: L = Logic Low H = Logic High

NOTE: The configure row can be selected while in either mode 1 or mode 3.