MACH111-5/7/10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 5 ns t_{PD}
- 167 MHz f_{CNT}
- 38 Bus-Friendly™ Inputs
- Peripheral Component Interconnect (PCI) compliant
- Programmable power-down mode
- 32 Outputs
- 32 Flip-flops; 4 clock choices
- 2 "PAL26V16" Blocks
- Pin-compatible with MACH110, MACH210, MACH211, MACH215
- Improved routing over the MACH110

GENERAL DESCRIPTION

The MACH111 is a member of AMD's EE CMOS Performance Plus MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH111 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL26V16" structures complete with product-term arrays and programmable macrocells, which can be programmed as high speed or low power. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH111 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

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BLOCK DIAGRAM