FINAL | COM'L: -10/12/15/20 | IND: -12/14/18/24

MACH231SP-10/12/15/20

High-Density EE CMOS In-System Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **JTAG-Compatible, 5-V in-system programming**
- **100 Pins**
- **128 Macrocells**
- **10-ns t_{PD} Commercial**
  12-ns t_{PD} Industrial
- **100 MHz f_{CNT}**
- **70 Bus-Friendly™ Inputs and I/Os**
- **Peripheral Component Interconnect (PCI) compliant (-10)**
- **Programmable power-down mode**
- **64 Outputs**
- **128 Flip-flops; 4 clock choices**
- **8 "PAL32V16" blocks with buried macrocells**
- **Improved routing over the MACH230**

IN-SYSTEM PROGRAMMING

In-system programming allows the MACH231SP to be programmed while soldered onto a system board. Programming the MACH231SP in-system yields numerous benefits at all stages of development: prototyping, manufacturing, and in the field. Since insertion into a programmer isn't needed, multiple handling steps and the resulting bent leads are eliminated. The design can be modified in-system for design changes and debugging while prototyping, programming boards in production, and field upgrades.

The MACH231SP offers advantages not available in other CPLD architectures with in-system programming. MACH devices have extensive routing resources for pin-out retention; design changes resulting in pin-out changes for other CPLDs cancel the advantages of in-system programming. The MACH231SP can be employed in any JTAG (IEEE 1149.1) compliant chain.

GENERAL DESCRIPTION

The MACH231SP is a member of AMD's EE CMOS Performance Plus MACH® 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH231SP consists of eight PAL® blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

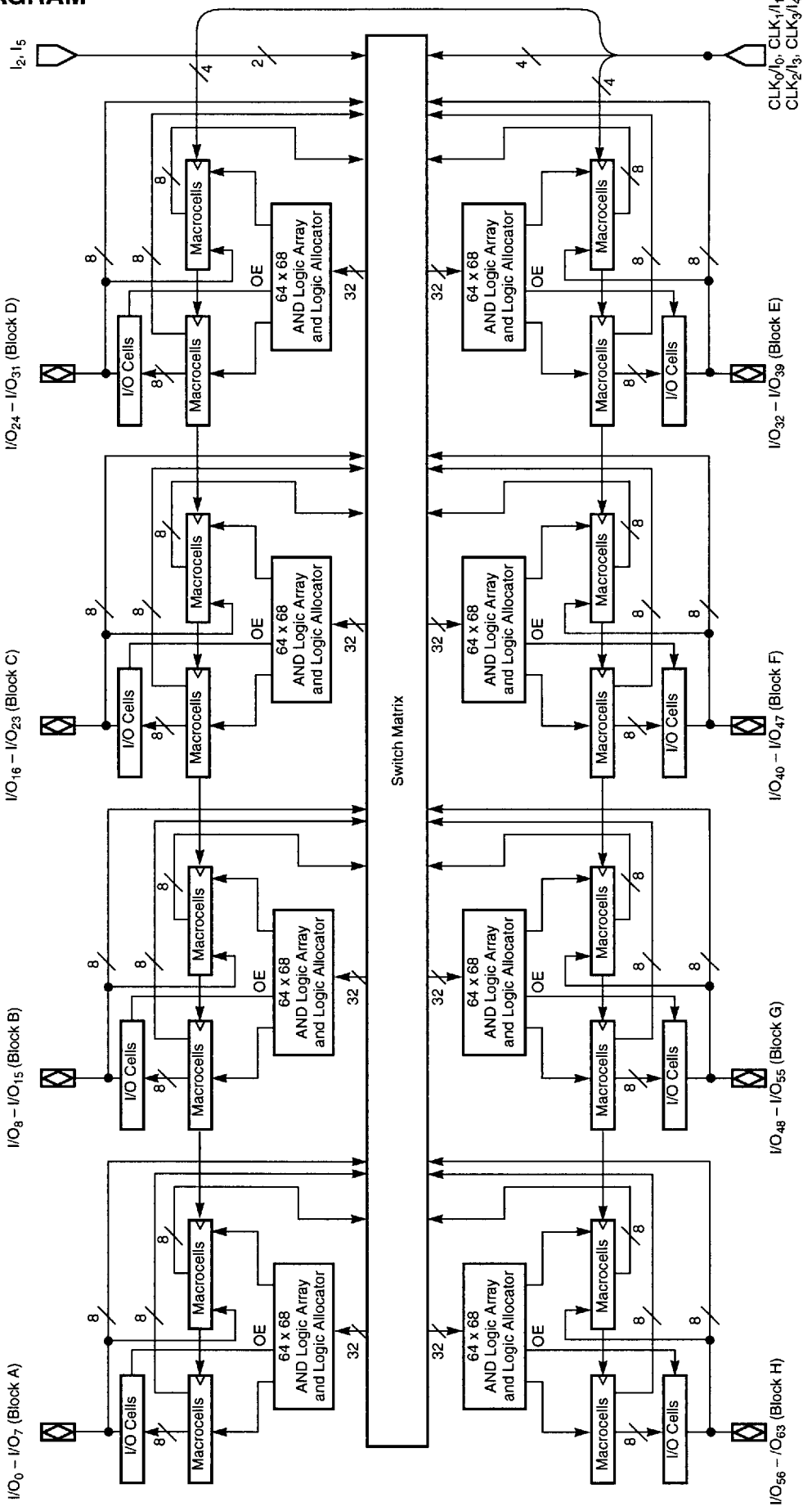
The MACH231SP has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH231SP has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

The MACH231SP is an enhanced version of the MACH231, adding the JTAG-compatible in-system programming feature.

Publication# **20406** Rev: **A** Amendment/**0**
Issue Date: **February 1996**

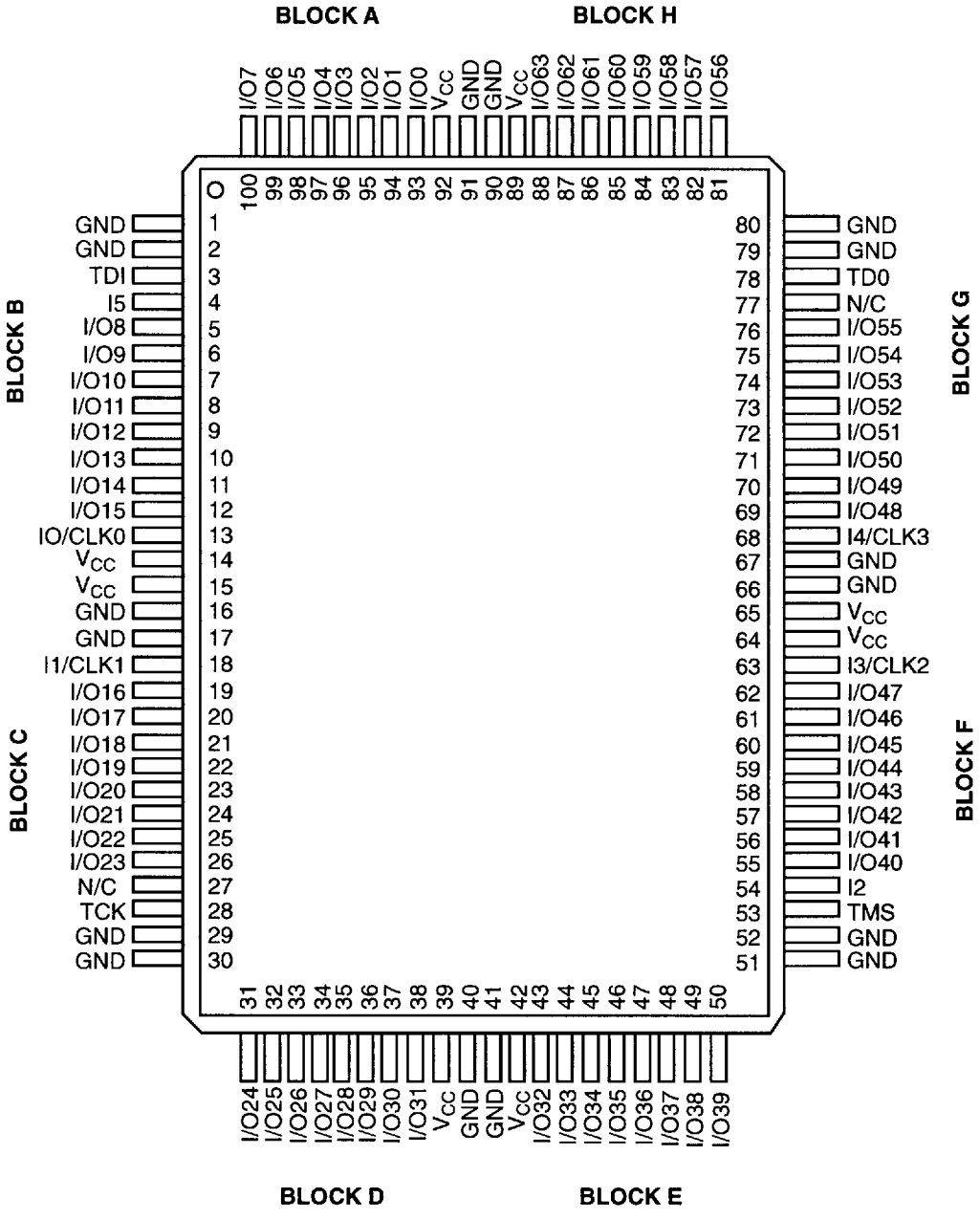
BLOCK DIAGRAM



CONNECTION DIAGRAM MACH231SP

Top View

100-Pin PQFP



20406A-2

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

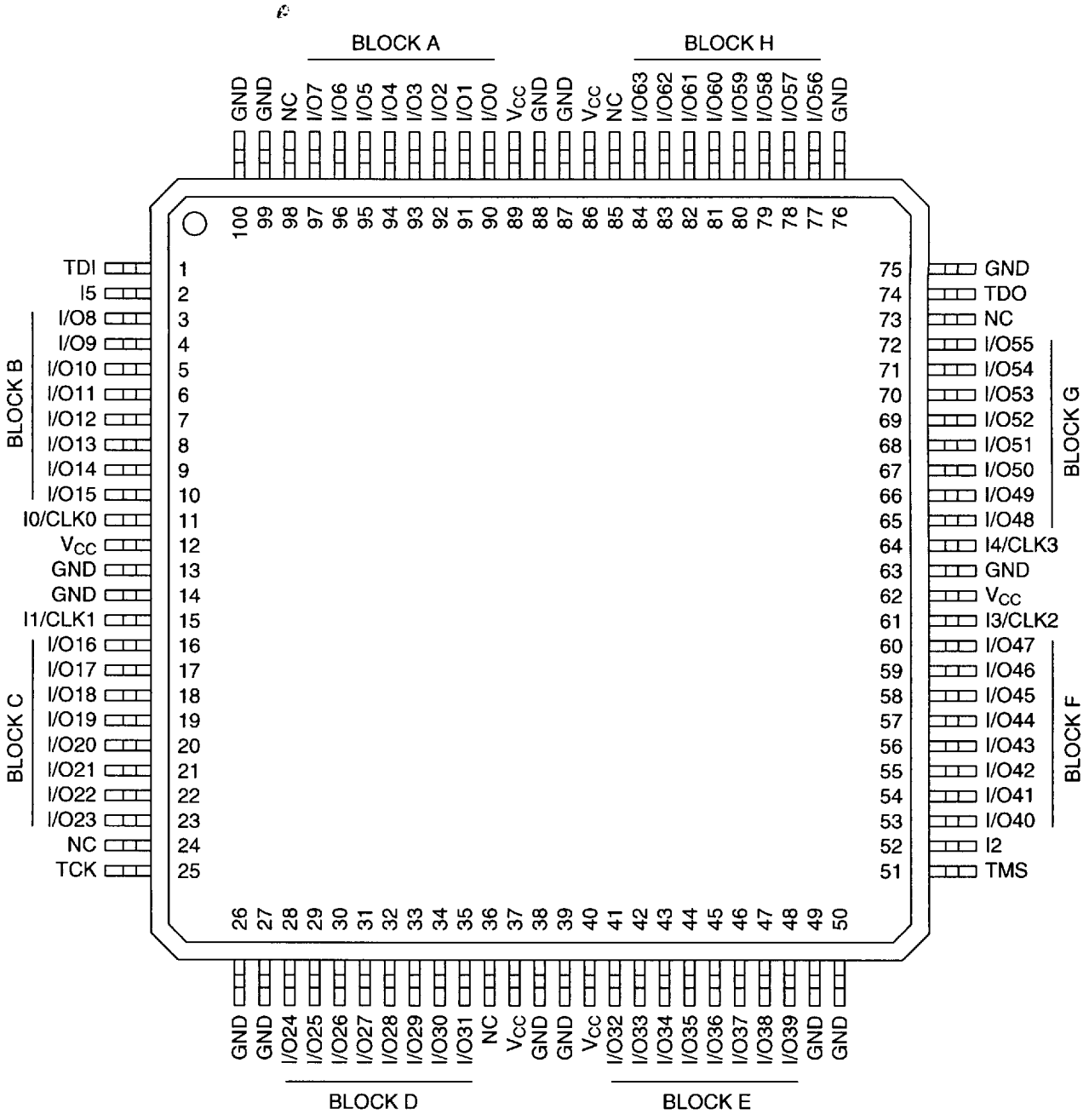
I/O = Input/Output

V_{CC} = Supply Voltage

CONNECTION DIAGRAM MACH231SP

Top View

100-Pin TQFP



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PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

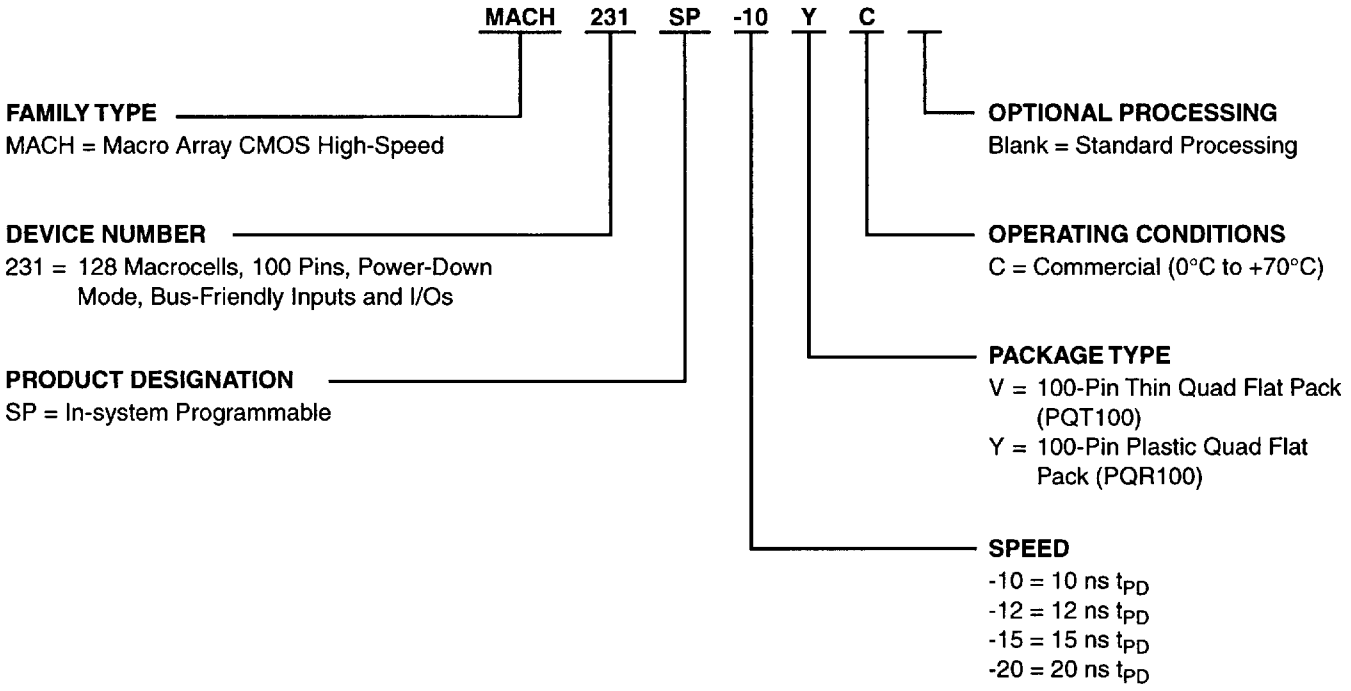
I/O = Input/Output

V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
MACH231SP-10	VC, YC
MACH231SP-12	
MACH231SP-15	
MACH231SP-20	

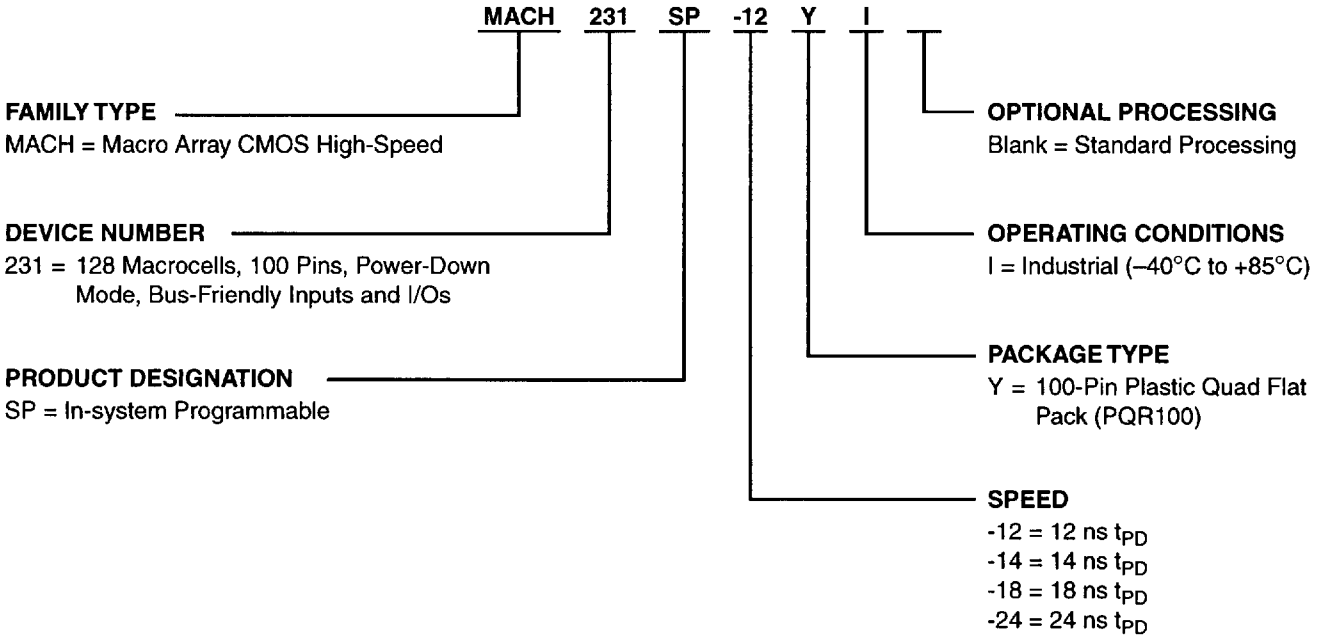
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
MACH231SP-12	YI
MACH231SP-14	
MACH231SP-18	
MACH231SP-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH231SP consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH231SP (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 32 inputs. This makes the PAL block look effectively like an independent "PAL32V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH231SP switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH231SP product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms per PAL block. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset per PAL block.

The Logic Allocator

The logic allocator in the MACH231SP takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms with no speed penalty. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

The Macrocell

The MACH231SP has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

Table 1. Logic Allocation

Macrocell		
Output	Buried	Available Clusters
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH231SP consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Power-Down Mode

The MACH231SP features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in low power mode resulting in power savings of up to 60%. If all signals in a PAL block are low-power, then total power is reduced further.

In-System Programming

Programming is the process where MACH devices are loaded with a pattern defined in a JEDEC file obtained from MACHXL software or third-party software. Programming is accomplished through four JTAG pins: Test Mode Select (TMS), Test Clock (TCK), Test Data In (TDI), and Test Data Out (TDO). The MACH231SP can be employed in any JTAG (IEEE 1149.1) compliant chain. While the MACH231SP is fully JTAG compatible, it does not support EXTEST and SAMPLE/PRELOAD instructions. The MACH231SP can be programmed across the commercial temperature range. Programming the MACH device after it has been placed on a circuit board is easily accomplished. Programming is initiated by placing the device into programming mode, using the MACHPRO programming software provided by AMD. The device is bulk erased and the JEDEC file is then loaded. After the data is transferred into the device, the PROGRAM instruction is loaded. Further programming details can be found in application note, "Advanced In-circuit Programming Guidelines."

On-Board Programming Options

Since the MACHPRO software performs these steps automatically, the following programming options are published for reference.

The configuration file, which is also known as the chain file, defines the MACH device JTAG chain. The file contains the information concerning which JEDEC file is to be placed into which device, the state which the outputs should be placed, and whether the security fuses should be programmed. The configuration file is discussed in detail in the MACHPRO software manual.

The MACH231SP devices tristate the outputs during programming. They have one security bit which inhibits program and verify. This allows the user to protect proprietary patterns and designs.

Program verification of a MACH device involves reading back the programmed pattern and comparing it with the original JEDEC file. The AMD method of program verification performed on the MACH devices permits the verification of one device at a time.

Accidental Programming or Erasure Protection

It is virtually impossible to program or erase a MACH device inadvertently. The following conditions must be met before programming actually takes place:

- The device must be in the password-protected program mode
- The programming or bulk erase instruction must be in the instruction register

If the above conditions are not met, the programming circuitry cannot be activated.

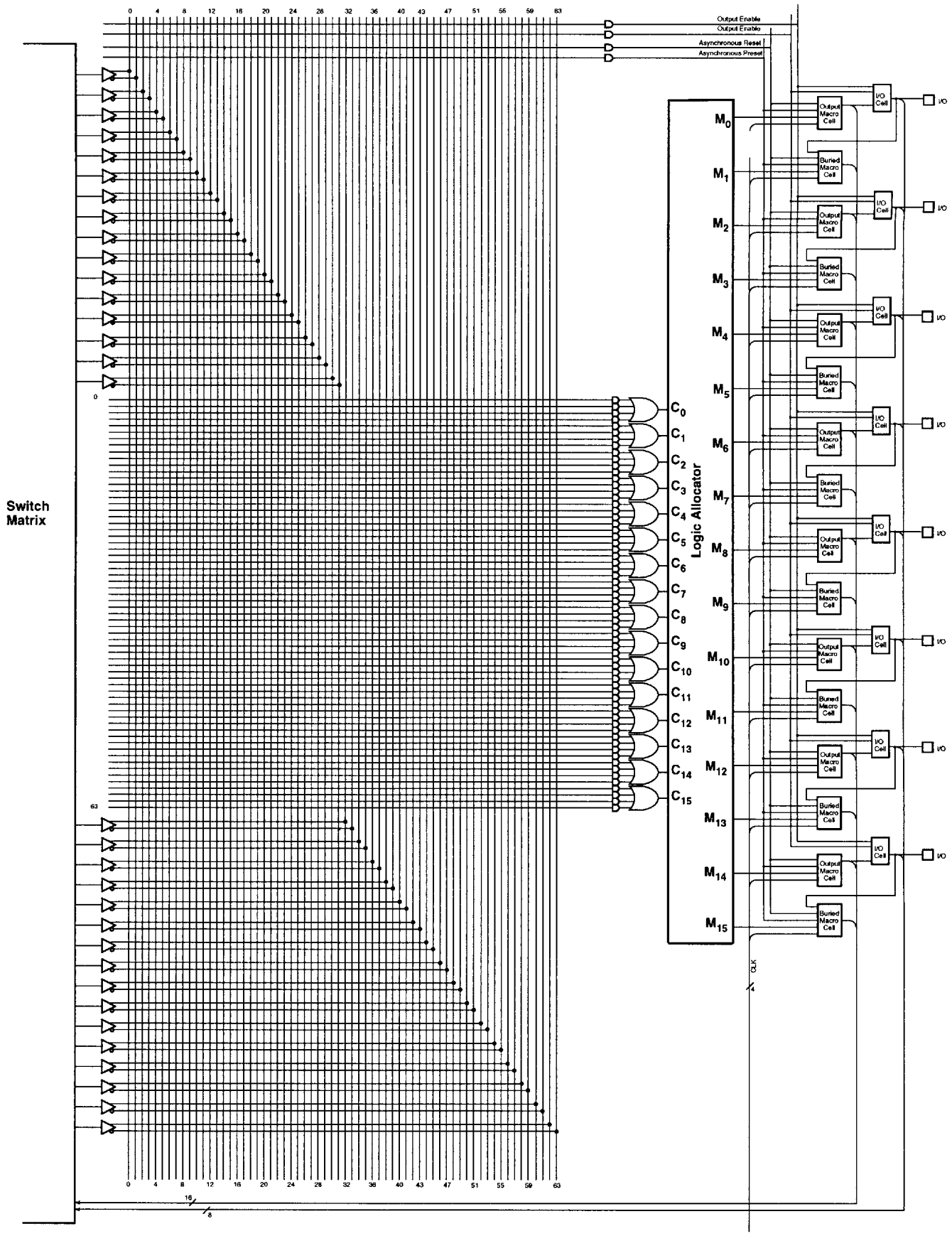
To ensure that the AMD ten year device data retention guarantee applies, 100 program/erase cycle limit should not be exceeded.

Bus-Friendly Inputs and I/Os

The MACH231SP inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the threshold voltage. For an illustration of this configuration, please turn to the Input/Output Equivalent Schematics section.

PCI Compliance

The MACH231SP-10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH231SP-10's predictable timing ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without predictable timing, PCI compliance is dependent upon routing and product term distribution.



20406A-4

Figure 1. MACH231SP PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground. . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage. . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = 0°C to 70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . .0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5 V, f = 0 MHz, T_A = 25°C (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, f = 1 MHz, T_A = 25°C (Note 4)		100		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10		-12		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					10		12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	6.5		7		ns
				T-type	7.5		8		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					6.5		8	ns
t_{WL}	Clock Width			LOW	4		6		ns
t_{WH}				HIGH	4		6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	77		66.7		MHz
				T-type	72		62.5		MHz
		Internal Feedback (f_{CNT})		D-type	100		83.3		MHz
				T-type	91		76.9		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		125		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				6.5		7		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output					7.5		8.5	ns
t_{GWL}	Gate Width LOW				4		6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		14.5	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2.5		2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15.5		16	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	11		12		ns
				T-type	12		13		ns
t_{WICL}	Input Register Clock Width			LOW	4		6		ns
t_{WICH}				HIGH	4		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			125		80		MHz
t_{SIL}	Input Latch Setup Time				2		2.5		ns
t_{HIL}	Input Latch Hold Time				2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					18		19.5	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-10		-12		Unit
		Min	Max	Min	Max	
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	10		10.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	11		13.5		ns
t_{WIGL}	Input Latch Gate Width LOW	4		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		17	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		13		16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	10		12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	7.5		8		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		13		16	ns
t_{APW}	Asynchronous Preset Width (Note 1)	10		12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	7.5		8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		12		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		12		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground. . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O
Pin Voltage. . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
(T_A = 0°C to 70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . .0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Static)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = 5 V, f = 0 MHz, T_A = 25°C (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, f = 1 MHz, T_A = 25°C (Note 4)		100		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output					11		12	ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	15		20		ns
				T-type	16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					22		27	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	16		21		ns
t_{WIGL}	Input Latch Gate Width LOW	6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		15		20	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground. . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Notes 3, 5)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		100		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled and reset.*
5. *This parameter is not 100% tested, but evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-14		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		14.5	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8		8.5		ns
				T-type	9		10		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10	ns
t_{WL}	Clock Width			LOW	6		7.5		ns
t_{WH}				HIGH	6		7.5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	65		54		MHz
				T-type	61		50		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		61.5		MHz
				T-type	76.9		57		MHz
		No Feedback	$1/(t_S + t_H)$		83.3		66.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8		8.5		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					10		12	ns
t_{GWL}	Gate Width LOW				6		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		18	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		14.5		ns
				T-type	13		16		ns
t_{WICL}	Input Register Clock Width			LOW	6		7.5		ns
t_{WICH}				HIGH	6		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			83.3		66.5		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					19		20.5	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					21		23	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-12		-14		Unit
		Min	Max	Min	Max	
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	10.5		11		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	13.5		16		ns
t_{WIGL}	Input Latch Gate Width LOW	6		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17		19.5	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		19.5	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		14.5		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		19.5		19.5	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		14.5		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		15		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		15		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground. . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Notes 3, 5)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		90		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		100		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled and reset.*
5. *This parameter is not 100% tested, but evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-18		-24		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		16		ns
				T-type	13.5		17		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		10		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	41		32		MHz
				T-type	39		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	53		38		MHz
				T-type	44		34.5		MHz
		No Feedback	$1/(t_S + t_H)$		66.5		50		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				12		16		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					13.5		14.5	ns
t_{GWL}	Gate Width LOW				7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	18		24		ns
				T-type	19.5		25.5		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		10		ns
t_{WICH}				HIGH	7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					26.5		32.5	ns

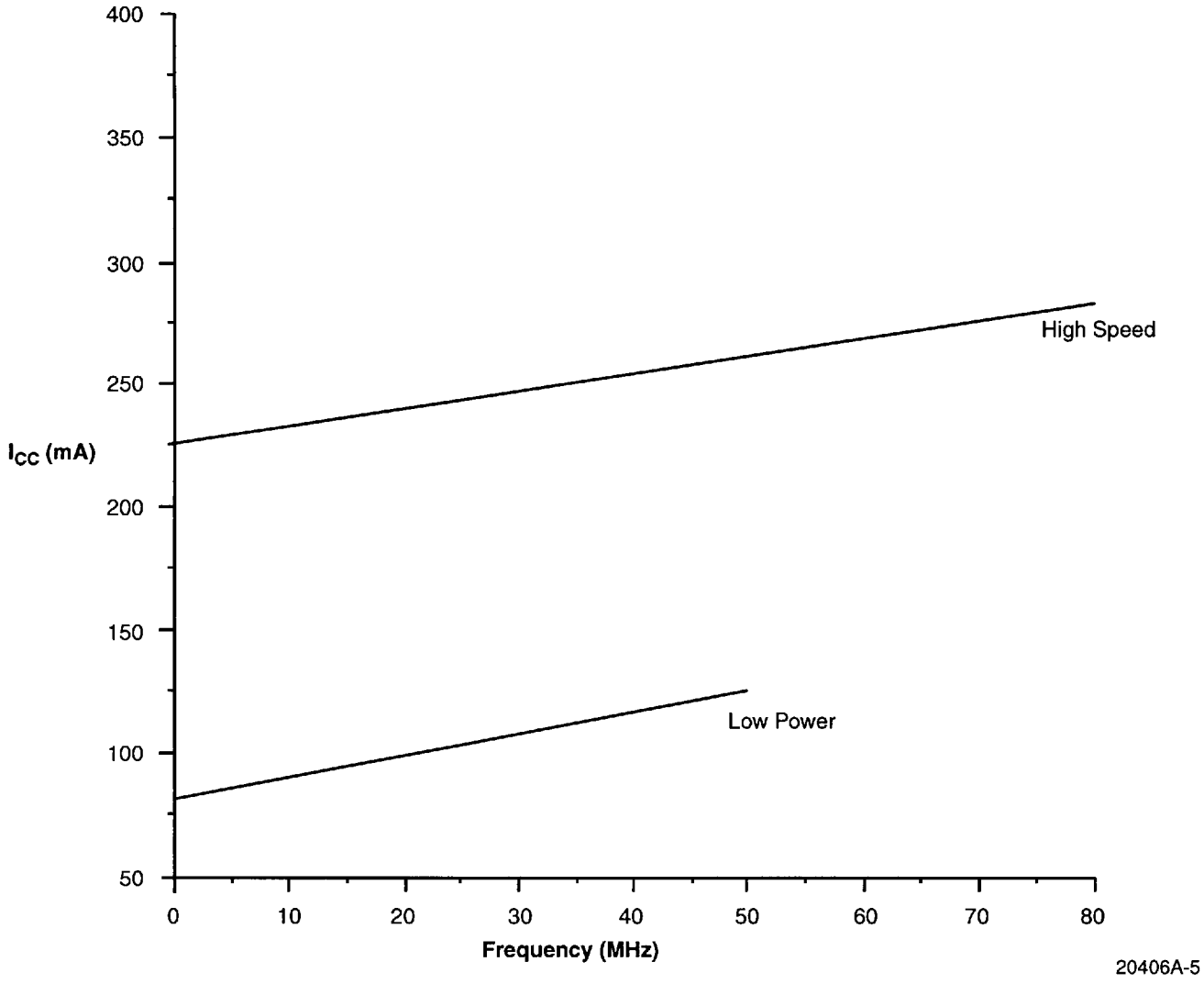
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-18		-24		Unit
		Min	Max	Min	Max	
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	14.5		18		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW	7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		23		29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		18		24	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		7		7	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		3		3	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*
3. *If a signal is powered down, this parameter must be added to its respective high-speed parameter.*

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

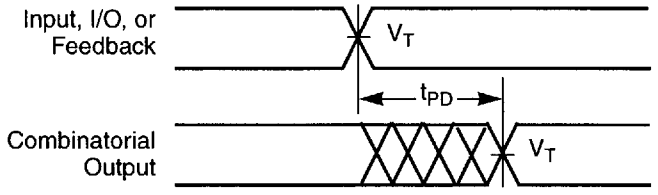
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			PQFP	TQFP	
θ_{jc}	Thermal impedance, junction to case		5	TBD	°C/W
θ_{ja}	Thermal impedance, junction to ambient		22.5	TBD	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	19.2	TBD	°C/W
		400 lfpm air	17.9	TBD	°C/W
		600 lfpm air	17	TBD	°C/W
		800 lfpm air	16.2	TBD	°C/W

Plastic θ_{jc} Considerations

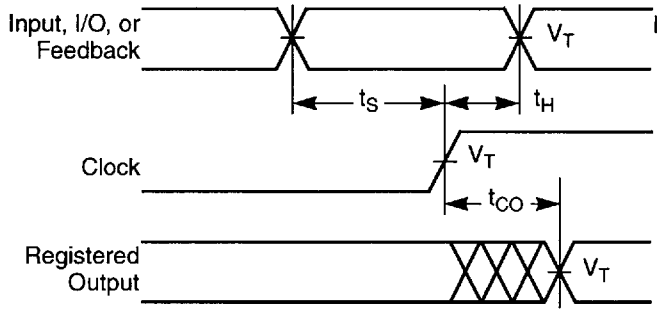
The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

SWITCHING WAVEFORMS



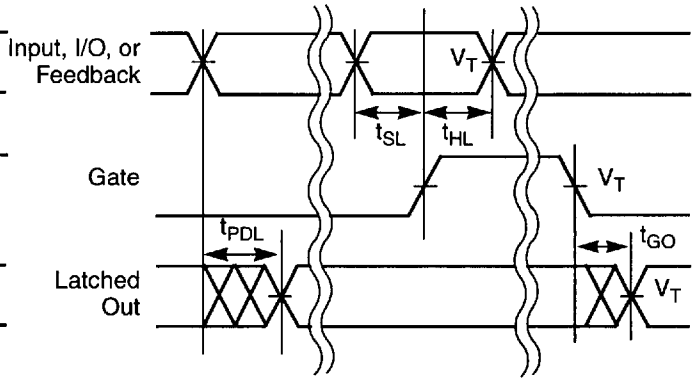
20406A-6

Combinatorial Output



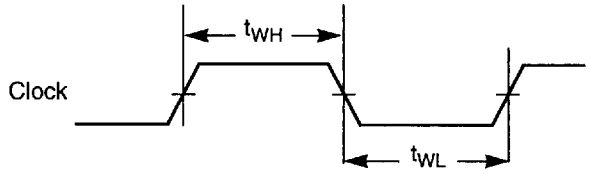
20406A-7

Registered Output



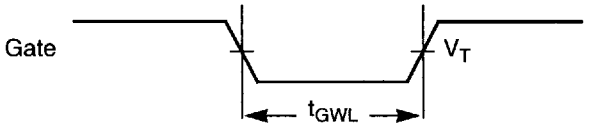
20406A-8

Latched Output



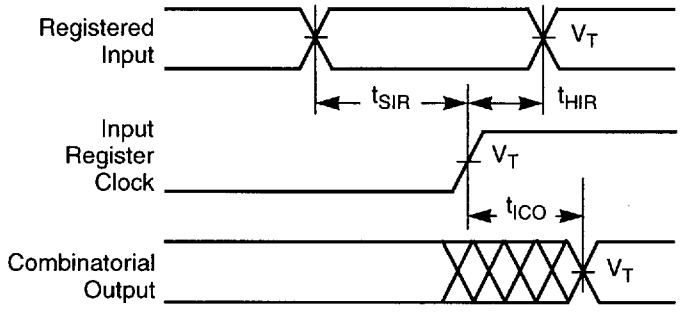
20406A-9

Clock Width



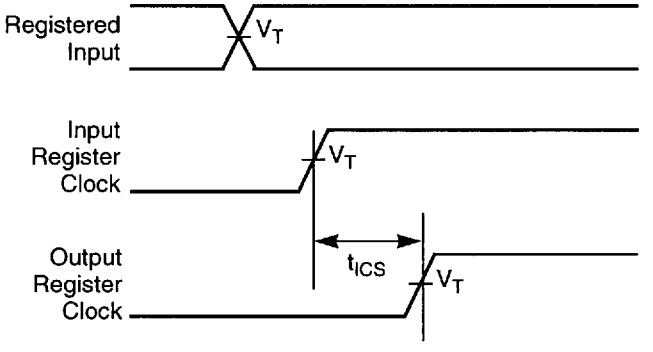
20406A-10

Gate Width



20406A-11

Registered Input



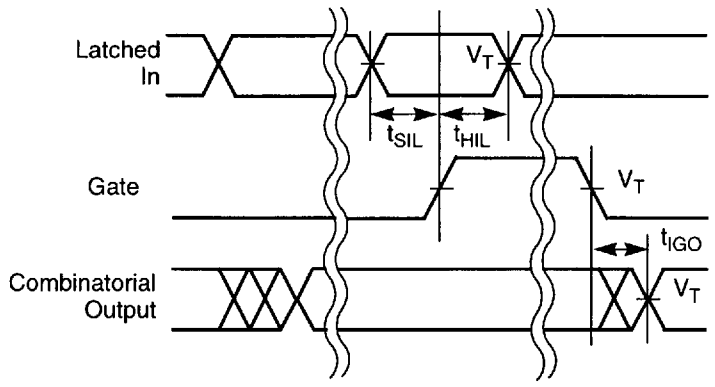
20406A-12

Input Register to Output Register Setup

Notes:

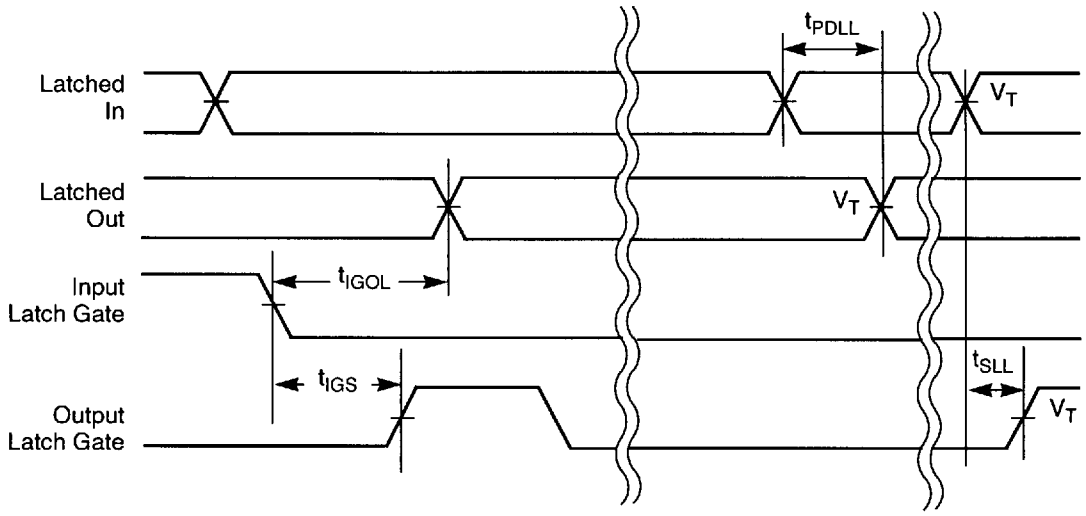
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



20406A-13

Latched Input



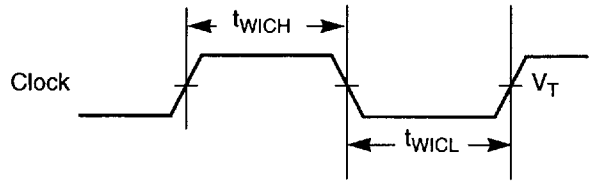
20406A-14

Latched Input and Output

Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS

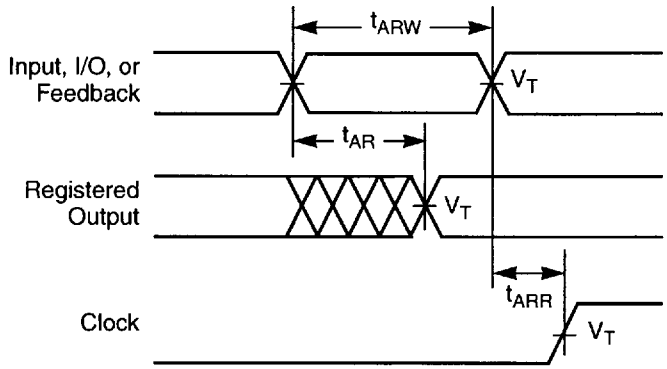


20406A-15

Input Register Clock Width

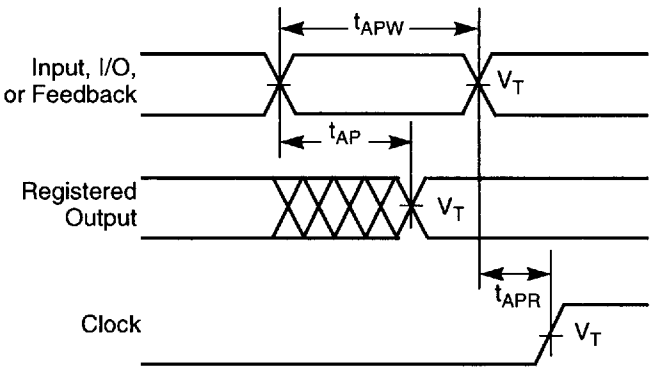
20406A-16

Input Latch Gate Width



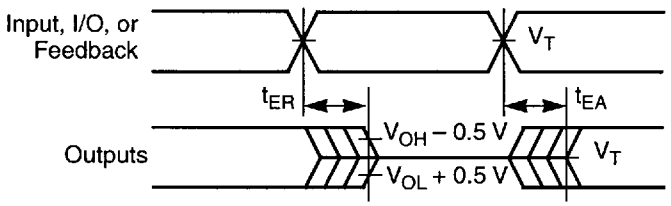
20406A-17

Asynchronous Reset



20406A-18

Asynchronous Preset



20406A-19

Output Disable/Enable

Notes:

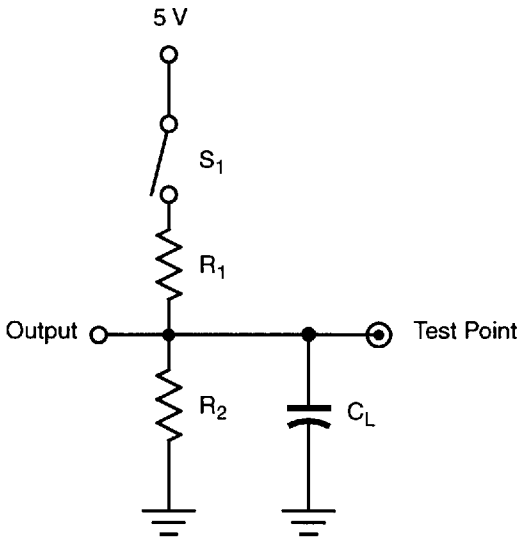
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



20406A-20

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

** Switching several outputs simultaneously should be avoided for accurate measurement.*

F_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

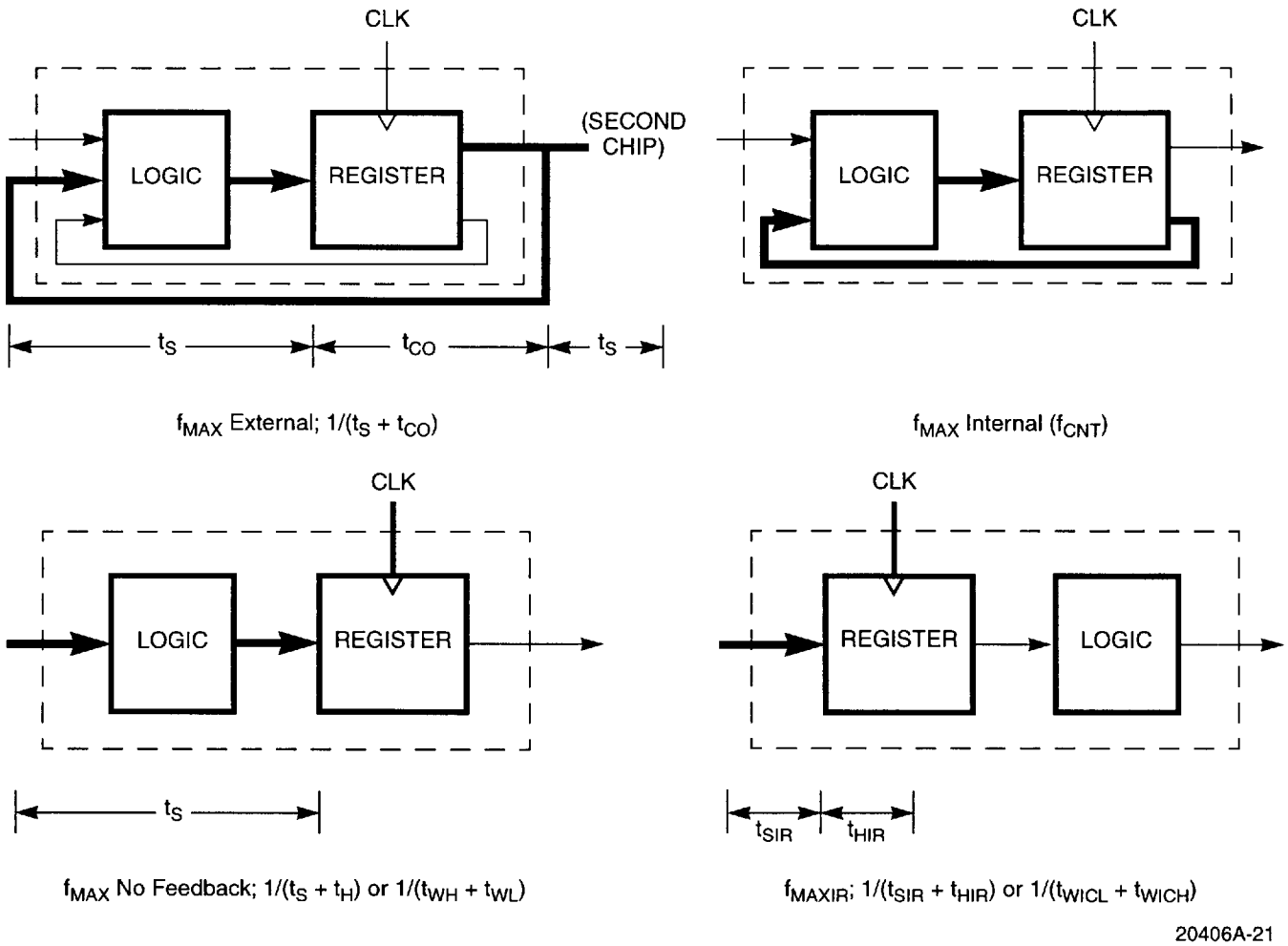
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



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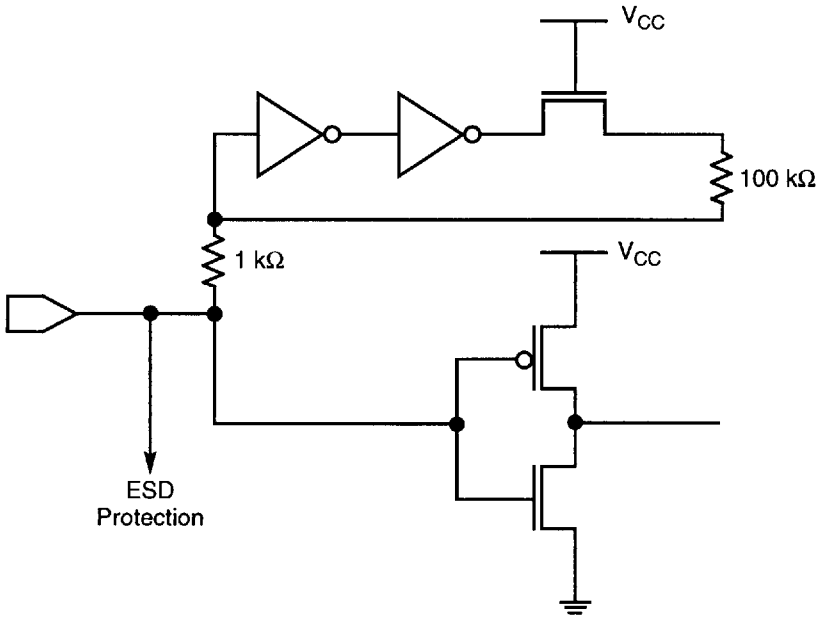
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

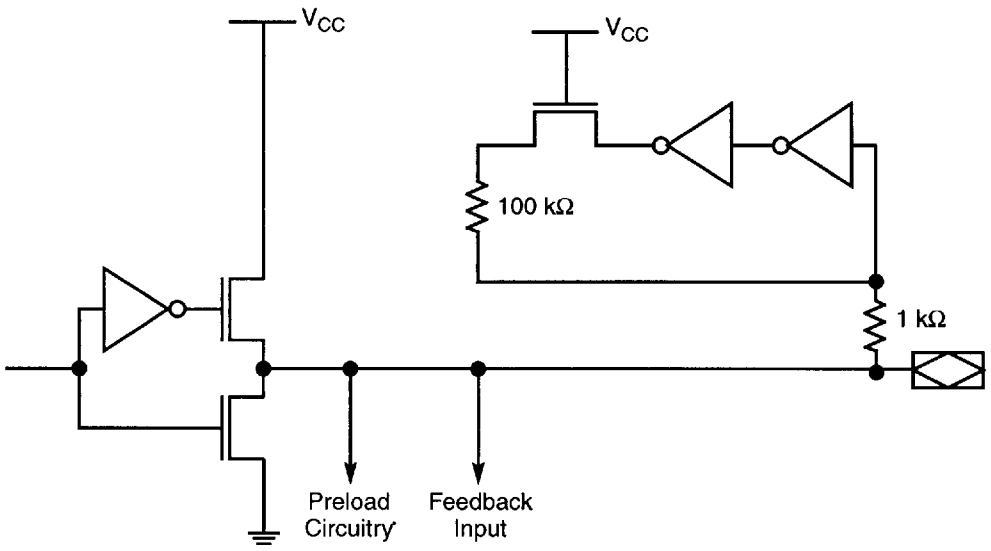
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



I/O

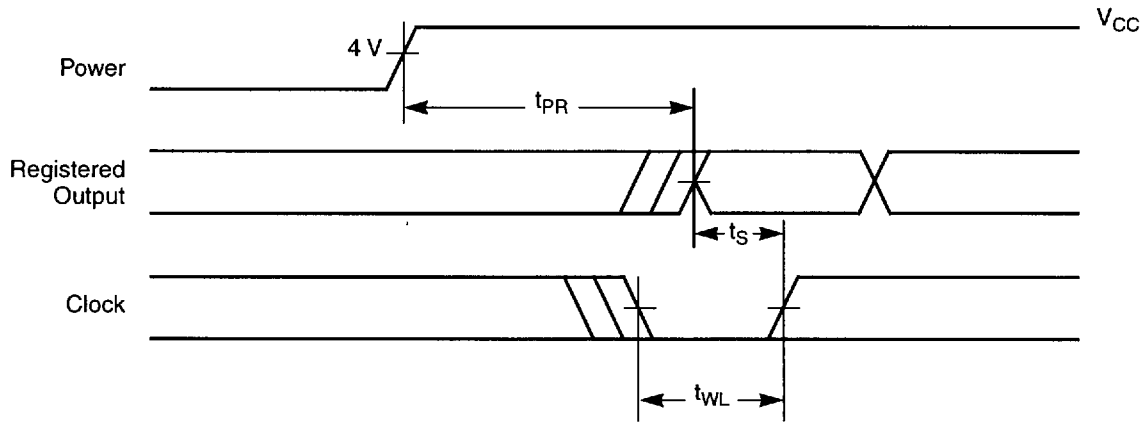
20406A-22

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



20406A-23

Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL® Software Ver. 3.0
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Design Center/AMD Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD-ABEL Software Data I/O MACH Fitters
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PROdeveloper/AMD Software PROsynthesis/AMD Software
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	PLD™ Designer Verilog, LeapFrog, RapidSim Simulators Ver. 9504
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Software Synario™ Software
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ II QuickSim Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	Design Center Software
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner™-XL Software
SUSIE-CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator
Synopsys Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Library
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR

DEVELOPMENT SYSTEMS (subject to change) (continued)

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD or PROPLD (Requires PROSim Simulator MACH Fitter) ViewSim Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	PROGRAMMER CONFIGURATION (Note 1)
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 243-7000	Pilot U84
BP Microsystems 100 N. Post Oak Rd. Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600	BP1200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ Model 3900 AutoSite
Hi/Lo 4F, No. 2, Sec. 5, Ming Shoh E. Rd. Taipei, Taiwan	ALL-07
Logical Devices Inc./Digelec 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766 or (305) 428-6868	ALLPRO™-88
SMS North America, Inc. 16522 NE 135th Place Redmond, WA 98052 (800) 722-4122 or SMS Im Grund 15 D-7988 Vangen Im Allgau, Germany 07522-5018	Sprint/Expert
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Stag Quazar
System General 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Turpro-1

Note:

1. Please contact the manufacturer for latest revision.

APPROVED ON-BOARD PROGRAMMERS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAG PROG
Advanced Micro Devices P.O. Box 3453, MS-1028 Sunnyvale, CA 94088-3453 (800) 222-9323	MACHPRO

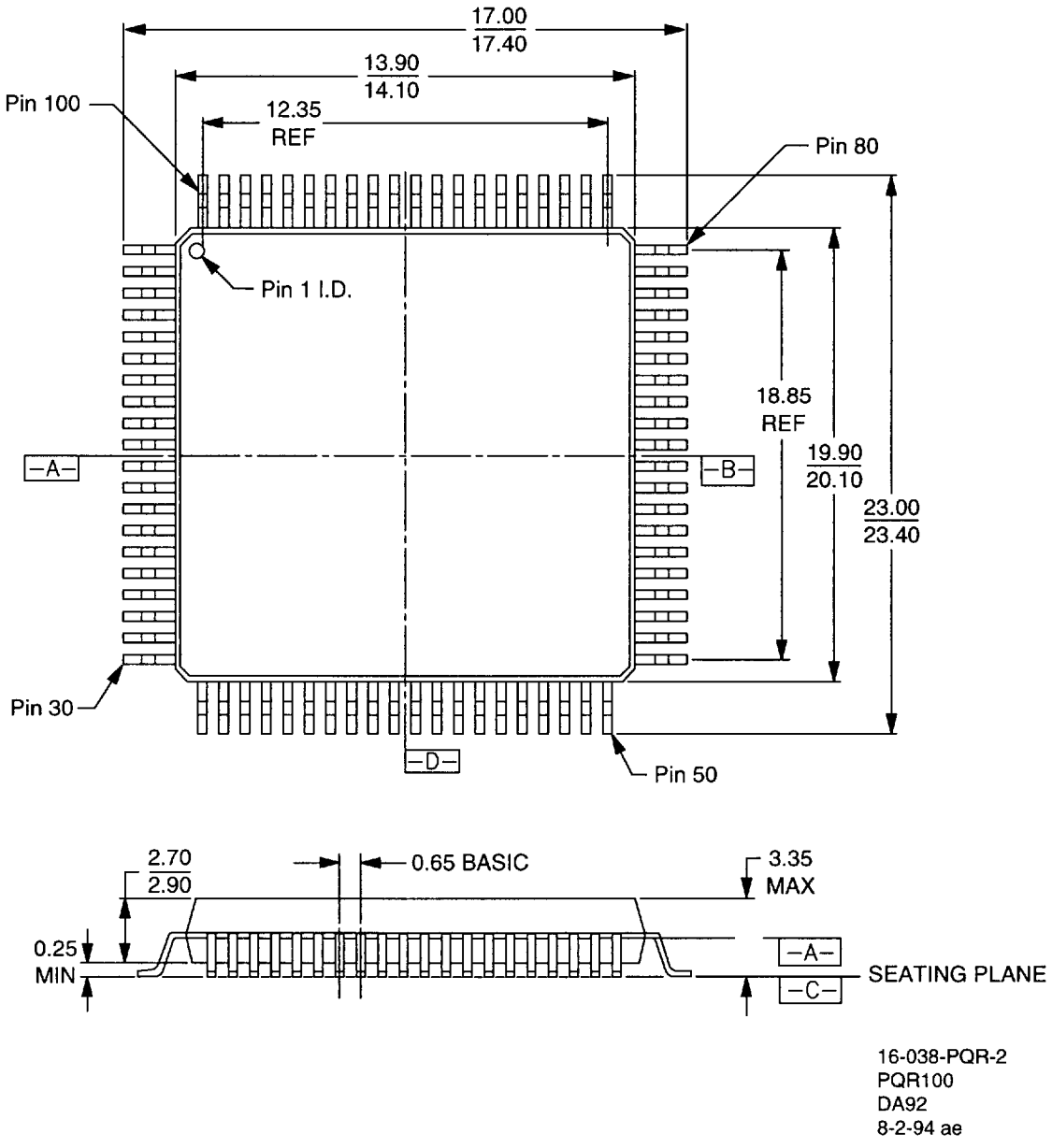
PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART NUMBER
California Integration Technologies 656 Main Street Placerville, CA 95667	Contact Manufacturer
EDI Corporation P.O. Box 366 Patterson, CA 95363 (209) 892-3270	Contact Manufacturer
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660	Contact Manufacturer
Logical Systems Corp. P.O. Box 6184 Syracuse, NY 13217-6184 (315) 478-0722	Contact Manufacturer
Procon Technologies, Inc. 1333 Lawrence Expwy, Suite 207 Santa Clara, CA 95051 (408) 246-4456	Contact Manufacturer

PHYSICAL DIMENSIONS*

PQR100

100-Pin Plastic Quad Flat Pack (measured in millimeters)



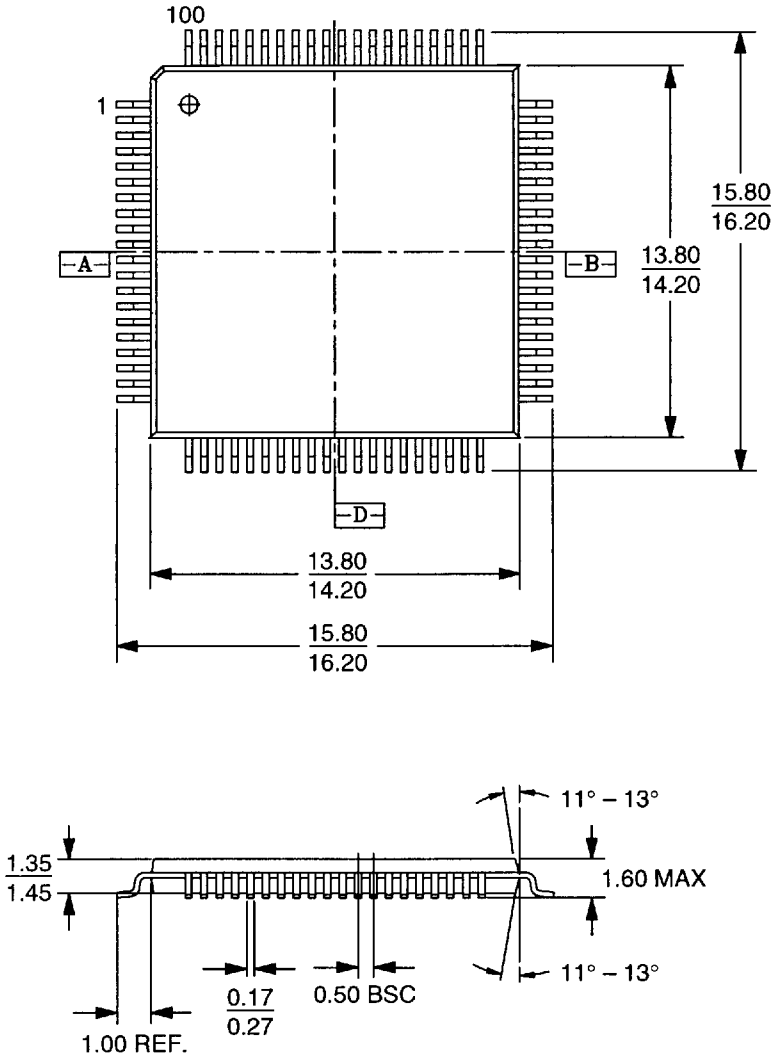
16-038-PQR-2
PQR100
DA92
8-2-94 ae

** For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS

PQT100

100-Pin Thin Quad Flat Pack (measured in millimeters)



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PQT100
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