

### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.



Not Intended For New Designs

## 100182 9-Bit Wallace Tree Adder

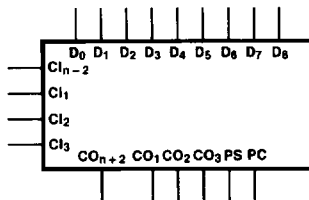
### General Description

The 100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The 100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the

100183 Recode Multiplier, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100182 assists in performing parallel multiplication of two signed numbers to produce a signed two's complement product. See 100183 data sheet for additional information. All inputs have 50 k $\Omega$  pull-down resistors.

**Ordering Code:** See Section 6

### Logic Symbol

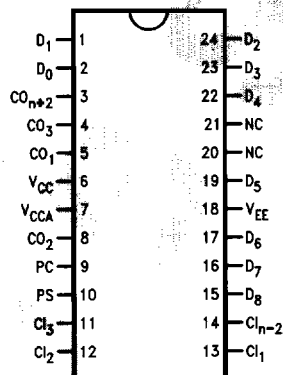


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Pin Names	Description
D <sub>0</sub> -D <sub>8</sub>	Data Inputs
Cl <sub>1</sub> -Cl <sub>3</sub> , Cl <sub>n-2</sub>	Carry Inputs
CO <sub>1</sub> -CO <sub>3</sub> , CO <sub>n+2</sub>	Carry Outputs
PS	Partial Sum Output
PC	Partial Carry Output

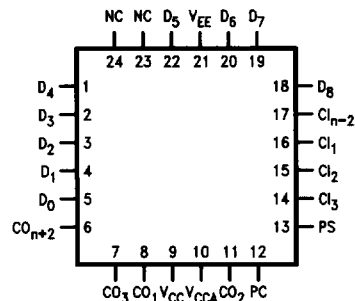
### Connection Diagrams

24-Pin DIP



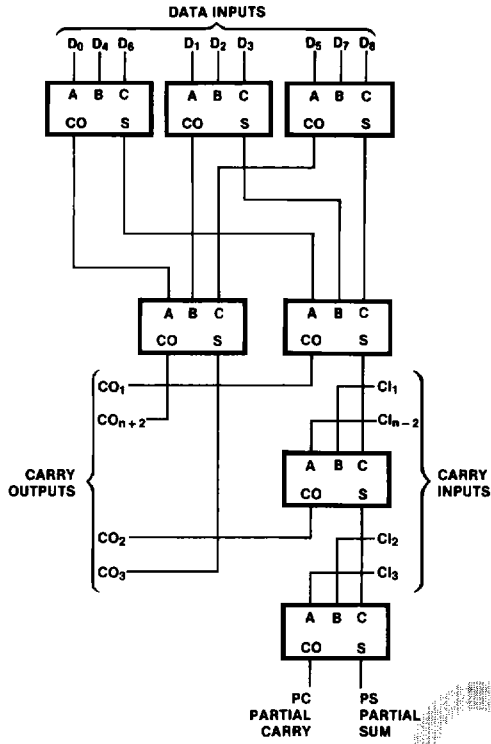
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24-Pin Quad Cerpak

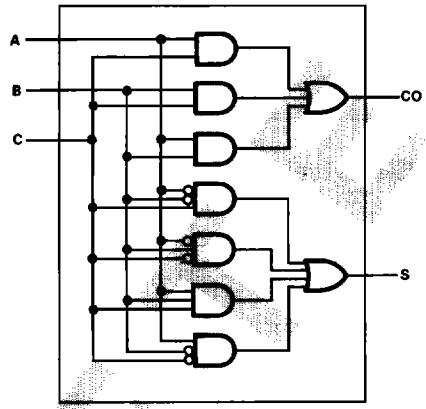


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### Logic Diagram



### Adder Logic Diagram



Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H



**DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-4.8V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ 

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{IH}$	Input HIGH Current $Cl_1 - Cl_3, Cl_{n-2}$ $D_1, D_3, D_4, D_5, D_6, D_8$			300	$\mu A$	$V_{IN} = V_{IH} (Max)$
	$D_0, D_2, D_7$			250		
$I_{EE}$	Power Supply Current	-260	-180	-125	mA	Inputs Open

**Ceramic Dual-In-Line Package AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_{n+2}$	1.40	4.50	1.40	4.50	1.50	4.70	ns	Figures 1 and 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_1$	1.30	4.80	1.30	4.70	1.50	5.00	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_2$	2.20	6.20	2.20	6.10	2.30	6.40	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_3$	1.30	4.70	1.40	4.70	1.50	5.00	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to PS, PC	2.50	7.20	2.50	7.20	2.70	7.40	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_{n-2}, Cl_1$ to $CO_2$	1.00	3.50	1.00	3.40	1.10	3.70	ns	Figures 1 and 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_{n-2}, Cl_1$ to PS, PC	1.50	4.50	1.50	4.45	1.60	4.60	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_3, Cl_2$ to PS, PC	0.80	3.30	0.80	3.20	0.90	3.60	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	Figures 1 and 2

## Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_{n+2}$	1.40	4.30	1.40	4.30	1.50	4.50	ns	<i>Figures 1 and 2</i>
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_1$	1.30	4.60	1.30	4.50	1.50	4.80	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_2$	2.20	6.00	2.20	5.90	2.30	6.20	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $CO_3$	1.30	4.50	1.40	4.50	1.50	4.80	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to PS, PC	2.50	7.00	2.50	7.00	2.70	7.20	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_{n-2}$ , $Cl_1$ to $CO_2$	1.00	3.30	1.00	3.20	1.10	3.50	ns	<i>Figures 1 and 2</i>
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_{n-2}$ , $Cl_1$ to PS, PC	1.50	4.30	1.50	4.25	1.60	4.40	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $Cl_3$ , $Cl_2$ to PS, PC	0.80	3.10	0.80	3.00	0.90	3.40	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	<i>Figures 1 and 2</i>

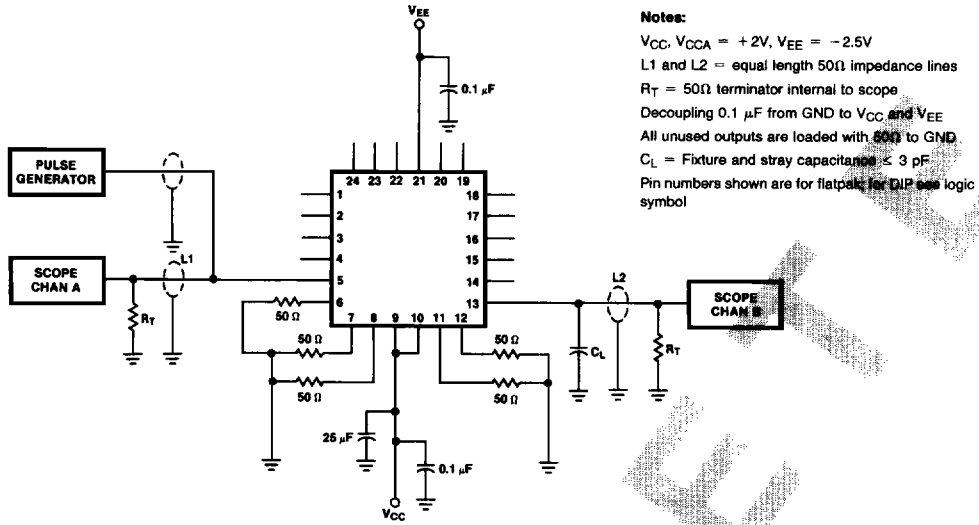


FIGURE 1. AC Test Circuit

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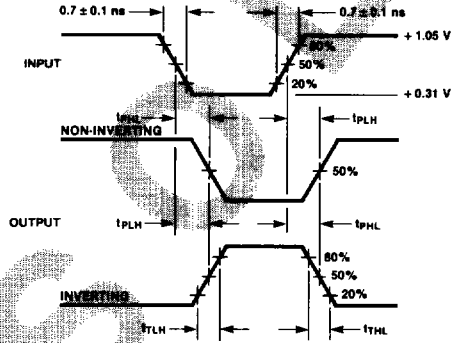
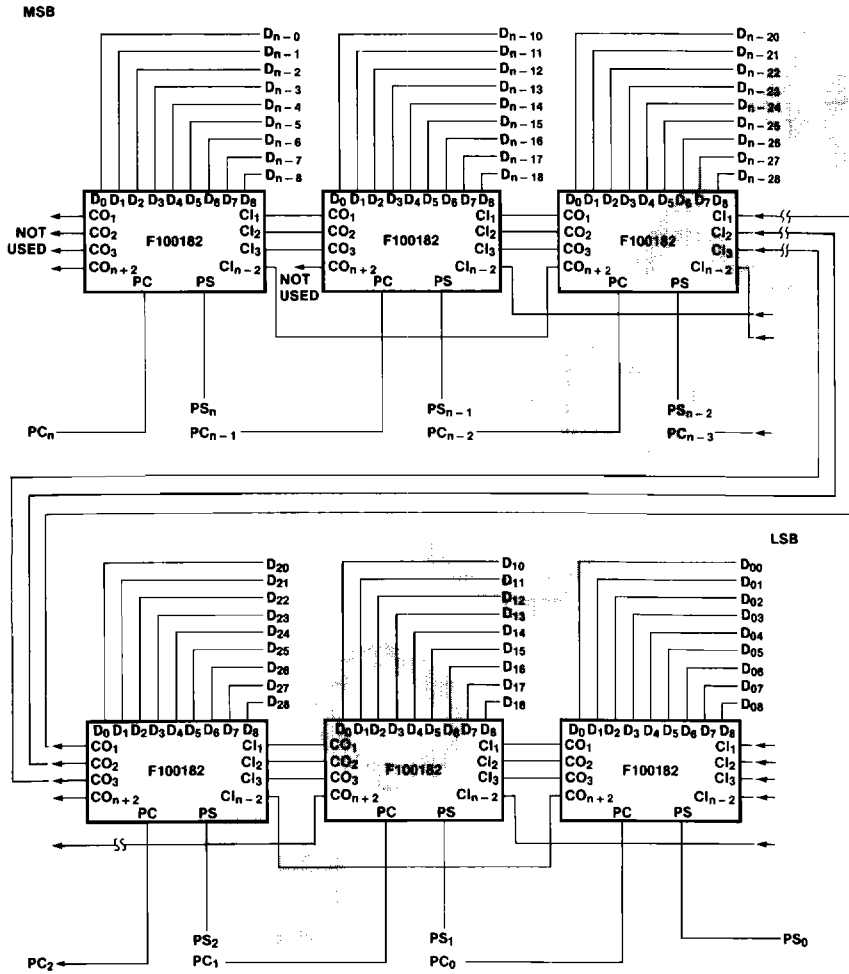


FIGURE 2. Propagation Delay and Transition Times

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# Application

Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182

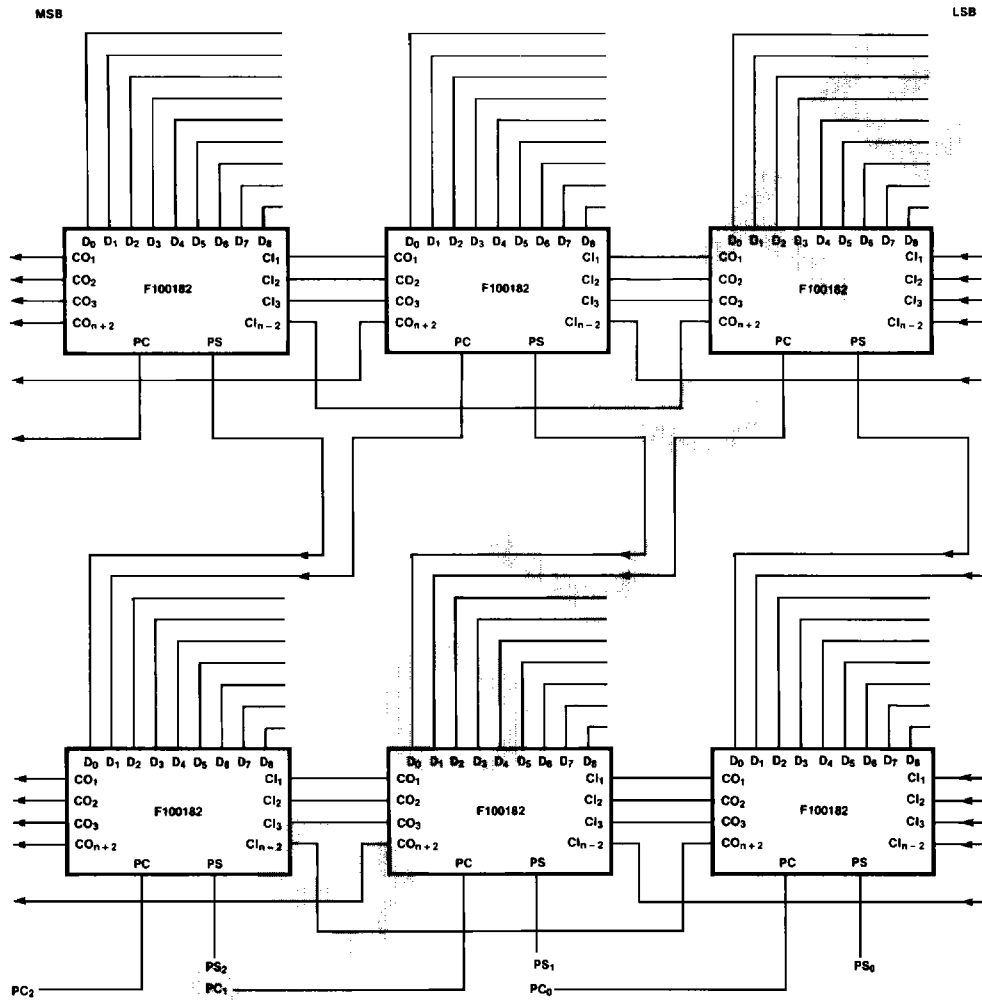


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# Application (Continued)

## 16-Bit Vertical Expansion of Wallace Tree Adders



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100182