National Semiconductor

DM54S160/DM74S160, DM54S161/DM74S161, DM54S162/DM74S162, DM54S163/DM74S163 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The S160 and S162 are 4-bit decade counters and the S161 and S163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 9 ns
- Typical clock frequency 70 MHz
- Typical power dissipation 475 mW

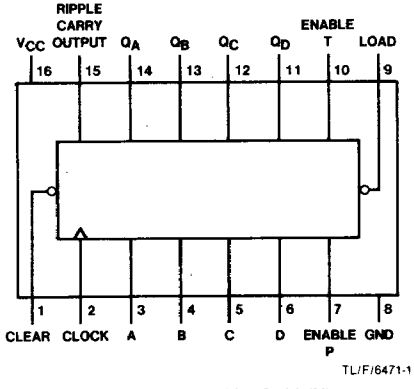
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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DM54S160 (J) DM74S160 (N)
DM54S161 (J) DM74S161 (N)
DM54S162 (J) DM74S162 (N)
DM54S163 (J) DM74S163 (N)

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Sym	Parameter		DM54S161 thru 163			DM74S161 thru 163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0		40	0		40	MHz
	Clock Frequency (Note 2)		0		35	0		35	
t_W	Pulse Width (Note 1)	Clock	10			10			ns
		Clear	10			10			
	Pulse Width (Note 2)	Clock	12			12			
		Clear	12			12			
t_{SU}	Setup Time (Note 1)	Data	4			4			ns
		Enable P	12			12			
		Load	14			14			
		Clear (Note 3)	14			14			
	Setup Time (Note 2)	Data	5			5			
		Enable P	14			14			
		Load	16			16			
		Clear (Note 3)	16			16			
t_H	Hold Time (Note 1)	Data	3			3			ns
		Others	0			0			
	Hold Time (Note 2)	Data	5			5			
		Others	2			2			
t_{REL}	Clear Release Time (Note 1)		12			12			ns
	Clear Release Time (Note 2)		14			14			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: $C_L = 15$ pF and $R_L = 280\Omega$.
Note 2: $C_L = 50$ pF and $R_L = 280\Omega$.
Note 3: Applies only to 'S162 and 'S163 which have synchronous clear inputs.

'S160 thru 'S163 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			100	μA
			Others			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Enable T			−4	mA
			Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 280Ω						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		40	70		35	60		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		14	25		16	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		17	25		19	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Any Q		8	15		10	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Any Q		10	15		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		10	15		12	18	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		10	15		12	18	ns
t_{PLH} Propagation Delay Time Low to High Level Output (Note 3)	Clear to Any Q		14	20		16	24	ns

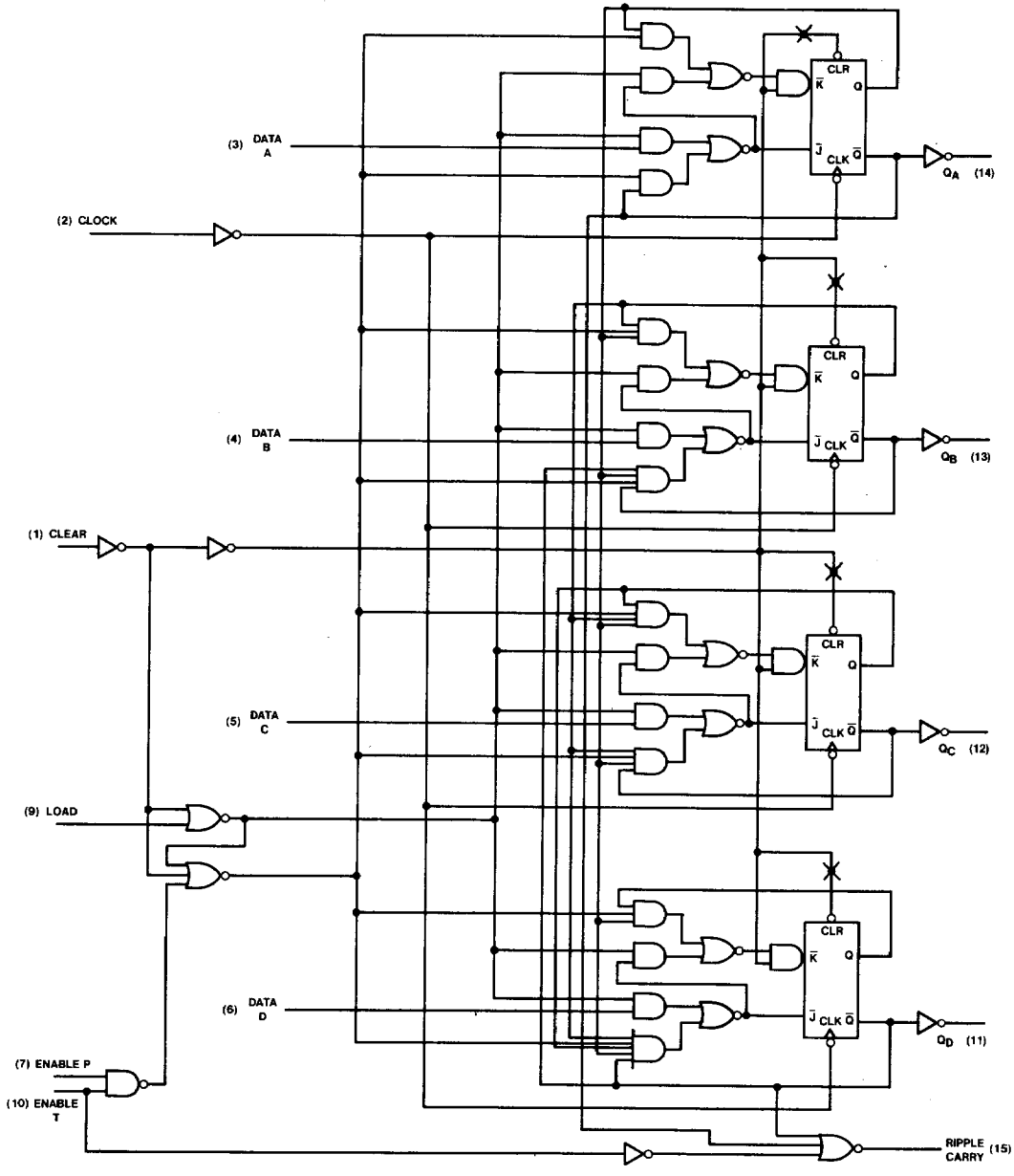
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Propagation delay for clearing is measured from clear input for 'S160 and 'S161 and from the clock input transition for the 'S162 and 'S163.

Logic Diagrams

S160, S162



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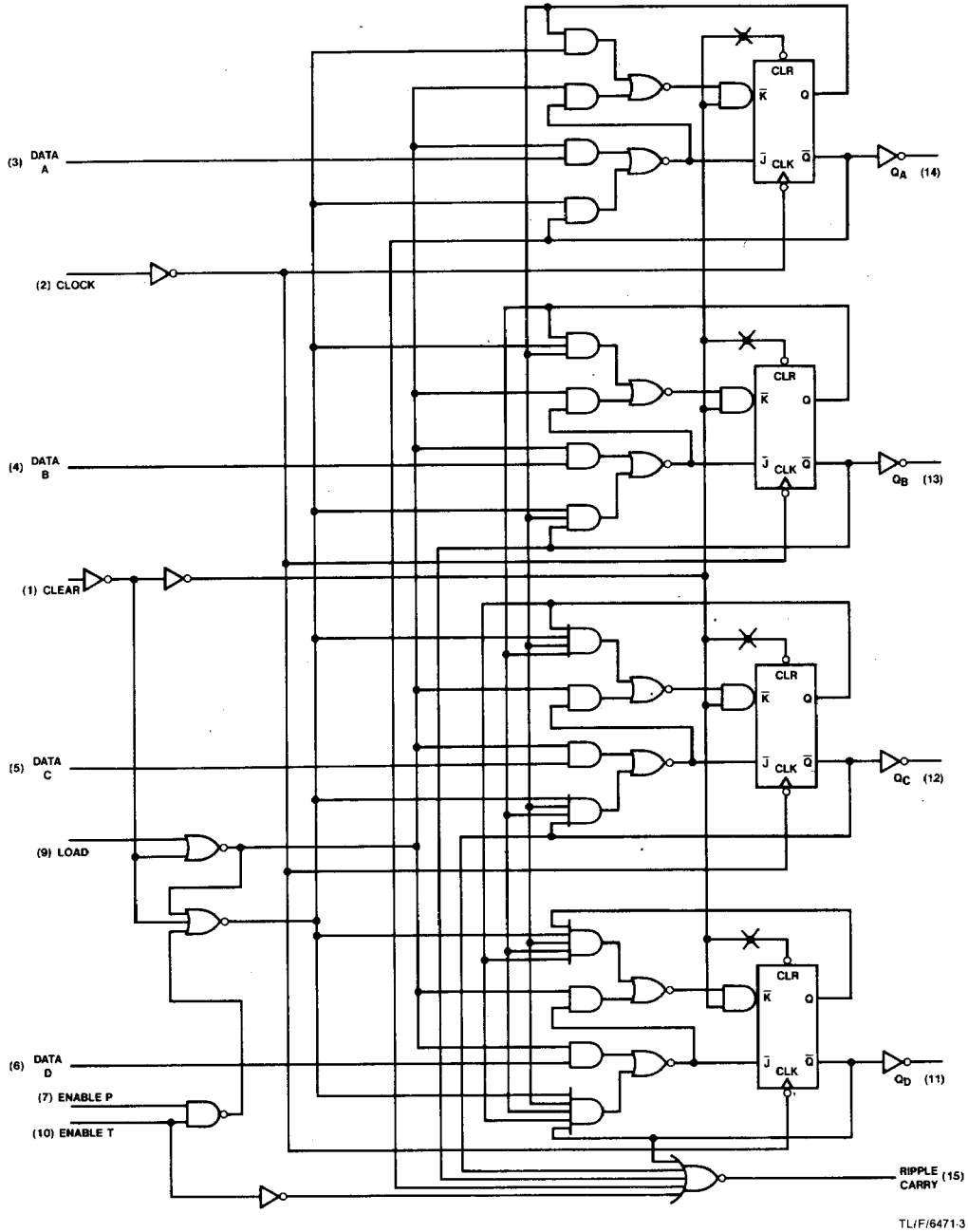
✖ S160 option

Logic Diagrams (Continued)

S161, S163



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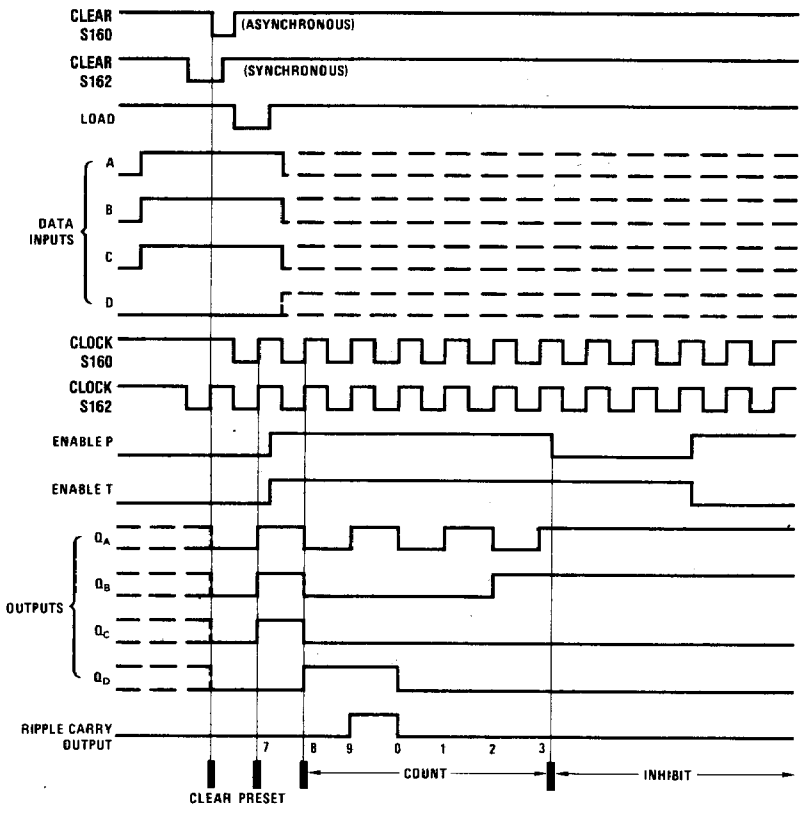
✕ S161 option

Timing Diagrams

S160, S162 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequences



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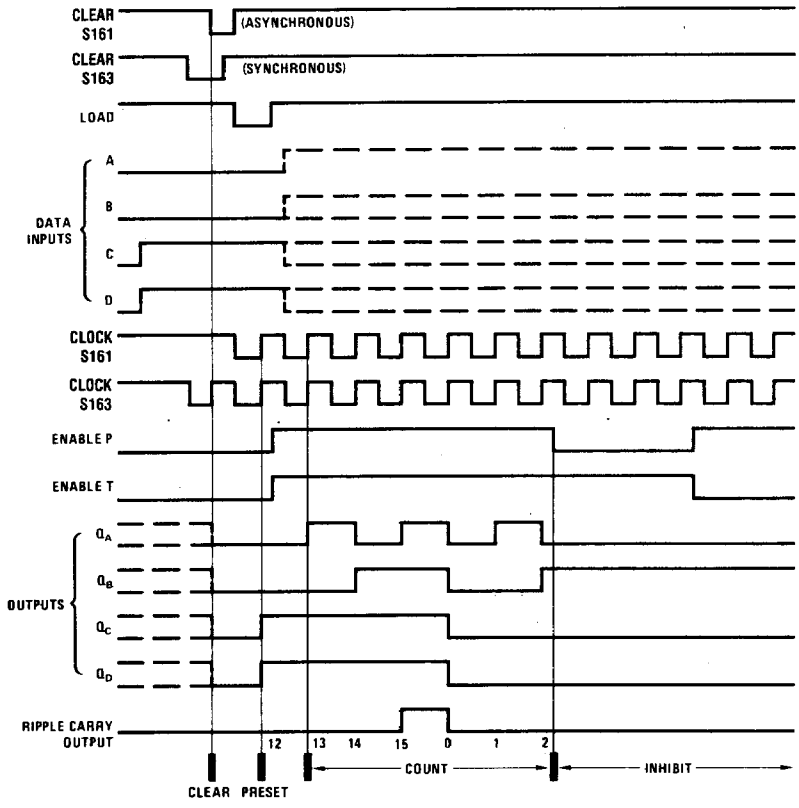
Sequence:

(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

Timing Diagrams (Continued)

S161, S163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



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Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

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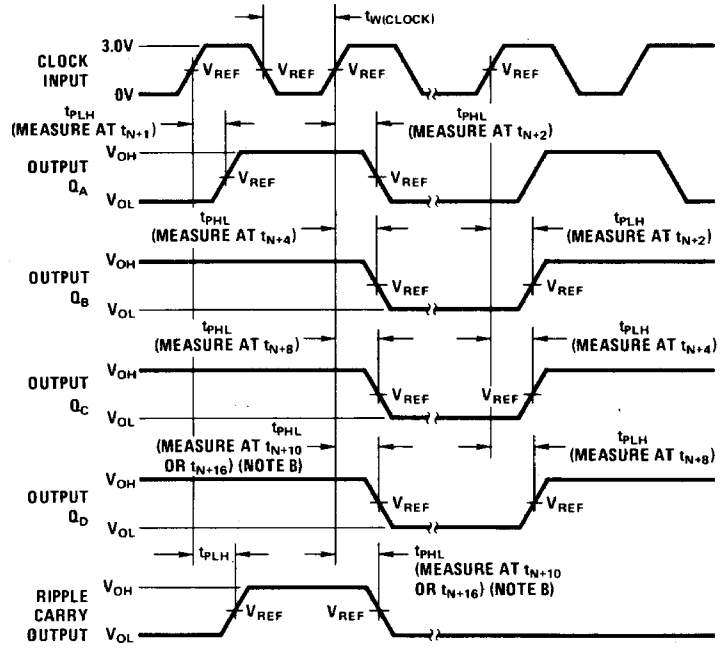
Parameter Measurement Information

SWITCHING TIME WAVEFORMS



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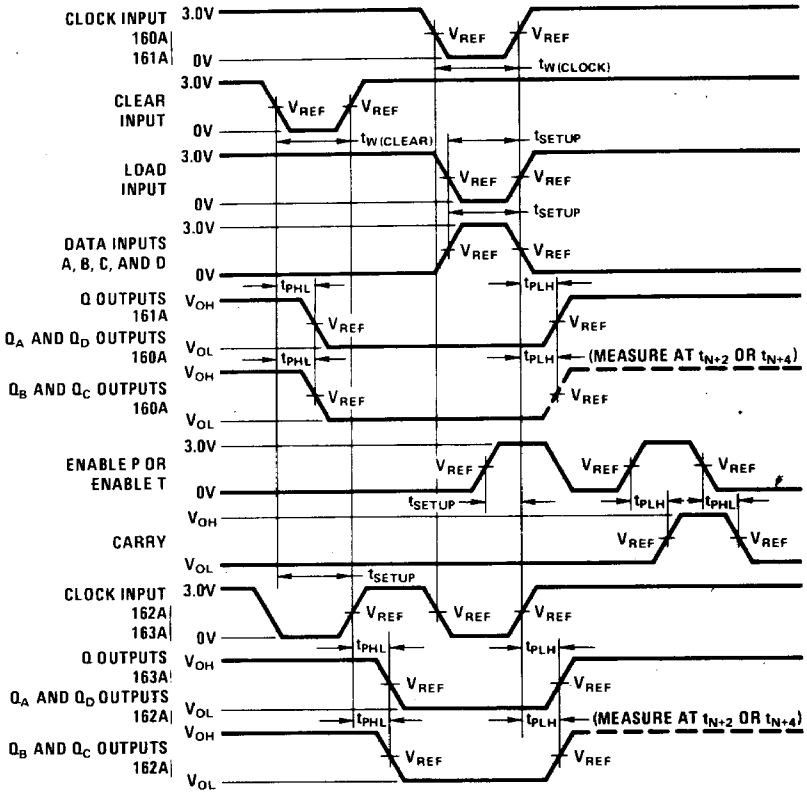
Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for S160, S162 and at t_{n+16} for S161, S163 where t_n is the bit time when all outputs are low.

Note C: For S160 through S163, $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

SWITCHING TIME WAVEFORMS



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Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S160 through S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: For S160 through S163, $V_{REF} = 1.5V$.

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