



CY54/74FCT163T

4-Bit Binary Counter

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.8 ns max. (Com'l),
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$

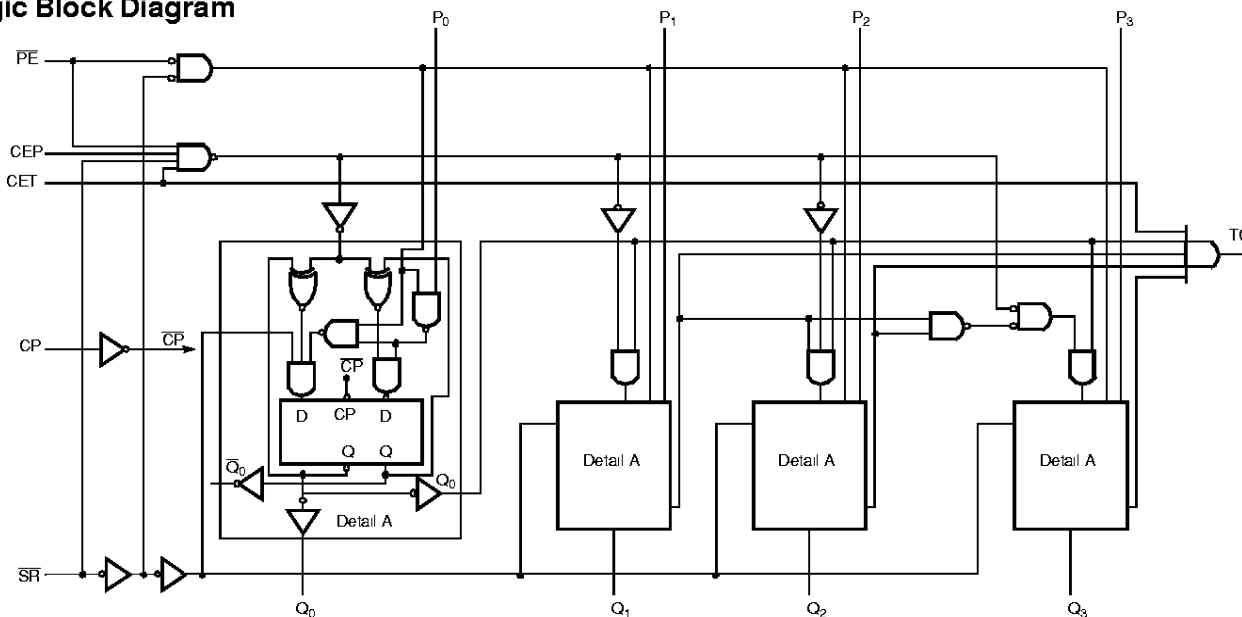
- Sink current 64 mA (Com'l), 32 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)

Functional Description

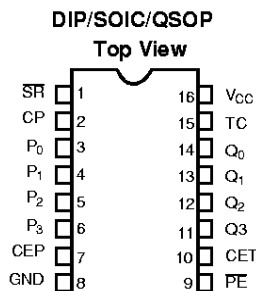
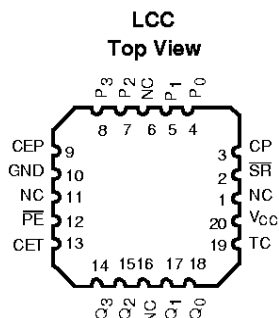
The FCT163T is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The FCT163T has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



Pin Configurations



Function Table^[1]

Inputs				Action on the Rising Clock Edge(s)
SR	PE	CET	CEP	
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P_n, Q_n)
H	H	H	H	Count (Incremental)
H	H	L	X	No Charge (Hold)
H	H	X	L	No Charge (Hold)

Pin Description

Name	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
\overline{SR}	Synchronous Reset Input (Active LOW)
P	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q	Flip-Flop Outputs
TC	Terminal Count Output

Maximum Ratings^[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation.....	0.5W
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	All	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0		V	
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3	V	
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3	V	
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V	
V _{IL}	Input LOW Voltage				0.8	V	
V _H	Hysteresis ^[6]	All inputs		0.2		V	
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V	
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA	
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA	
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA	
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA	
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA	

Notes:

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V ^[8] f ₁ =0, Outputs Open	0.2	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, CEP=CET=PE=GND, SR=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₀ =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, CEP=CET=PE=GND, SR=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., f ₀ =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =5 MHz, CEP=CET=PE=GND, SR=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	1.2	3.4	mA
		V _{CC} =Max., f ₀ =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =5 MHz, CEP=CET=PE=GND, SR=V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.6	3.2 ^[11]	mA
		V _{CC} =Max., f ₀ =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f ₁ =5 MHz, CEP=CET=PE=GND, SR=V _{CC} , V _{IN} =3.4V or V _{IN} =GND	2.9	8.2 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
11. All currents are in milliamps and all frequencies are in megahertz.
Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range

Parameter	Description	CY54FCT163T		CY74FCT163CT		Unit	Fig. No. ^[13]
		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Q (PE Input HIGH)	2.0	11.5	1.5	5.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to TC (PE Input LOW)	2.0	10.0	1.5	5.2	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to TC	2.0	16.5	1.5	7.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CET to TC	1.5	9.0	1.5	4.4	ns	1, 5
t _S	Set-Up Time, HIGH or LOW P to CP	5.5		3.5		ns	4
t _H	Hold Time, HIGH or LOW P to CP	2.0		1.5		ns	4
t _{SU}	Set-Up Time HIGH or LOW PE or SR to CP	13.5		7.6		ns	4
t _H	Hold Time HIGH or LOW PE or SR to CP	1.5		1.0		ns	4
t _{SU}	Set-Up Time HIGH or LOW CEP or CET to CP	13.0		7.6		ns	4
t _H	Hold Time HIGH or LOW CEP or CET to CP	0		0		ns	4
t _W	Clock Pulse Width (Load) HIGH or LOW	5.0		4.0		ns	5
t _W	Clock Pulse Width(Count) HIGH or LOW	8.0		5.0		ns	5

Notes:

- 12. Minimum limits are guaranteed but not tested on Propagation Delays.
- 13. See "Parameter Measurement Information" in the General Information section.

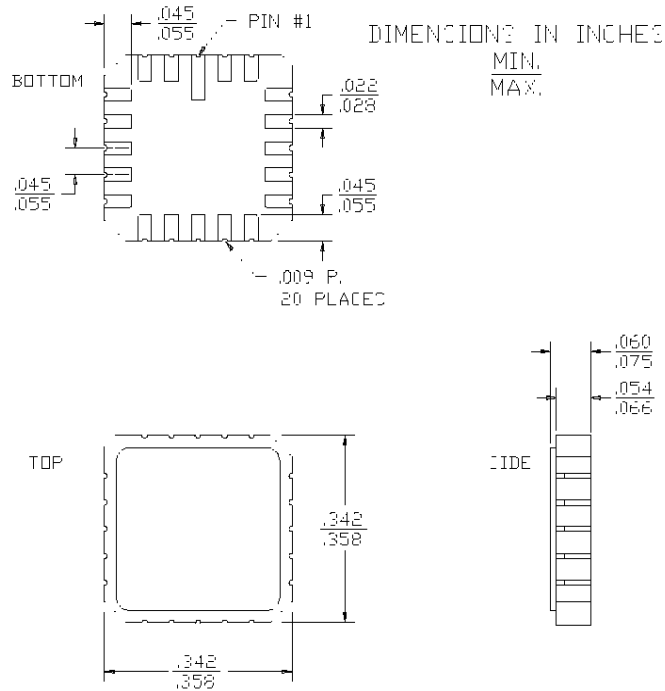
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT163CTQC	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY54FCT163CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
11.5	CY54FCT163TLMB	L61	20-Square Leadless Chip Carrier	Military

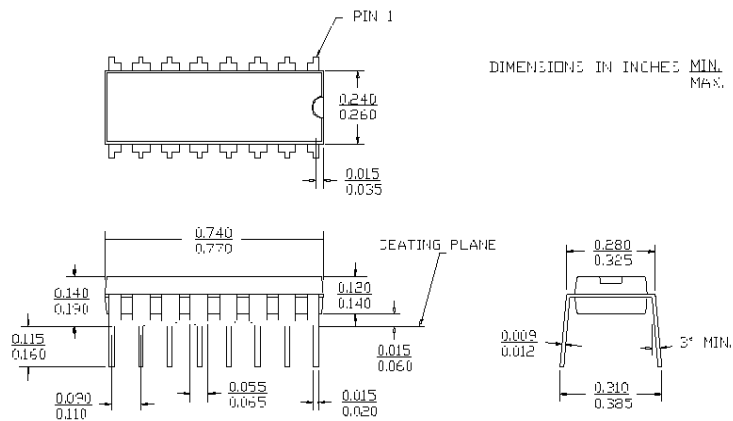
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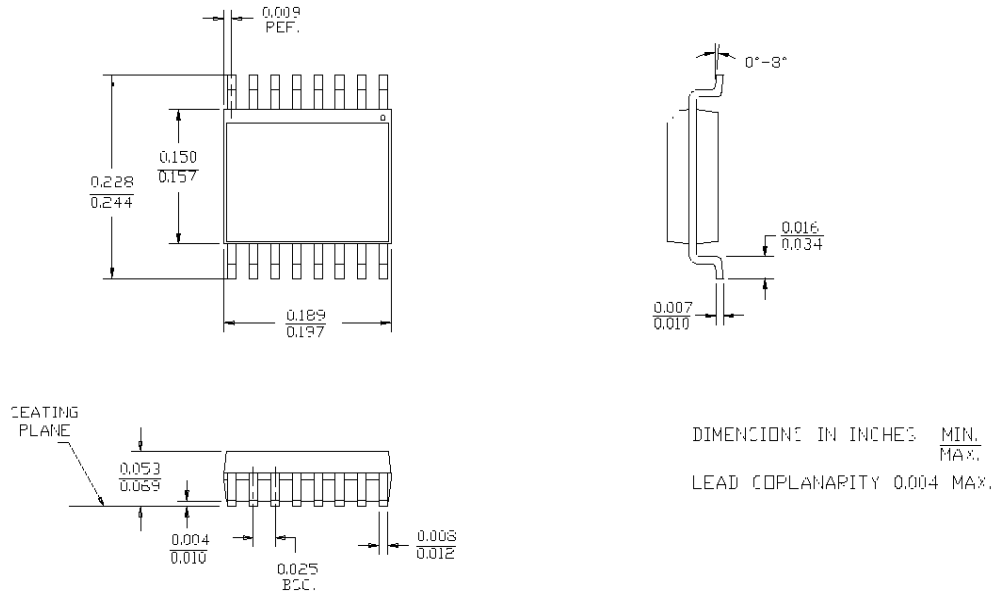
Package Diagrams

20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



16-Lead (300-Mil) Molded DIP P1



Package Diagrams (continued)
16-Lead Quarter Size Outline Q1

16-Lead Molded SOIC S1
