

# MC14018B

## Pre-settable Divide-By-N Counter

The MC14018B contains five Johnson counter stages which are asynchronously pre-settable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Pre-setting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective Q outputs (inverted). A logic 1 on the reset input will cause all Q outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate Q outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 3.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

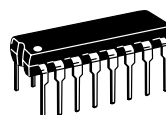
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



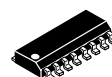
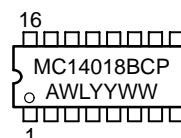
ON Semiconductor

<http://onsemi.com>

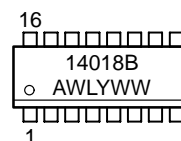
### MARKING DIAGRAMS



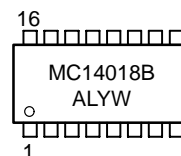
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14018BCP	PDIP-16	2000/Box
MC14018BD	SOIC-16	48/Rail
MC14018BDR2	SOIC-16	2500/Tape & Reel
MC14018BF	SOEIAJ-16	See Note 1.
MC14018BFEL	SOEIAJ-16	See Note 1.



1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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## PIN ASSIGNMENT

D <sub>in</sub>	1	●	16	V <sub>DD</sub>
JAM 1	2		15	R
JAM 2	3		14	C
$\bar{Q}2$	4		13	$\bar{Q}5$
$\bar{Q}1$	5		12	JAM 5
$\bar{Q}3$	6		11	$\bar{Q}4$
JAM 3	7		10	PE
V <sub>SS</sub>	8		9	JAM 4

## FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\bar{Q}_n$
	0	0	X	$\bar{Q}_n$
	0	0	X	$\bar{D}_n^*$
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

\* $\bar{D}_n$  is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage “0” Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  “1” Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	µAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (0.3 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.7 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.0 µA/kHz) f + I <sub>DD</sub>							µAdc	

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (8.)	Max	
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 102 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 72 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	310 120 85	620 240 170	ns
Reset to $\bar{Q}$ $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$		5.0 10 15	— — —	370 150 100	740 300 200	ns
Preset Enable to $\bar{Q}$ $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 325 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 81 \text{ ns}$		5.0 10 15	— — —	370 150 100	740 300 200	ns
Setup Time Data (Pin 1) to Clock	$t_{su}$	5.0 10 15	200 100 80	0 0 0	— — —	ns
Jam Inputs to Preset Enable		5.0 10 15	200 100 80	0 0 0	— — —	ns
Data (Jam Inputs)–to–Preset Enable Hold Time	$t_h$	5.0 10 15	540 500 480	270 250 240	— — —	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	400 200 160	200 100 80	— — —	ns
Reset or Preset Enable Pulse Width	$t_{WH}$	5.0 10 15	290 130 110	145 65 55	— — —	ns
Clock Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	No Limit			ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.5 6.5 8.0	1.25 3.25 4.0	MHz

7. The formulas given are for the typical characteristics only at 25°C.

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

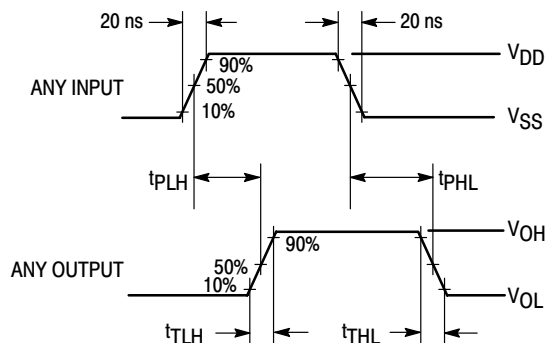
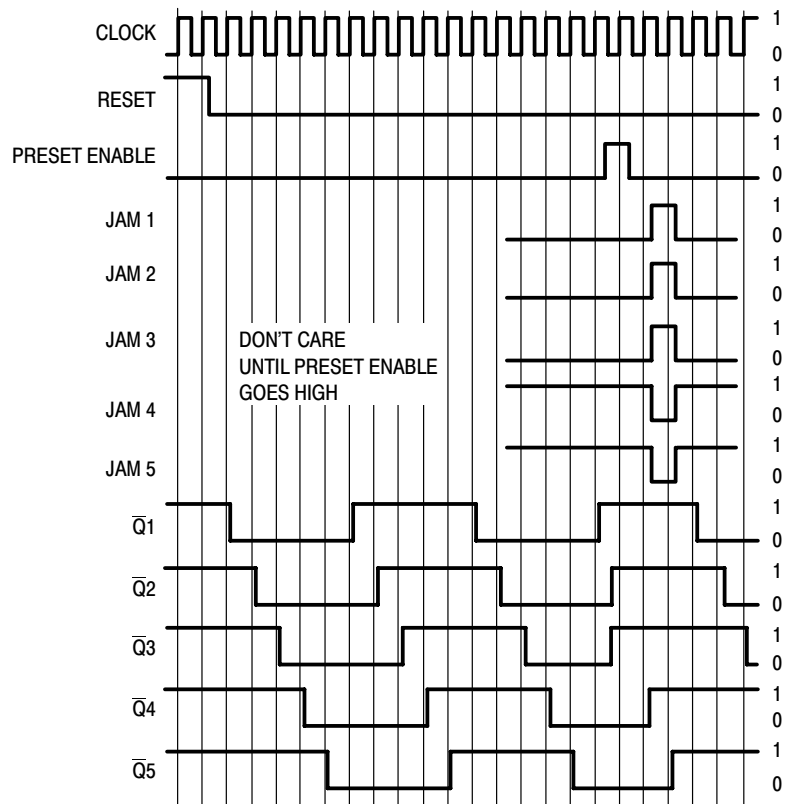


Figure 1. Switching Time Waveforms

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**TIMING DIAGRAM**  
( $\bar{Q}5$  Connected to Data Input)



## FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	$\bar{Q}5$ $\bar{Q}4$ $\bar{Q}3$ $\bar{Q}2$ $\bar{Q}1$	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	$Q5 \cdot Q4$ $Q4 \cdot Q3$ $Q3 \cdot Q2$ $Q2 \cdot Q1$	Gate package needed to provide AND function. Counter Skips all 1's state

## LOGIC DIAGRAM

