ADSANTEC
Ultra High-Speed Mixed Signal ASICs

*Advanced Science And Novel Technology Company, Inc.*
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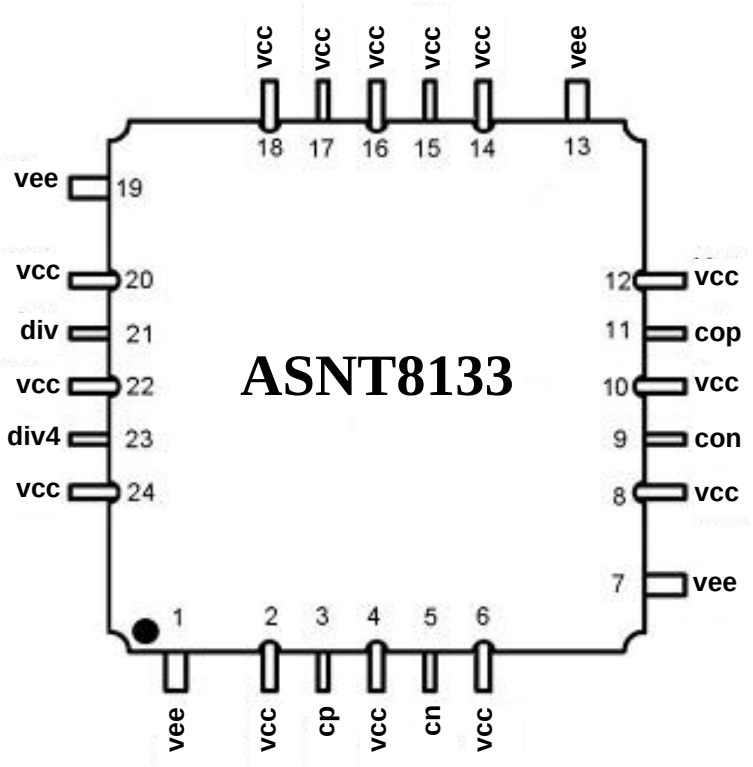
# ASNT8133-KMC
# DC-50*GHz* High-Speed Clock Divider by 1, 2, or 4

- Wide input clock frequency range from DC to 50*GHz*
- Selectable Forwarded, Divided-by-2, or Divided-by-4 output
- 50% duty cycle of the divided clock signals
- Fully differential CML input interface
- Fully differential CML output interface with 400*mV* single-ended swing
- CMOS 3.3*V* control signals
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 845*mW* at full operational speed
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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# DESCRIPTION

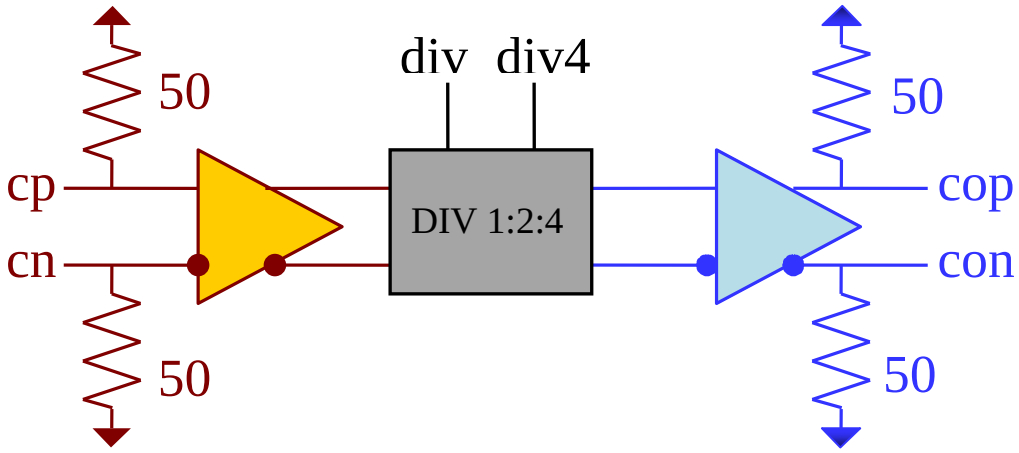


*Fig. 1. Functional Block Diagram*

ASNT8133-KMC is a high-speed, low-power divider by-1, by-2, or by-4 with increased sensitivity. The part shown in Fig. 1 accepts a CML input clock signal cp/cn with the speed from DC to maximum operational frequency and provides a clean 50% duty cycle output signal cop/con with its frequency defined by the states of CMOS level div and div4 control signals as shown in Table 1.

*Table 1. Clock frequency division control signals*

| div | div4 | Output Frequency |
|---|---|---|
| "0" | x | Forwarded, no division |
| "1" | "0" | Divided by 2 |
| "1" | "1" | Divided by 4 |

The part's high-speed I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

# POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V* =ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50Ohm termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

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# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 0.92 | *W* |
| RF Input Voltage Swing (SE) | | 1.0 | *V* |
| Case Temperature | | +90 | *°C* |
| Storage Temperature | -40 | +100 | *°C* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| cp | 3 | CML input | Differential clock input with internal SE 50*Ohm* termination to vcc |
| cn | 5 | | |
| cop | 11 | CML output | Differential clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| con | 9 | | |
| **Static I/Os** | | | |
| div | 21 | CMOS Input | Output clock frequency select signals. Pull-up to vcc |
| div4 | 23 | | |
| **Supply and Termination Voltages** | | | |
| **Name** | **Description** | | **Pin Number** |
| vcc | Positive power supply (+3.3*V* or 0*V*) | | 2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24 |
| vee | Negative power supply (0*V* or -3.3*V*) | | 1, 7, 13, 19 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.1 | -3.3 | -3.5 | *V* | ±6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | | 255 | | *mA* | |
| Power consumption | | 845 | | *mW* | |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **HS Input Clock (cp/cn)** | | | | | |
| Maximum Frequency | 50 | | | *GHz* | |
| Swing | 120 | | 800 | *mV* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.8 | vcc-0.2 | vcc | *mV* | Must match for both inputs |
| **Output Divided Clock (cop/con)** | | | | | |
| Maximum Forwarded Frequency | 25 | | | *GHz* | div = "0" |
| Maximum Divided Frequency | 25 | | | *GHz* | div = "1" |
| Logic "1" level | | vcc | | *V* | |
| Logic "0" level | | vcc-0.4 | | *V* | With external 50*Ohm* termination |
| Duty cycle | 45 | 50 | 55 | *%* | |
| Additive Jitter | | TBD | | *ps* | Peak-to-peak |
| **Divide Ration Control Signals (div, div4)** | | | | | |
| Logic "1" level | $V_{CC}$-0.4 | | | *V* | |
| Logic "0" level | | | $V_{EE}$+0.4 | *V* | |

# PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8133-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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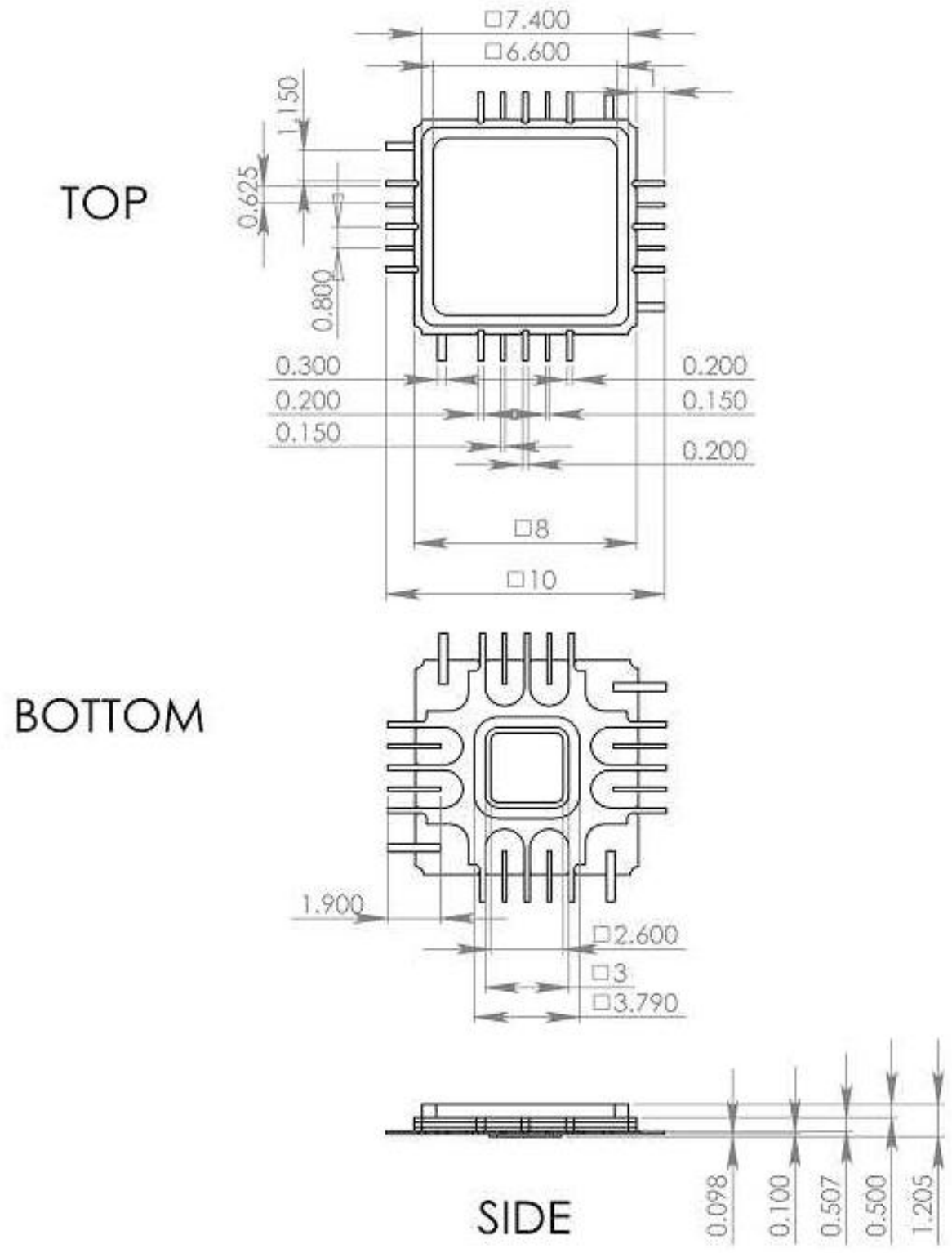


*Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)*

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.2.2 | 02-2020 | Updated Package Information |
| 1.1.2 | 07-2019 | Updated Letterhead |
| 1.1.1 | 01-2016 | Revised Description section<br>Added content to Electrical Characteristics table |
| 1.0.1 | 07-2015 | First release |
| 1.0.0 | 03-2015 | Preliminary release |