National Semiconductor

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MM54HC190/MM74HC190 Synchronous Decade Up/Down Counters with Mode Control MM54HC191/MM74HC191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HC191/MM74HC191 are 4-bit binary counters and the MM54HC190/MM74HC190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

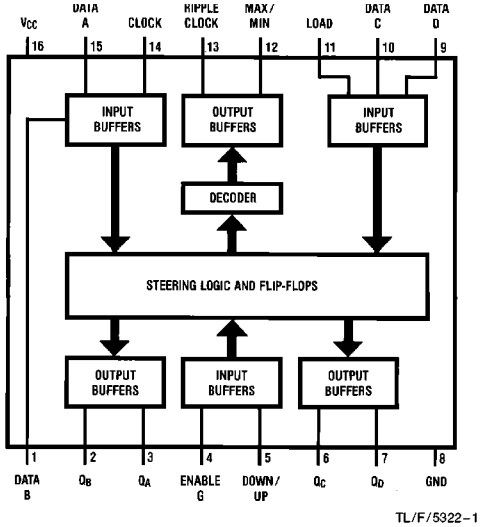
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock input
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



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Top View

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

Order Number MM54HC190/191 or MM74HC190/191

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Typ	Units
f_{MAX}	Maximum Clock Frequency			40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D	27	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock	16	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D	24	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock	29	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock	22	ns
t_W	Minimum Clock, Clear or Load Input Pulse Width			10	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
					Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			2.0V	9	4.0	3.5	2.6	MHz
				4.5V	30	20	16	13	MHz
				6.0V	36	24	19	15	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D	2.0V	80	220	275	330	ns
				4.5V	27	44	55	66	ns
				6.0V	21	37	47	56	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D	2.0V	71	200	250	300	ns
				4.5V	25	40	50	60	ns
				6.0V	19	34	43	51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock	2.0V	44	125	155	190	ns
				4.5V	25	25	31	38	ns
				6.0V	14	21	26	32	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D	2.0V	83	215	270	325	ns
				4.5V	29	43	54	65	ns
				6.0V	22	37	46	55	ns

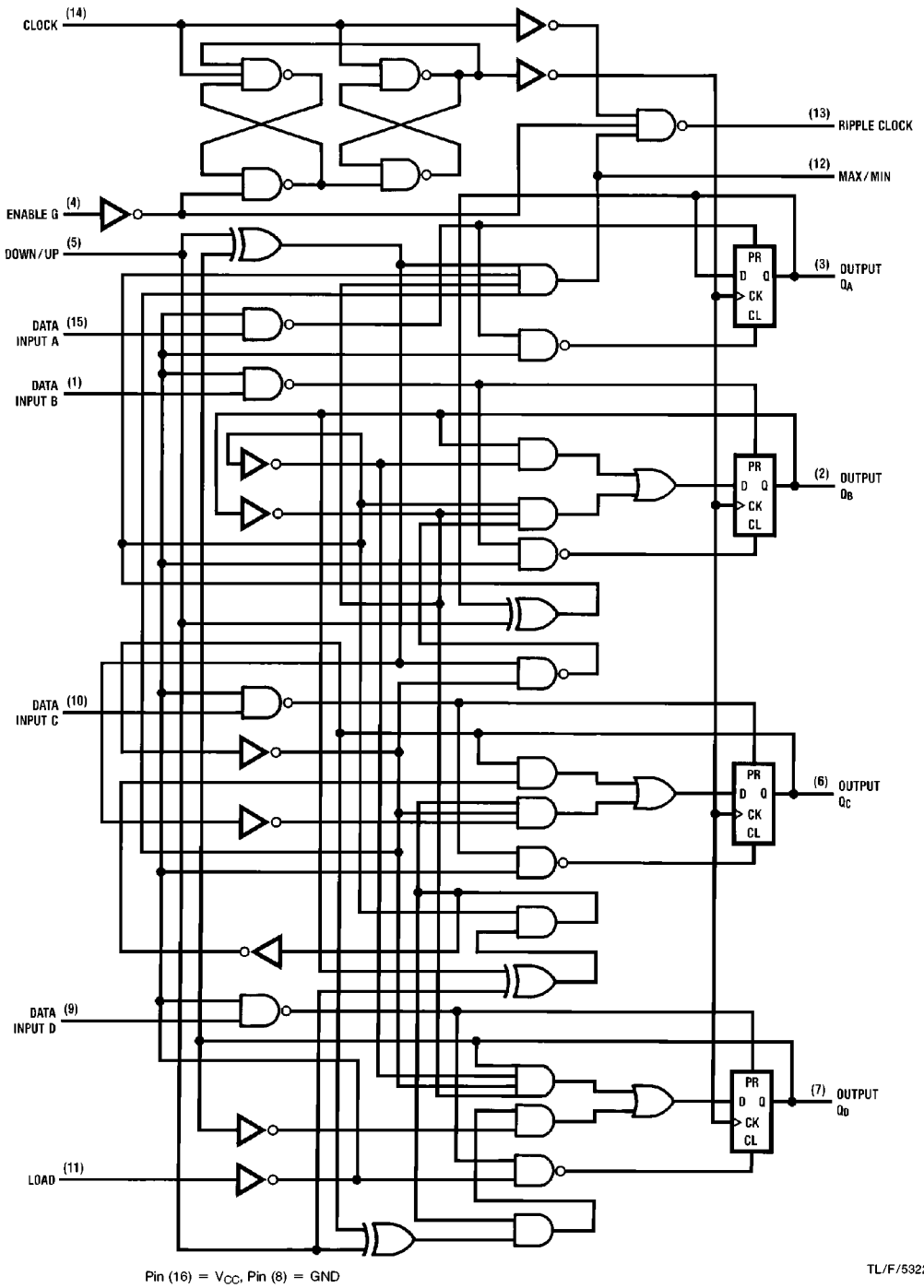
AC Electrical Characteristics (Continued)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		2.0V	125	255	320	385	ns
					4.5V	41	51	64	77	ns
					6.0V	31	43	54	65	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		2.0V	90	210	265	315	ns
					4.5V	30	42	53	63	ns
					6.0V	24	36	45	54	ns
t_{PLH},t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		2.0V	88	190	240	285	ns
					4.5V	30	38	48	57	ns
					6.0V	23	32	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		2.0V	50	125	155	190	ns
					4.5V	18	25	31	38	ns
					6.0V	14	21	26	32	ns
t_W	Minimum Clock, Load or Clear Input Pulse Width				2.0V	36	125	155	190	ns
					4.5V	12	25	31	38	ns
					6.0V	9	21	26	32	ns
t_S	Minimum Setup Time	Data	Load		2.0V	50	100	125	150	ns
					4.5V	14	20	25	30	ns
					6.0V	10	17	21	26	ns
t_H	Data Hold Time	Load	Data		2.0V	−16	25	30	40	ns
					4.5V	−3	5	6	8	ns
					6.0V	−2	5	6	7	ns
t_S	Minimum Setup Time	Down/Up	Clock		2.0V	62	150	190	225	ns
					4.5V	18	30	38	48	ns
					6.0V	14	26	33	38	ns
t_H	Minimum Hold Time	Clock	Down/Up		2.0V	−23	0	0	0	ns
					4.5V	−5	0	0	0	ns
					6.0V	−4	0	0	0	ns
t_S	Minimum Setup Time	Enable	Clock		2.0V	28	100	125	150	ns
					4.5V	10	20	25	30	ns
					6.0V	7	17	21	26	ns
t_H	Minimum Hold Time	Clock	Enable		2.0V	−11	0	0	0	ns
					4.5V	−5	0	0	0	ns
					6.0V	−3	0	0	0	ns
t_{rem}	Minimum Removal Time	Load	Clock		2.0V	1	25	30	40	ns
					4.5V	1	5	6	8	ns
					6.0V	0	5	6	7	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				2.0V	30	75	95	110	s
					4.5V	10	15	19	22	ns
					6.0V	9	13	16	19	ns
t_W	Minimum Load Pulse Width				2.0V	53	100	125	150	ns
					4.5V	15	20	25	30	ns
					6.0V	12	17	21	26	ns
C_{IN}	Input Capacitance					5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)					35				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

'HC190 Decade Counters



Pin (16) = V_{CC}, Pin (8) = GND

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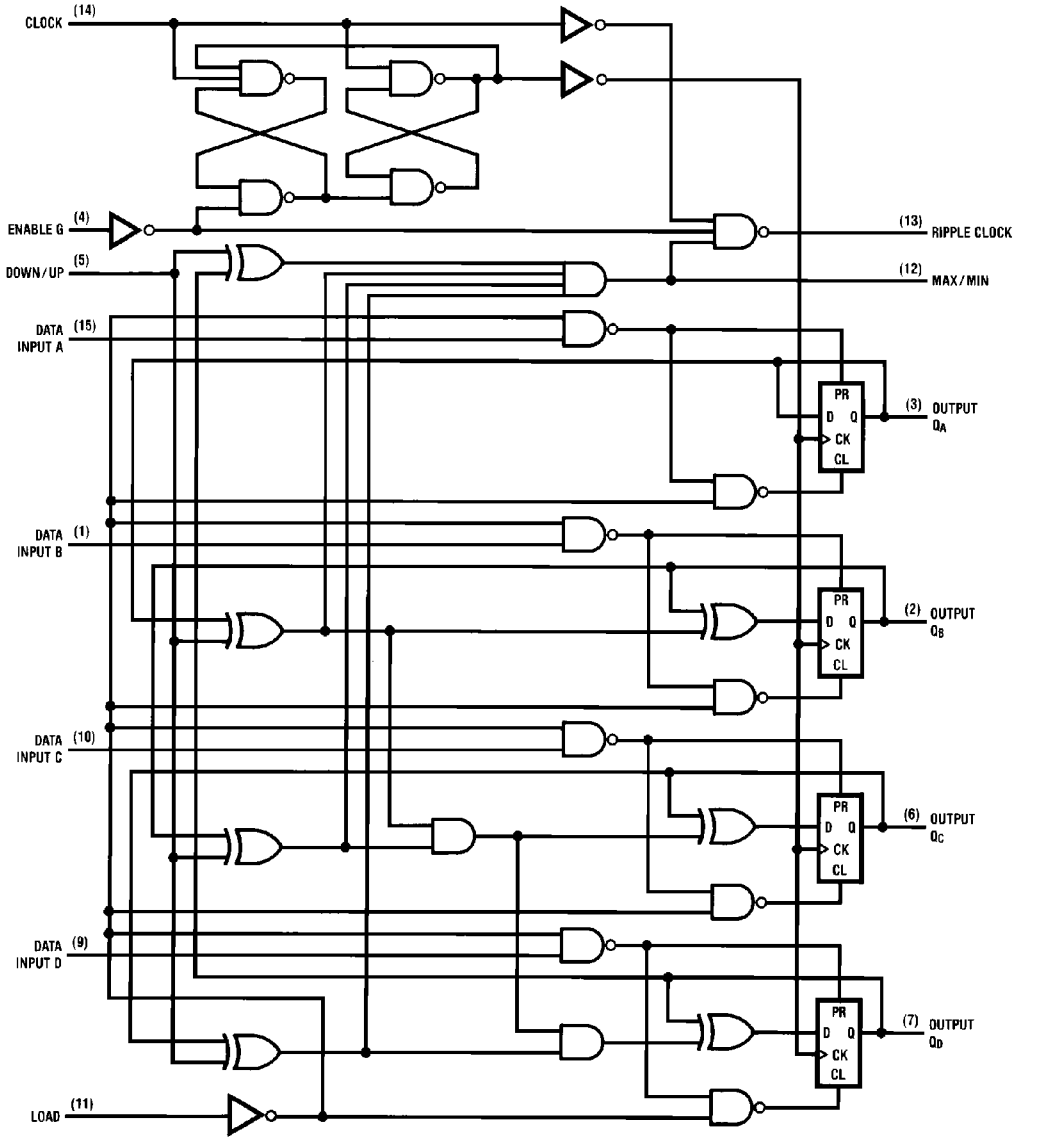
Logic Diagrams (Continued)

'HC191 Binary Counters



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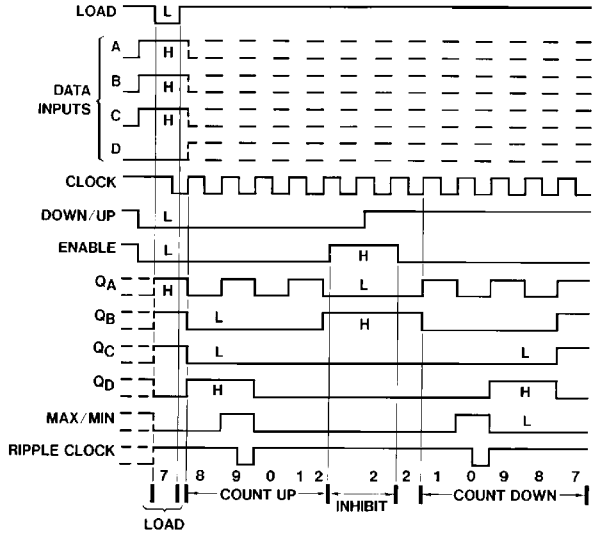
Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

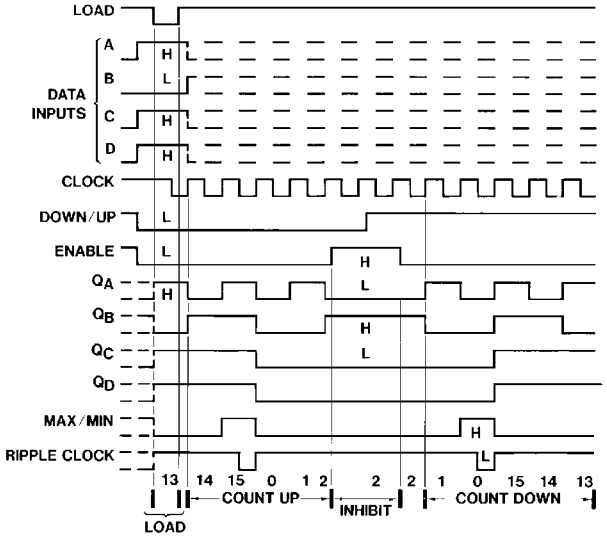
'HC190 Synchronous Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/5322–4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

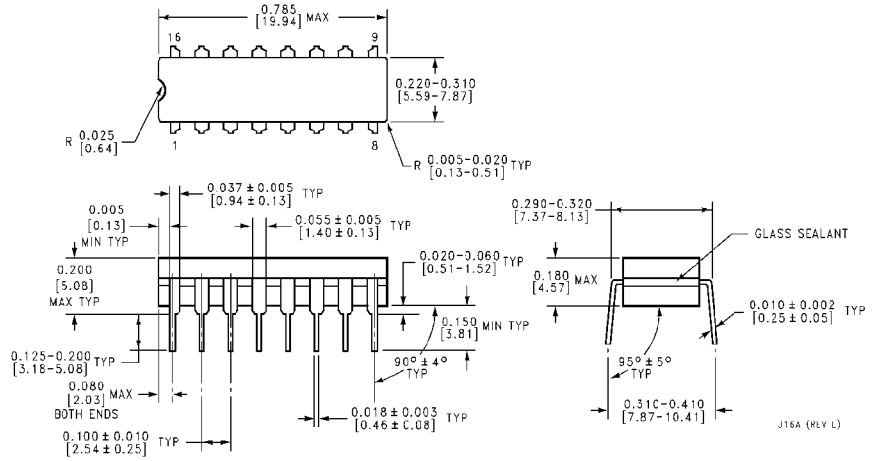
'HC191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



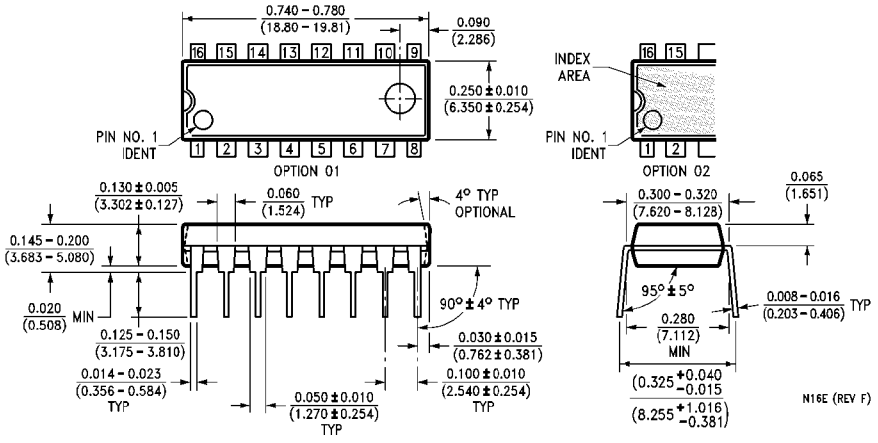
TL/F/5322–5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

Physical Dimensions inches (millimeters)



Order Number MM54HC190J, MM54HC191J, MM74HC190J, or MM74HC191J
NS Package J16A



Order Number MM74HC190N or MM74HC191N
NS Package N16E

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