ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

RoHS 2002/95/EC

NTE74LS90
Integrated Circuit
TTL– Decade Counter
14–Lead DIP

Description:

The NTE74LS90 is a monolithic counter in a 14–Lead DIP type package that contains four master–slave flip–flops and additional gating to provide a divide–by–two counter and a three–stage binary counter for which the count cycle length is divide–by–five.

The counter has a gated zero reset and also has gated set–to–nine inputs for use in BDC nine's complement applications.

To use the maximum count length (decade or four–bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate Function Table. A symmetrical divide–by–ten count can be obtained from the counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide–by–ten square wave at output Q_A.

Features:

- Typical Power Dissipation: 145mW

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1) 7V
Input Voltage
R Inputs 7V
A and B Inputs 5.5V
Operating Free–Air Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . –65° to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operating Conditions:

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	V
HIGH Level Output Current		I_{OH}	–	–	–400	µA
LOW Level Output Current		I_{OL}	–	–	8	mA
Count Frequency	A Input	f_{count}	0	–	32	MHz
	B Input		0	–	16	MHz
Pulse Width	A Input	t_W	15	–	–	ns
	B Input		30	–	–	ns
	Reset Inputs		30	–	–	ns
Reset Inactive–State Setup Time		t_{su}	25	–	–	ns
Operating Free Air Temperature		T_A	0	–	70	°C

DC Electrical Characteristics: (T_A = 0° to +70°C, Note 2, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
HIGH Level Input Voltage	V_{IH}			2	–	–	V
LOW Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = Min, I_I = –18mA		–	–	–1.5	V
HIGH Level Output Voltage	V_{OH}	V_{CC} = Min, I_{OH} = –400μA, V_{IL} = Max, V_{IH} = 2V		2.7	3.4	–	V
LOW Level Output Voltage	V_{OL}	V_{CC} = Min, V_{IH} = 2V, V_{IL} – Max, Note 5	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current at Max Input Voltage	I_I	V_{CC} = Max, V_I = 7V	Any Reset	–	–	0.1	mA
		V_{CC} = Max, V_I = 5.5V	A Input	–	–	0.2	mA
			B Input	–	–	0.4	mA
HIGH Level Input Current	I_{IH}	V_{CC} = Max, V_I = 2.7V	Any Reset	–	–	20	μA
			A Input	–	–	40	μA
			B Input	–	–	80	μA
LOW Level Input Current	I_{IL}	V_{CC} = Max, V_I = 0.4V	Any Reset	–	–	–0.4	mA
			A Input	–	–	–2.4	mA
			B Input	–	–	–3.2	mA
Short–Circuit Output Current	I_{OS}	V_{CC} = Max, Note 4		–20	–	–100	mA
Supply Current	I_{CC}	V_{CC} = Max, Note 6		–	9	15	mA

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operating Conditions”.

Note 3. All typicals are at V_{CC} = +5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and duration of the short–circuit should not exceed one second

Note 5. Q_A outputs are tested at I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan–out capability.

Note 6. I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5V, and all other o=inputs grounded.

Switching Characteristics: (V_{CC} = +5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	From (Input) To (Output)	R_L = 2kΩ, C_L = 15pF			Unit
			Min	Typ	Max	
Maximum Clock Frequency	f_{MAX}	A to Q_A	32	42	–	MHz
		B to Q_B	16	–	–	MHz
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	A to Q_A	–	10	16	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	A to Q_A	–	12	18	ns
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	A to Q_D	–	32	48	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	A to Q_D	–	34	50	ns
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	B to Q_B	–	10	16	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	B to Q_B	–	14	21	ns
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	B to Q_C	–	21	32	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	B to Q_C	–	23	35	ns
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	B to Q_D	–	21	32	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	B to Q_D	–	23	35	ns

Switching Characteristics (Con't): (V_{CC} = +5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	From (Input) To (Output)	R_L = 2kΩ, C_L = 15pF			Unit
			Min	Typ	Max	
Propagation Delay Time LOW–to–HIGH Level Output	t_{PLH}	SET–9 to Q_A, Q_D	–	20	30	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	SET–9 to Q_B, Q_C	–	26	40	ns
Propagation Delay Time HIGH–to–LOW Level Output	t_{PHL}	SET–0 Any Q	–	26	40	ns

Function Tables:

BCD Count Sequence: (Note 7)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BCD Bi–Quinary: (Note 8)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care

Note 7. Output Q_A is connected to input B for BCD count.
Note 8. Output Q_D is connected to input A for bi–quinary count.

Function Tables (Cont'd):

Reset/Count Function Table:

Reset Inputs				Outputs			
R_0 (1)	R_0 (2)	R_9 (1)	R_9 (2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care

Pin Connection Diagram