FAIRCHILD SEMICONDUCTOR™

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# 74F579
# 8-Bit Bidirectional Binary Counter with 3-STATE Outputs

## General Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

## Features

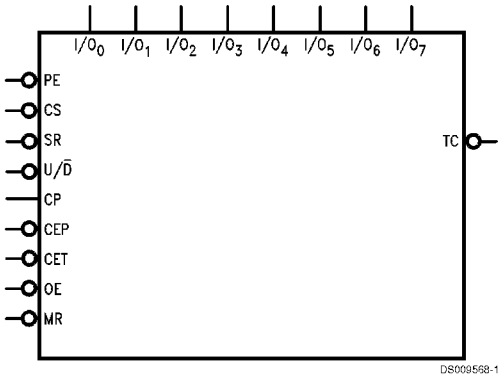
- Multiplexed 3-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typical
- Supply current 75 mA typical
- Guaranteed 4000V minimum ESD protection

## Ordering Code:

| Commercial | Package Number | Package Description |
|---|---|---|
| 74F579PC | N20A | 20-Lead (0.300" Wide) Molded Dual-In-Line |
| 74F579SC (Note 1) | M20B | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F579SJ (Note 1) | M20D | 20-Lead (0.300" Wide) Molded Small Outline, EIAJ |

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

## Logic Symbol

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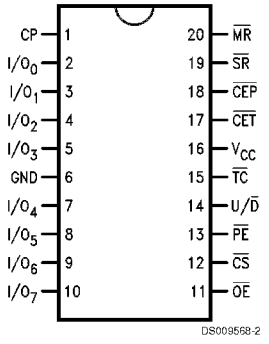
## Connection Diagram

**Pin Assignment for DIP and SOIC**

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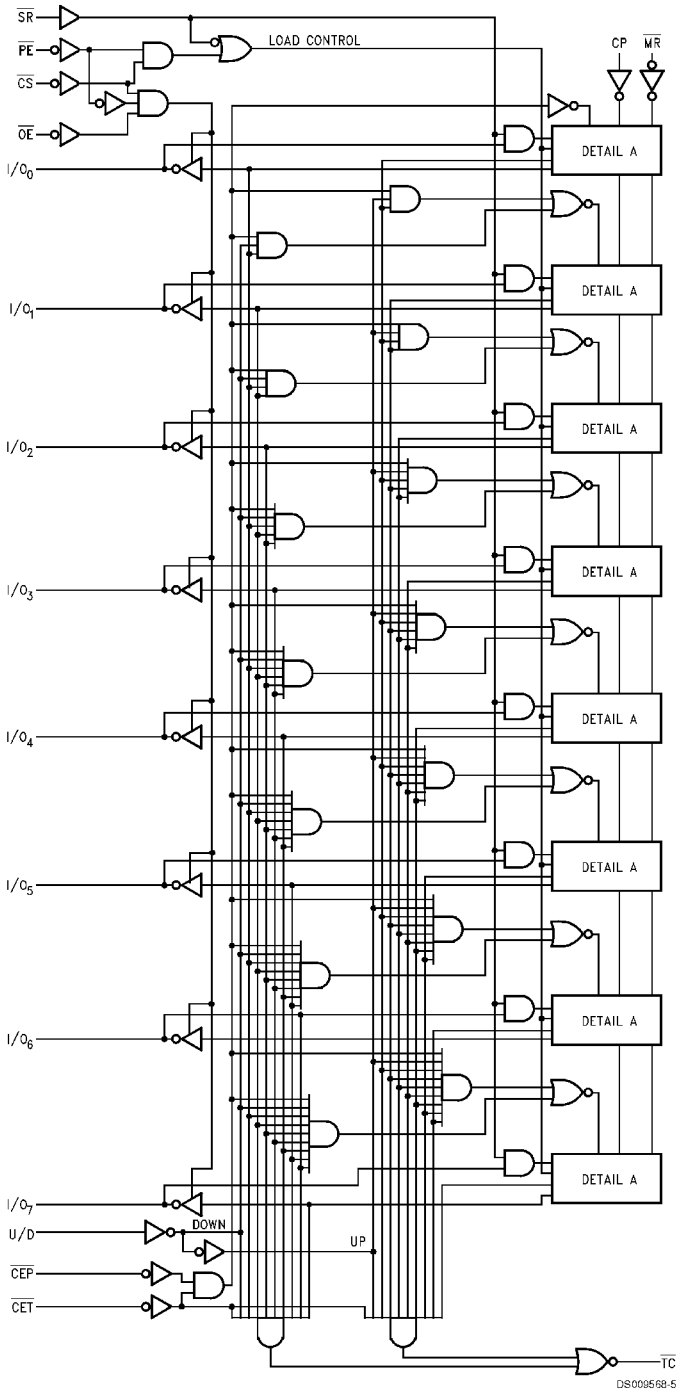
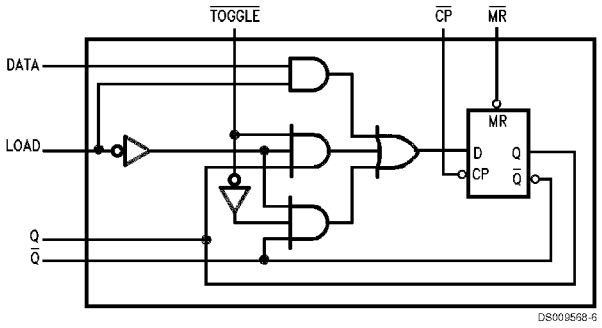
## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Logic Diagram (Continued)




$V_{CC}$ = Pin 16
GND = Pin 6
( ) = Pin Numbers

**Detail A**

## Unit Loading/Fan Out

| Pin Names | Description | 74F | |
|---|---|---|---|
| | | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
| $I/O_0$–$I/O_7$ | Data Inputs or | 3.5/0.333 | 70 µA/–0.2 mA |
| | 3-STATE Outputs | 75/15 | –3 mA/24 mA |
| $\overline{PE}$ | Parallel Enable Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $U/\overline{D}$ | Up-Down Count Control Input | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{MR}$ | Master Reset Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{SR}$ | Synchronous Reset Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{CEP}$ | Count Enable Parallel Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{CET}$ | Count Enable Trickle Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{CS}$ | Chip Select Input Active (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{OE}$ | Output Enable Input (Active LOW) | 0.25/0.333 | 5 µA/–0.2 mA |
| CP | Clock Pulse Input (Active Rising Edge) | 0.25/0.333 | 5 µA/–0.2 mA |
| $\overline{TC}$ | Terminal Count Output (Active LOW) | 25/12.5 | –1 mA/5 mA |

## Unit Loading/Fan Out (Continued)

## Function Table

| $\overline{MR}$ | $\overline{SR}$ | $\overline{CS}$ | $\overline{PE}$ | $\overline{CEP}$ | $\overline{CET}$ | U/$\overline{D}$ | $\overline{OE}$ | CP | Function |
|---|---|---|---|---|---|---|---|---|---|
| X | X | H | X | X | X | X | X | X | $I/O_a$ to $I/O_h$ in High Z ($\overline{PE}$ Disabled) |
| X | X | L | H | X | X | X | H | X | $I/O_a$ to $I/O_h$ in High Z |
| X | X | L | H | X | X | X | L | X | Flip-Flop Outputs Appear on I/O Lines |
| L | X | X | X | X | X | X | X | X | Asynchronous Reset for all Flip-Flops |
| H | L | X | X | X | X | X | X | ⌐ | Synchronous Reset for all Flip-Flops |
| H | H | L | L | X | X | X | X | ⌐ | Parallel Load all Flip-Flops |
| H | H | (Not LL) | | H | X | X | X | ⌐ | Hold |
| H | H | (Not LL) | | X | H | X | X | ⌐ | Hold ($\overline{TC}$ Held HIGH) |
| H | H | (Not LL) | | L | L | H | X | ⌐ | Count Up |
| H | H | (Not LL) | | L | L | L | X | ⌐ | Count Down |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immeterial
⌐ = LOW to HIGH Clock Transition
Not LL = $\overline{CS}$ and $\overline{PE}$ should never both be LOW voltage level at the same time.

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +175°C |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 3) | −0.5V to +7.0V |
| Input Current (Note 3) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Commercial | +4.5V to +5.5V |

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol | Parameter | | 74F Min | 74F Typ | 74F Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 74F 10% $V_{CC}$ | 2.4 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | |
| $V_{OL}$ | Output LOW Voltage | 74F 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 20 mA ($\overline{TC}$), $I_{OL}$ = 24 mA ($I/O_n$) |
| | | 74F 5% $V_{CC}$ | | | 0.5 | | | $I_{OL}$ = 20 mA ($\overline{TC}$), $I_{OL}$ = 24 mA ($I/O_n$) |
| $I_{IH}$ | Input HIGH Current | 74F | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V (Non-I/O Pins) |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | 74F | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V (Non-I/O Pins) |
| $I_{BVIT}$ | Input HIGH Current Breakdown (I/O) | 74F | | | 0.5 | mA | Max | $V_{IN}$ = 5.5V ($I/O_n$) |
| $I_{CEX}$ | Output HIGH Leakage Current | 74F | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | 74F | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Control | 74F | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{ZZ}$ | Bus Drainage Test | | | | 500 | µA | 0.0 | $V_{OUT}$ = 5.25V |
| $I_{IL}$ | Input LOW Current | | | | −0.2 | mA | Max | $V_{IN}$ = 0.5V (Non-I/O Pins) |
| $I_{IH}$ & $I_{OZH}$ | Output Leakage Current | | | | 70 | µA | Max | $V_{OUT}$ = 2.7V ($I/O_n$) |
| $I_{IL}$ & $I_{OZL}$ | Output Leakage Current | | | | −200 | µA | Max | $V_{OUT}$ = 0.5V ($I/O_n$) |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CCH}$ | Power Supply Current | | | 70 | 110 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | | 85 | 120 | mA | Max | $V_O$ = LOW |
| $I_{CCZ}$ | Power Supply Current | | | 85 | 125 | mA | Max | $V_O$ = HIGH Z |

## AC Electrical Characteristics

| Symbol | Parameter | 74F $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | | 74F $T_A$, $V_{CC}$ = Comm, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $f_{max}$ | Maximum Clock Frequency | 70 | 85 | | 80 | | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 5.0 | 7.5 | 3.0 | 8.0 | ns |
| $t_{PHL}$ | CP to $I/O_n$ | 5.0 | 8.0 | 11.5 | 5.0 | 11.5 | |
| $t_{PLH}$ | Propagation Delay | 5.0 | 7.5 | 11.5 | 5.0 | 12.0 | ns |
| $t_{PHL}$ | CP to $\overline{TC}$ | 5.0 | 7.0 | 11.5 | 5.0 | 12.0 | |
| $t_{PLH}$ | Propagation Delay | 4.5 | 7.0 | 9.0 | 4.5 | 10.0 | ns |
| $t_{PHL}$ | U/$\overline{D}$ to $\overline{TC}$ | 4.5 | 8.0 | 9.5 | 4.5 | 10.0 | |
| $t_{PLH}$ | Propagation Delay | 2.5 | 3.8 | 6.0 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | $\overline{CEP}$ or $\overline{CET}$ to $\overline{TC}$ | 3.5 | 6.0 | 8.0 | 3.5 | 8.5 | |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to $I/O_n$ | 5.0 | 7.5 | 10.0 | 5.0 | 10.0 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to TC | 6.5 | 10.0 | 13.0 | 6.5 | 13.5 | ns |
| $t_{PZH}$ | Output Enable Time | 3.0 | 5.0 | 8.5 | 3.0 | 9.0 | ns |
| $t_{PZL}$ | $\overline{CS}$ or $\overline{PE}$ to I/O | 5.5 | 8.0 | 10.5 | 5.5 | 11.5 | |
| $t_{PHZ}$ | Output Disable Time | 2.0 | 5.0 | 8.5 | 2.0 | 9.0 | ns |
| $t_{PLZ}$ | $\overline{CS}$ or $\overline{PE}$ to I/O | 2.0 | 4.5 | 8.0 | 2.0 | 8.5 | |
| $t_{PZH}$ | Output Enable Time | 3.0 | 5.0 | 8.0 | 3.0 | 8.5 | ns |
| $t_{PZL}$ | $\overline{OE}$ to $I/O_n$ | 5.0 | 8.0 | 11.0 | 5.0 | 12.0 | |
| $t_{PHZ}$ | Output Disable Time | 2.0 | 4.0 | 6.5 | 2.0 | 6.5 | ns |
| $t_{PLZ}$ | $\overline{OE}$ to $I/O_n$ | 2.0 | 4.0 | 6.0 | 2.0 | 6.5 | |

## AC Operating Requirements

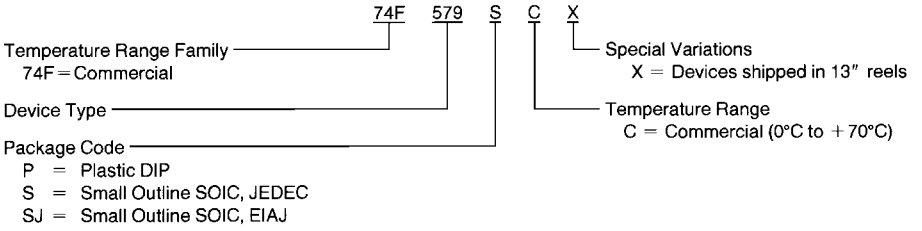
| Symbol | Parameter | 74F $T_A$ = +25°C, $V_{CC}$ = +5.0V | | | 74F $T_A$, $V_{CC}$ = Comm | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_s$(H) | Setup Time | 4.0 | | | 4.0 | | ns |
| $t_s$(L) | $I/O_n$ to CP | 4.0 | | | 4.0 | | |
| $t_h$(H) | Hold Time | 0.0 | | | 0.0 | | ns |
| $t_h$(L) | $I/O_n$ to CP | 0.0 | | | 0.0 | | |
| $t_s$(H) | Setup Time | 9.5 | | | 9.5 | | ns |
| $t_s$(L) | $\overline{PE}$ , $\overline{CS}$ or $\overline{SR}$ to CP | 9.5 | | | 9.5 | | |
| $t_h$(H) | Hold Time | 0.0 | | | 0.0 | | ns |
| $t_h$(L) | $\overline{PE}$ , $\overline{CS}$ or $\overline{SR}$ to CP | 0.0 | | | 0.0 | | |
| $t_s$(H) | Setup Time | 6.5 | | | 6.5 | | ns |
| $t_s$(L) | $\overline{CET}$ or $\overline{CEP}$ to CP | 9.5 | | | 9.5 | | |
| $t_h$(H) | Hold Time | 0.0 | | | 0.0 | | ns |
| $t_h$(L) | $\overline{CET}$ or $\overline{CEP}$ to CP | 0.0 | | | 0.0 | | |
| $t_s$(H) | Setup Time | 9.0 | | | 9.5 | | ns |
| $t_s$(L) | U/$\overline{D}$ to CP | 9.0 | | | 9.5 | | |
| $t_h$(H) | Hold Time | 0.0 | | | 0.0 | | ns |
| $t_h$(L) | U/$\overline{D}$ to CP | 0.0 | | | 0.0 | | |

## AC Operating Requirements (Continued)

| Symbol | Parameter | 74F $T_A$ = +25°C $V_{CC}$ = +5.0V | | | 74F $T_A$, $V_{CC}$ = Comm | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_w(H)$ | Clock Pulse Width | 4.5 | | | 4.5 | | ns |
| $t_w(L)$ | High or Low | 4.5 | | | 4.5 | | |
| $t_w(L)$ | $\overline{MR}$ Pulse Width | 3.0 | | | 3.0 | | ns |
| $t_{rec}$ | Recovery Time $\overline{MR}$ to CP | 4.0 | | | 4.0 | | ns |

## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

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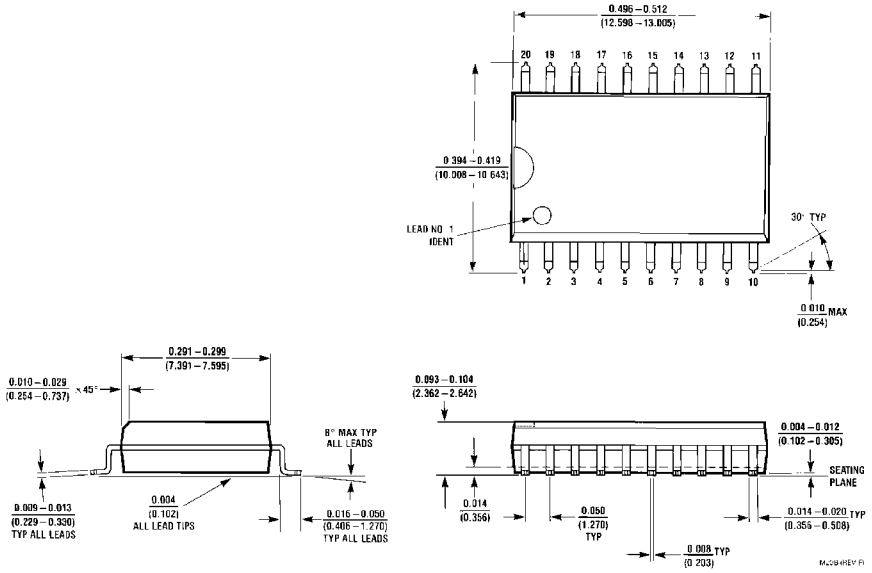
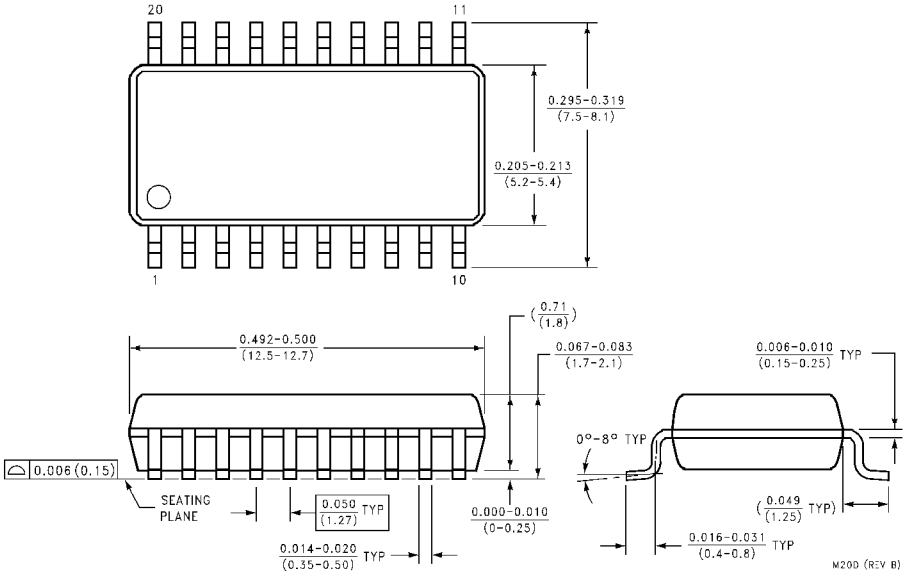
## Physical Dimensions inches (millimeters) unless otherwise noted

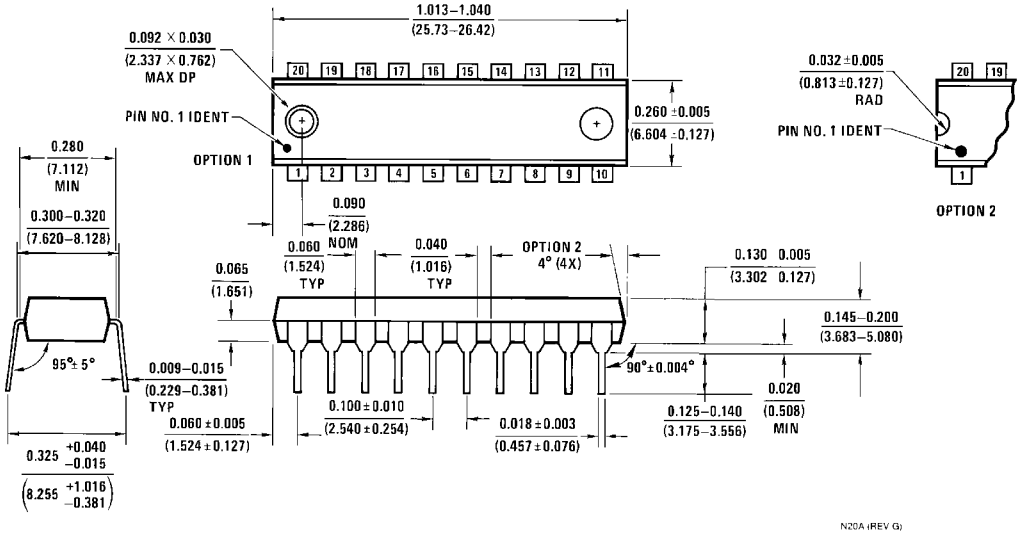



**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)**
**Package Number M20D**




**20-Lead (0.300" Wide) Molded Dual In-Line Package (P)**
**Package Number N20A**

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