



# High Speed CMOS Synchronous Presettable 4-Bit Binary Counters

QS54/74FCT161T  
QS54/74FCT163T

QS54/74FCT2161T  
QS54/74FCT2163T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F161/3 74FCT161/3 and 74FCT161T/3T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

### FCT-T 161T, 163T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. thru C speed grades with 5.6 ns t<sub>PD</sub> for C
- I<sub>OL</sub> = 48 mA Com., 32 mA Mil.

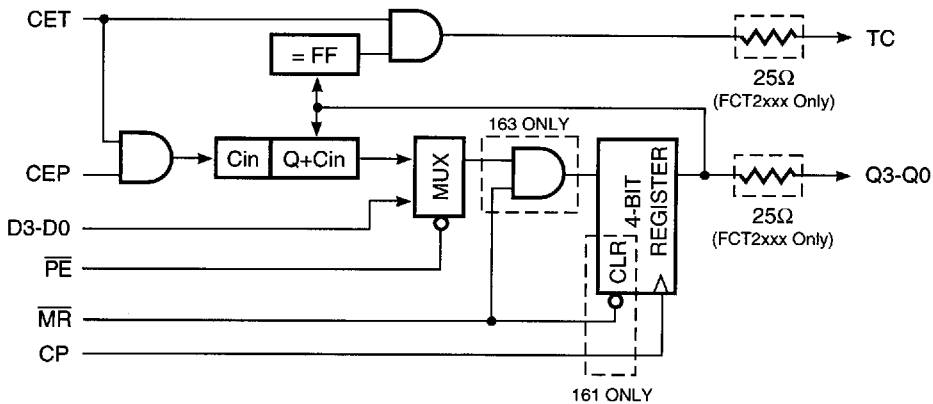
### FCT-T 2161T, 2163T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. and A speed grades with 6.2 ns t<sub>PD</sub> for A
- I<sub>OL</sub> = 12 mA Com.

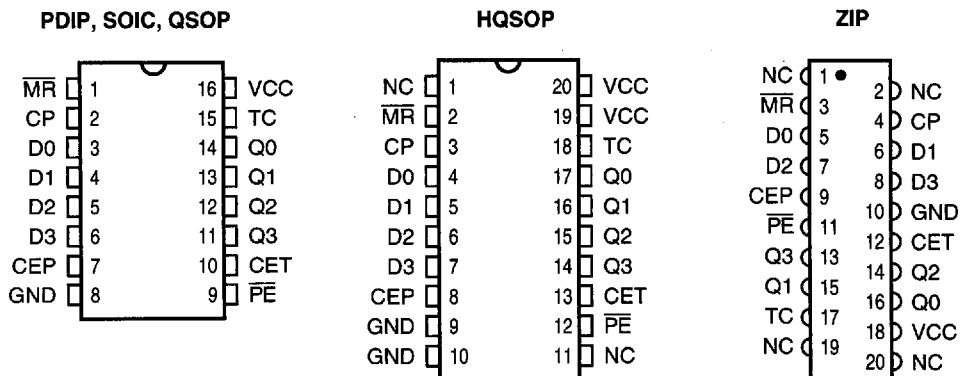
## DESCRIPTION

The QSFC161T and QSFC163T are high-speed CMOS synchronous presettable 4-bit binary counters. The 161 has an asynchronous clear; the 163 has a clocked synchronous clear. The 2161 and 2163 are 25Ω resistor output versions of the 161 and 163, respectively, and are useful for driving transmission lines and reducing system noise. Data is preloaded or the counters count on the rising edge of the clock. Count enable inputs and terminal count outputs allow these counters to be cascaded without loss of speed. Preset inputs override count inputs, and clear inputs override both preset and count inputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

## FUNCTIONAL BLOCK DIAGRAM



**PIN CONFIGURATIONS (All Pins Top View)**



**Note:**  
Available in both 150 mil wide SOIC (package code S1)  
and 300 mil SOIC (package code SO).

**PIN DESCRIPTION**

Name	I/O	Description
D3-D0	I	Data Inputs
Q3-Q0	O	Data Outputs
CP	I	Clock
MR	I	Master Reset

Name	I/O	Description
CEP	I	Count Enable
CET	I	Count and TC Enable
TC	O	Terminal Count
PE	I	Parallel Load Enable

**FUNCTION TABLE**

Inputs						Outputs			Function
MR	PE	CP	CEP	CET	Di	Q3-Q0		TC	
						161	163		
L	X	X	X	X	X	L	—	L	Clear 161
L	X	↑	X	X	X	—	L	L	Clear 163
H	L	↑	X	X	D3-D0	D3-D0	D3-D0	X	Load Data
H	H	↑	H	H	X	Q+1	Q+1	X	Count
H	H	↑	L	X	X	Q	Q	X	Count Inhibit P
H	H	↑	X	L	X	Q	Q	X	Count Inhibit T
H	H	X	X	H	X	F	F	H	Count = 1111
H	H	X	X	H	X	0-E	0-E	L	Count ≠ 1111
H	H	X	X	L	X	X	X	L	TC Inhibit

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20 mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-7, 9, 10	4	4	5	7	pF
11 - 15	6	6	7	9	pF
—	8	8	9	10	pF

**Note:** Capacitance is characterized but not tested.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , $\text{freq} = 0$ <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

## QSFCT161T, 2161T, 163T, 2163T

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCTXXX)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2XXX)	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}, T_A = 25^\circ\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -12 \text{ mA (MIL)}$ $I_{OH} = -15 \text{ mA (COM)}$	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCTXXX)	$V_{CC} = \text{Min.}, I_{OL} = 32 \text{ mA (MIL)}$ $I_{OL} = 48 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$V_{OL}$	Output LOW Voltage (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2XXX- 25 $\Omega$ )	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (MIL)}$ $I_{OL} = 12 \text{ mA (COM)}$	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**QSFACT161T, 2161T, 163T, 2163T**

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		161 163 2161 2163		161A 163A 2161A 2163A		161C 163C		Unit
			Min	Max	Min	Max	Min	Max	
tCPQ	Propagation Delay CP TO Qi, 161/3	Com	2.0	9.5	2.0	6.2	2.0	5.6	ns
		Mil	2.0	10	2.0	6.5	2.0	6.1	
tCPQ	Propagation Delay CP to Qi, 2161/3	Com	2.0	9.5	2.0	6.2	—	—	ns
		Mil	2.0	10	2.0	6.5	—	—	
tMRQ	Propagation Delay $\overline{\text{MR}}$ to Qi, 161	Com	2.0	13	2.0	8.5	2.0	7.8	ns
		Mil	2.0	14	2.0	9.1	2.0	8.3	
tMRQ	Propagation Delay $\overline{\text{MR}}$ to Qi, 2161	Com	2.0	14	2.0	9.1	—	—	ns
		Mil	2.0	13	2.0	8.5	—	—	
tcPTC	Propagation Delay CP to TC	Com	2.0	15	2.0	9.8	2.0	8.8	ns
		Mil	2.0	16.5	2.0	10.8	2.0	9.8	
tcETC	Propagation Delay CET to TC	Com	1.5	8.5	1.5	5.5	1.5	5.0	ns
		Mil	1.5	9	1.5	5.9	1.5	5.4	
tMRTC	Propagation Delay $\overline{\text{MR}}$ to TC	Com	1.5	11.5	1.5	7.5	1.5	6.8	ns
		Mil	1.5	12.5	1.5	8.2	1.5	7.4	

**Notes:**

1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

## QSFCT161T, 2161T, 163T, 2163T

### TIMING REQUIREMENTS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description		161 163 2161 2163		161A 163A 2161A 2163A		161C 163C		Unit
			Min	Max	Min	Max	Min	Max	
ts	Data Setup Time Di to CP	Com	5.0		4.0		3.5		ns
		Mil	5.5		4.5		4.0		
th	Data Hold Time Di to CP	Com	1.5		1.5		1.5		ns
		Mil	2.0		2.0		2.0		
tcs	Count Enab. Setup Time CEP, CET to CP	Com	11.5		9.5		8.5		ns
		Mil	13		11		10		
tCH	Count Enable Hold Time CEP, CET to CP	Com	0		0		0		ns
		Mil	0		0		0		
tmRS tpES	Control Setup Time $\overline{MR}$ , $\overline{PE}$ to CP	Com	11.5		9.5		8.5		ns
		Mil	13.5		11.5		10.5		
tmRH tpEH	Control Hold Time $\overline{MR}$ , $\overline{PE}$ to CP	Com	1.5		1.5		1.5		ns
		Mil	1.5		1.5		1.5		
tcpW	Clock Pulse Width <sup>(1)</sup> HIGH or LOW	Com	5.0		4.0		3.0		ns
		Mil	5.0		4.0		3.0		
tmRW	$\overline{MR}$ Reset Pulse Width <sup>(1)</sup> 161, 2161	Com	5.0		4.0		3.0		ns
		Mil	5.0		4.0		3.0		
tmRW	Reset Recovery Time <sup>(1)</sup> $\overline{MR}$ to CP, 161, 2161	Com	6.0		5.0		4.0		ns
		Mil	6.0		5.0		4.0		

**Notes:**

1. This parameter is guaranteed by design but not tested.
2. See Test Circuit and Waveforms.

3