

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

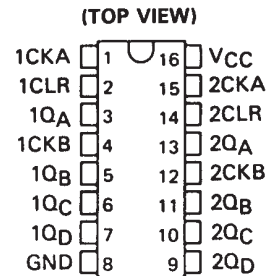
- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

description

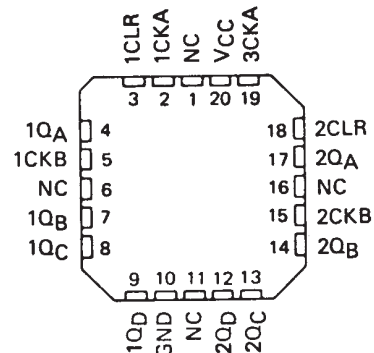
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

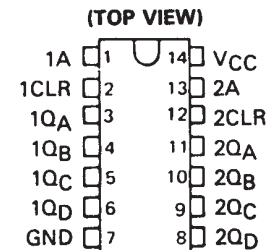
SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390 . . . N PACKAGE
SN74LS390 . . . D OR N PACKAGE



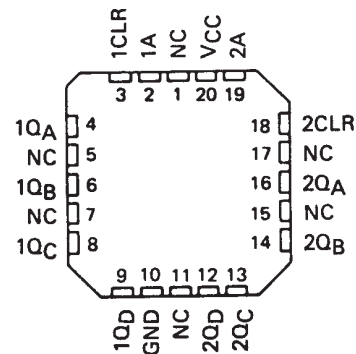
SN54LS390 . . . FK PACKAGE
(TOP VIEW)



SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393 . . . N PACKAGE
SN74LS393 . . . D OR N PACKAGE



SN54LS393 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

**'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

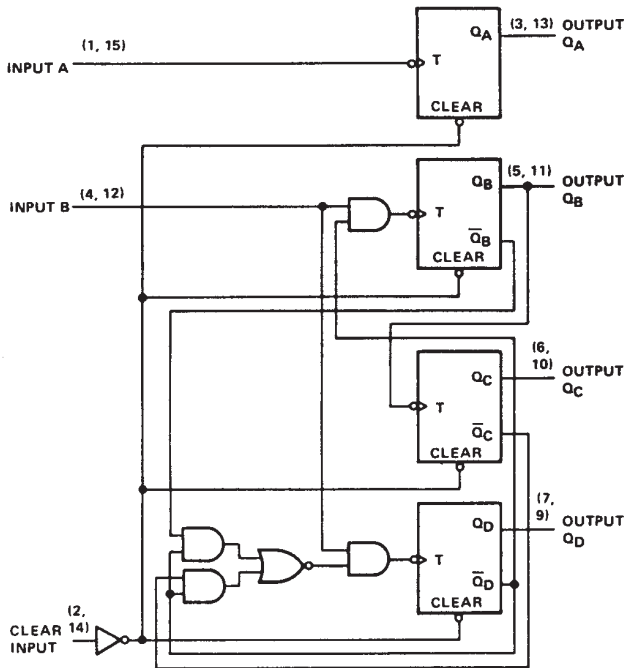
**'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

- NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

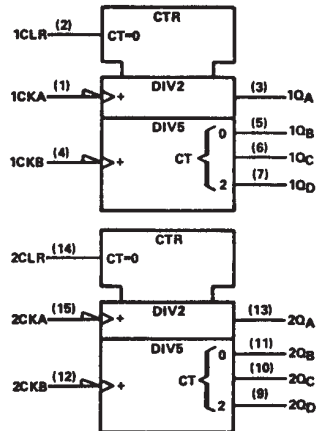
logic diagrams (positive logic)

'390, 'LS390

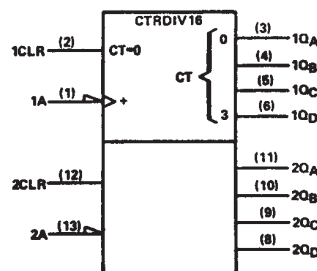


logic symbols †

'390, 'LS390



'393, 'LS393



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

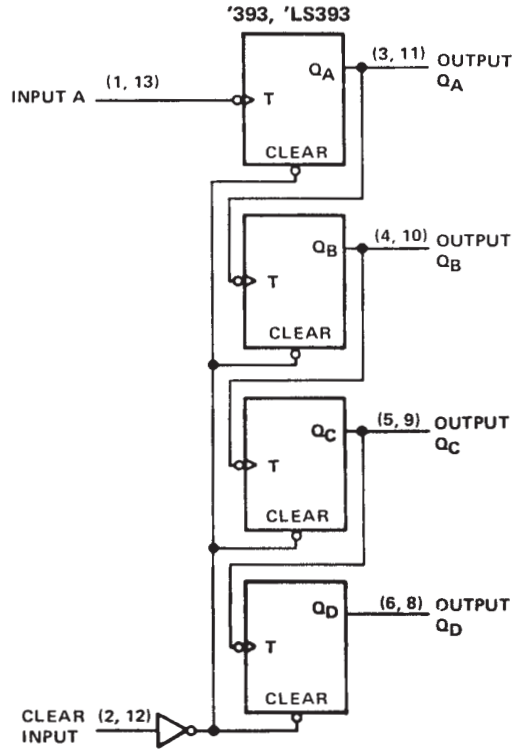
Pin numbers shown are for D, J, N, and W packages.



SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

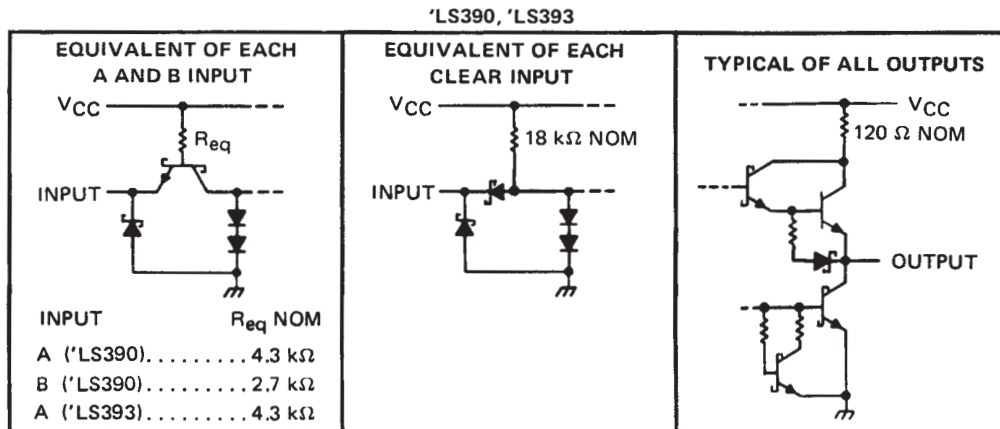
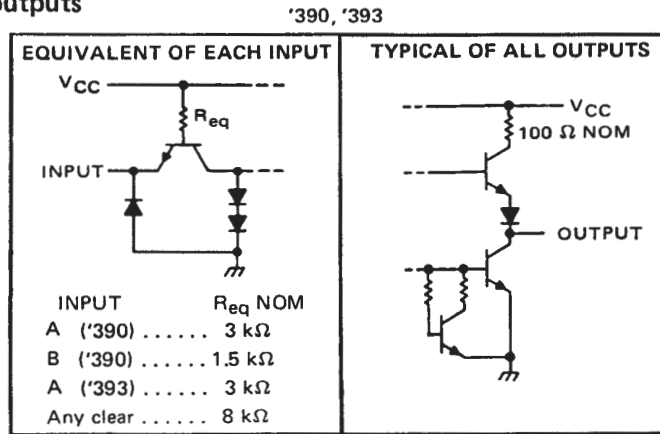
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logic diagrams (continued)



Pin numbers shown are for D, J, N and W packages.

schematics of inputs and outputs



SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	-55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54390 SN54393			SN74390 SN74393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}			-800			-800	μ A	
Low-level output current, I_{OL}			16			16	mA	
Count frequency, f_{count}	A input		0	25	0		25	MHz
	B input		0	20	0		20	
Pulse width, t_w	A input high or low		20		20		ns	
	B input high or low		25		25			
	Clear high		20		20			
Clear inactive-state setup time, t_{SU}	25↓		25↓				ns	
Operating free-air temperature, T_A	-55		125		0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'390			'393			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.8			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA} \uparrow$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH} High-level input current	Clear	40			40			μ A
	Input A	80			80			
	Input B	120						
I_{IL} Low-level input current	Clear	-1			-1			mA
	Input A	-3.2			-3.2			
	Input B	-4.8						
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54'	-20	-57	-20	-57	mA	
		SN74'	-18	-57	-18	-57		
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	42	69		38	64	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ The Q_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

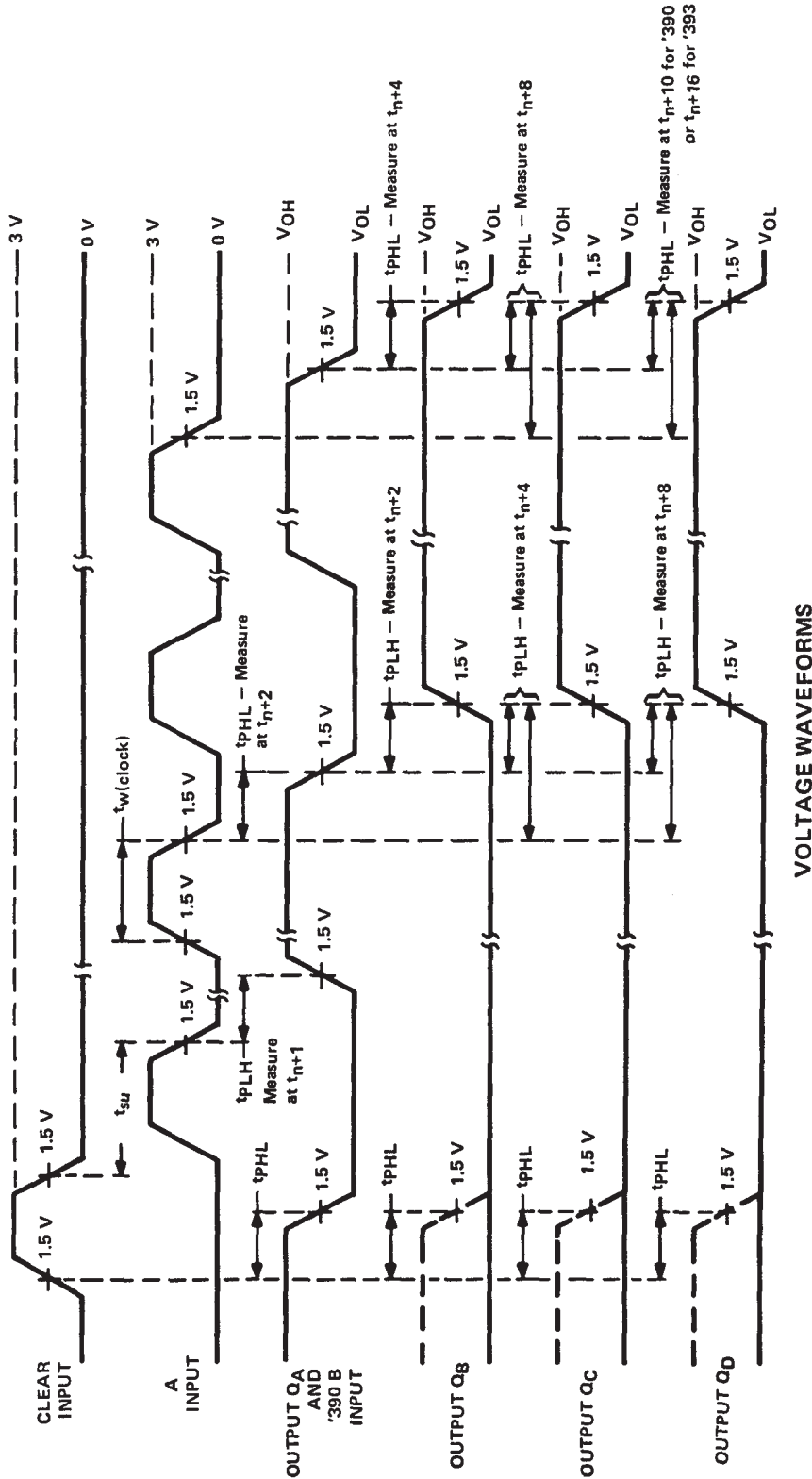
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 3 and Figure 1	25	35		25	35	MHz	
	B	Q_B		20	30					
t_{PLH}	A	Q_A		12	20		12	20	ns	
t_{PHL}				13	20		13	20		
t_{PLH}	A	Q_C of '390 Q_D of '393		37	60		40	60	ns	
t_{PHL}				39	60		40	60		
t_{PLH}	B	Q_B		13	21				ns	
t_{PHL}				14	21					
t_{PLH}	B	Q_C		24	39				ns	
t_{PHL}				26	39					
t_{PLH}	B	Q_D		13	21				ns	
t_{PHL}				14	21					
t_{PHL}	Clear	Any		24	39		24	39	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 1



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SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	-55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}			-400			-400	μ A	
Low-level output current, I_{OL}			4			8	mA	
Count frequency, f_{count}	A input		0	25	0		25	MHz
	B input		0	12.5	0		12.5	
Pulse width, t_w	A input high or low		20		20		ns	
	B input high or low		40		40			
	Clear high		20		20			
Clear inactive-state setup time, t_{SU}	25 \downarrow		25 \downarrow				ns	
Operating free-air temperature, T_A	-55		125		0		70	°C

\downarrow The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS'			SN74LS'			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.7			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$	$I_{OL} = 4 \text{ mA}$ [¶]		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$ [¶]				0.35	0.5	
I_I Input current at maximum input voltage	Clear	$V_{CC} = \text{MAX}$		$V_I = 7 \text{ V}$		0.1	0.1	mA
	Input A			$V_I = 5.5 \text{ V}$		0.2	0.2	
	Input B					0.4	0.4	
I_{IH} High-level input current	Clear	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$				0.02	0.02	mA
	Input A					0.1	0.1	
	Input B					0.2	0.2	
I_{IL} Low-level input current	Clear	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				-0.4	-0.4	mA
	Input A					-1.6	-1.6	
	Input B					-2.4	-2.4	
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	-20	-100			mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS390		15	26	15	26	mA
		'LS393		15	26	15	26	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[¶] The Q_A outputs of the 'LS390 are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS**

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

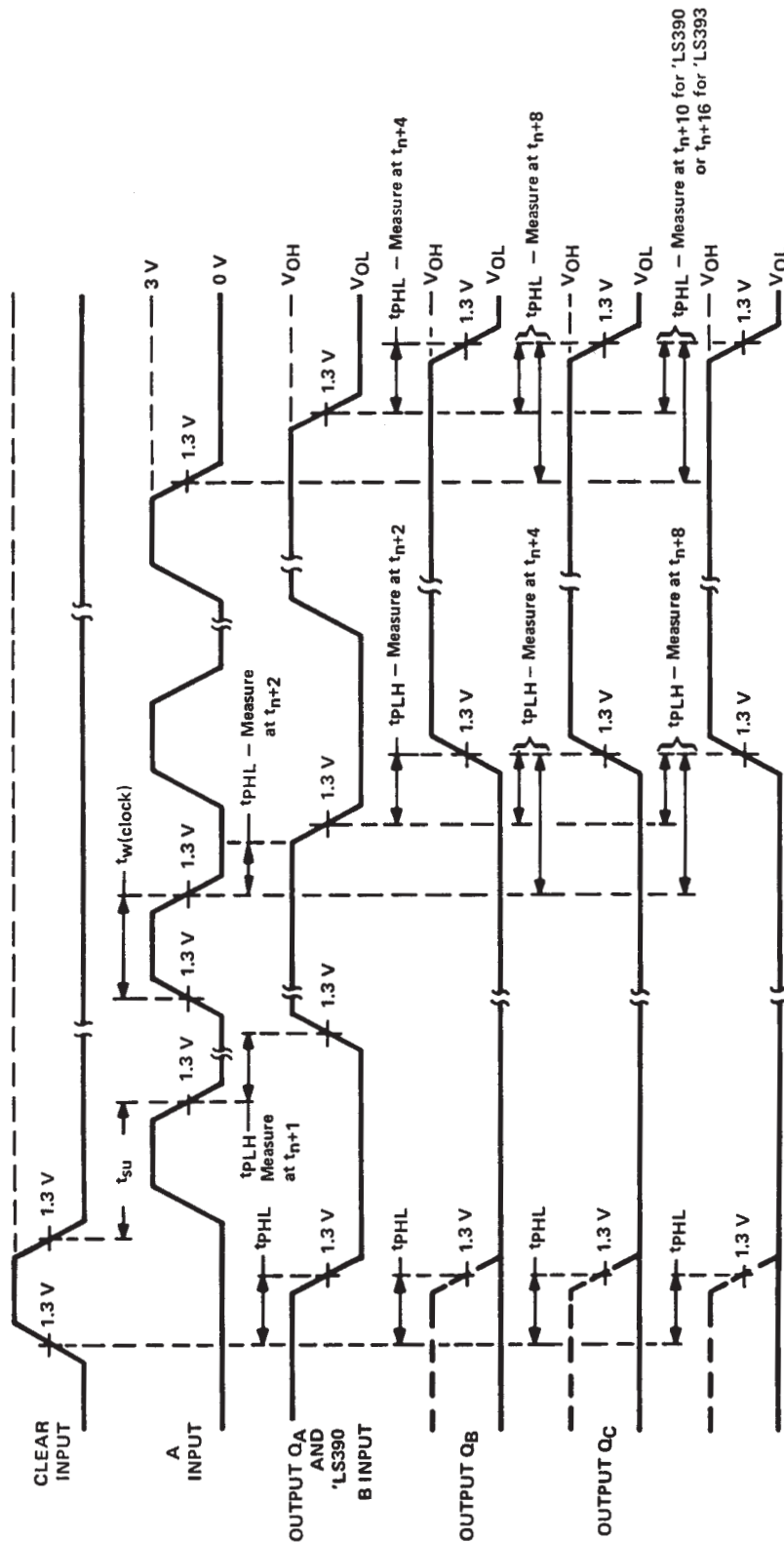
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Note 4 and Figure 2	25	35		25	35	MHz	
	B	Q_B		12.5	20					
t_{PLH}	A	Q_A		12	20		12	20	ns	
t_{PHL}				13	20		13	20		
t_{PLH}	A	Q_C of 'LS390		37	60		40	60	ns	
t_{PHL}		Q_D of 'LS393		39	60		40	60		
t_{PLH}	B	Q_B		13	21				ns	
t_{PHL}				14	21					
t_{PLH}	B	Q_C		24	39				ns	
t_{PHL}				26	39					
t_{PLH}	B	Q_D		13	21				ns	
t_{PHL}				14	21					
t_{PHL}	Clear	Any		24	39		24	39	ns	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50 %, $Z_{out} \approx 50$ ohms.

FIGURE 2

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SN74LS390, Dual 4-Bit Decade Counters

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS390	SN74LS390
Voltage Nodes (V)	5	5

FEATURES

[▲Back to Top](#)

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 ... Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393 ... Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency ... 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

DESCRIPTION

[▲Back to Top](#)

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a binary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals. Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

[▲Back to Top](#)

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Full datasheet in Acrobat PDF: [sn74ls390.pdf](#) (343 KB) (Updated: 03/01/1988)

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- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

[▲ Back to Top](#)

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS390D	ACTIVE	SOP (D) 16	0 TO 70	View Contents	1KU 0.46	40	1000	> 10k 10 Oct	4 WKS	Avnet AMERICA	650	BUY NOW
SN74LS390DR	ACTIVE	SOP (D) 16	0 TO 70	View Contents	1KU 0.49	2500	N/A*	> 10k 10 Oct	4 WKS			
SN74LS390N	ACTIVE	PDIP (N) 16	0 TO 70	View Contents	1KU 0.41	25	N/A*	119 24 Sep	4 WKS	Avnet AMERICA	> 1k	BUY NOW
								> 10k 04 Oct				
								> 10k 09 Oct				
SN74LS390N3	OBSOLETE	PDIP (N) 16	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS390NSR	ACTIVE	SOP (NS) 16		View Contents	1KU 0.41	2000	N/A*	2000 03 Oct	4 WKS			
								> 10k 04 Oct				
								2302 11 Oct				
								> 10k 18 Oct				

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PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS393, Dual 4-Bit Binary Counters

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS393	SN74LS393
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
Clear	Async	Async

FEATURES

[▲Back to Top](#)

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 ... Individual Clocks for A and B Flip-Flops Provide Dual ÷ 2 and ÷ 5 Counters
- '393, 'LS393 ... Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency ... 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

DESCRIPTION

[▲Back to Top](#)

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a binary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals. Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

[▲Back to Top](#)

To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

[▲Back to Top](#)

Full datasheet in Acrobat PDF: [sn74ls393.pdf](#) (343 KB) (Updated: 03/01/1988)

View Application Notes for [Digital Logic](#)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTS[▲Back to Top](#)View Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG[▲Back to Top](#)

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS393D	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.46	50	N/A*		12 WKS			
SN74LS393DR	ACTIVE	SOP (D) 14	0 TO 70	View Contents	1KU 0.49	2500	N/A*		12 WKS			
SN74LS393J	OBSOLETE	CDIP (J) 14	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS393N	ACTIVE	PDIP (N) 14	0 TO 70	View Contents	1KU 0.41	25	N/A*		16 WKS	Avnet AMERICA	>1k	BUY NOW
										DigiKey AMERICA	317	BUY NOW
SN74LS393N3	OBSOLETE	PDIP (N) 14	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS393NSR	ACTIVE	SOP (NS) 14		View Contents	1KU 0.41	2000	N/A*		12 WKS			

Table Data Updated on: 9/26/2002