

## 24-BIT QUADRATURE COUNTER

Feb 2018

### FEATURES.

- Programmable count modes: non-quadrature, up/down, quadrature X1, X2 or X4, binary, BCD, 24-hour clock, mod-N and single cycle.
- Up to 40MHz count frequency in non-quadrature mode.
- 24-bit counter, 24-bit preset register and 24-bit comparator.
- 8-bit bi-directional data bus for uC interface.
- Readable status register.
- Carry, borrow, carry toggle and borrow toggle outputs.
- Compare and compare toggle outputs for counter to preset register equality.
- Programmable inputs for dynamic hardware control.
- TTL and CMOS compatible IOs.
- Operating voltage: 3V to 5.5V.
- Package types: DIP (LS7166A), SOIC (LS7166A-S), TSSOP (LS7166A-TS24).

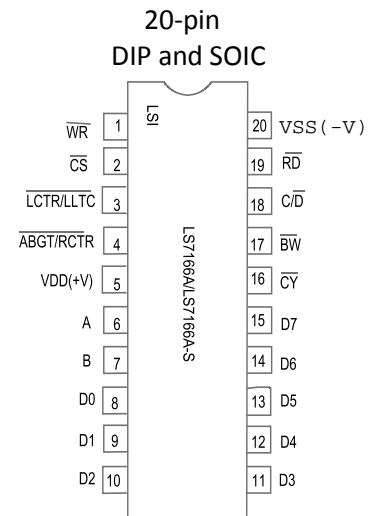
### GENERAL DESCRIPTION.

LS7166A is a CMOS, 24-bit counter which can be programmed to operate in several functional modes. The operating modes are set up by writing configuration data into control registers (see fig 8). There are three 6-bit and one 2-bit control registers for configuring the functional modes. In addition to the control registers there is a 5-bit status register which indicates the instantaneous device status. A 24-bit preset register is available for presetting the counter. It also serves as the division factor in the mod-N count mode. The device communicates with a host controller over an 8-bit 3-state bidirectional data bus through read/write operations. In addition, a number of discrete inputs and outputs facilitate instantaneous hardware control functions and instantaneous status indication.

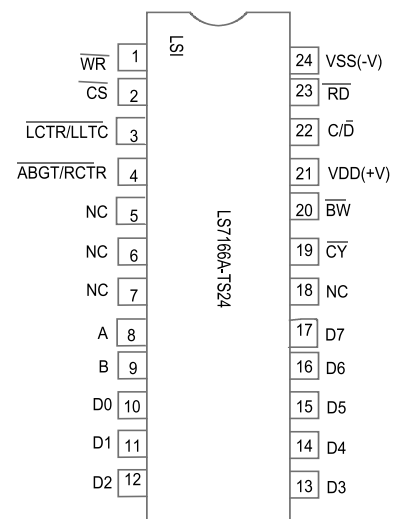
### REGISTER DESCRIPTION.

Hardware registers are accessible via the data bus (D7-D0) for read or write when CS = 0. The C/D input selects between a control register (C/D = 1) and a data register (C/D = 0) during a read or write operation (see table 1).

### PIN ASSIGNMENTS- Top View

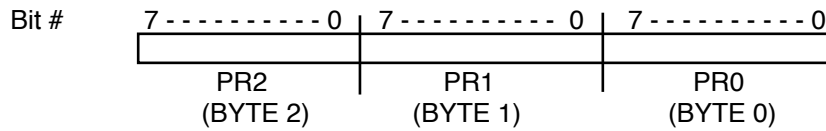


### 24-pin TSSOP



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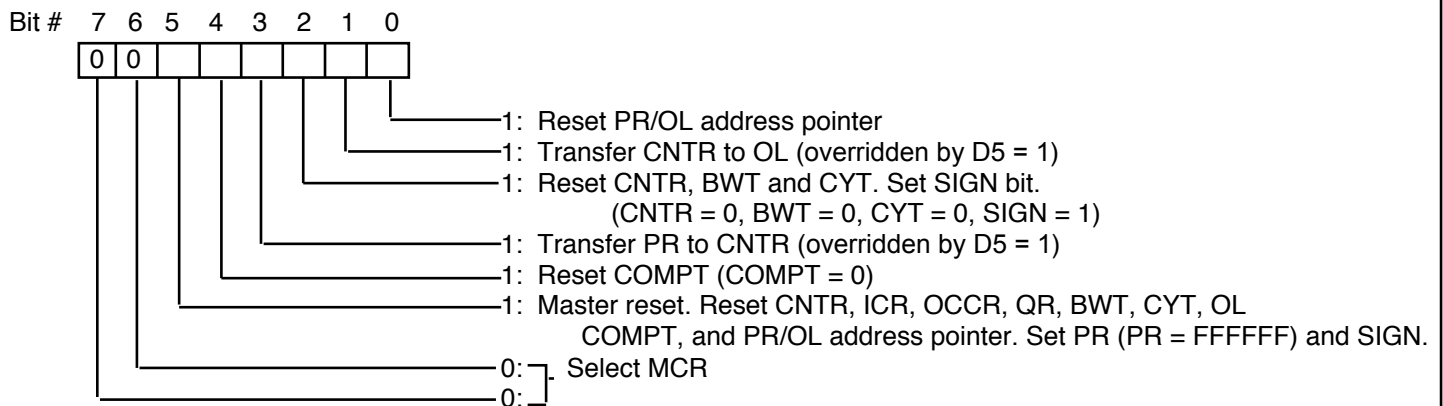
**PR (Preset register).** The PR is the input port for the CNTR. The CNTR is loaded with a 24 bit data via the PR. The data is first written into the PR in 3 WRITE cycle sequence of Byte 0 (PR0), Byte 1 (PR1) and Byte 2 (PR2). The address pointer for PR0/PR1/PR2 is automatically incremented with each write cycle. Accessed by: WRITE when  $C/\overline{D} = 0$ ,  $\overline{CS} = 0$ .



Standard Sequence for Loading PR and Reading CNTR:

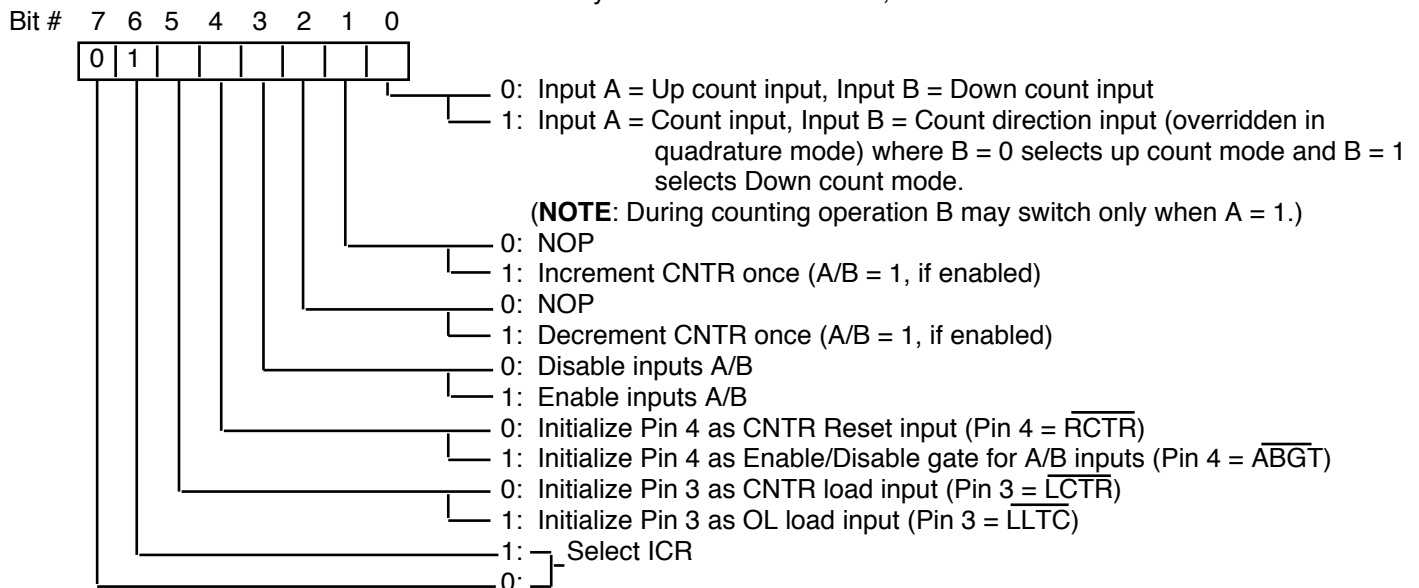
- 1 → MCR ; Reset PR address pointer
- WRITE PR ; Load Byte 0 and into PR0 increment address
- WRITE PR ; Load Byte 1 and into PR1 increment address
- WRITE PR ; Load Byte 2 and into PR3 increment address
- 8 → MCR ; Transfer PR to CNTR

**MCR (Master Control Register).** Performs register reset and load operations. Writing a "non-zero" word to MCR does not require a follow-up write of an "all-zero" word to terminate a designated operation. Accessed by: WRITE when  $C/\overline{D} = 1$ ,  $\overline{CS} = 0$ .



**NOTE:** Control functions may be combined.

**ICR (Input Control Register).** Initializes counter input operating modes. Accessed by: WRITE when  $C/\overline{D} = 1$ ,  $\overline{CS} = 0$ .



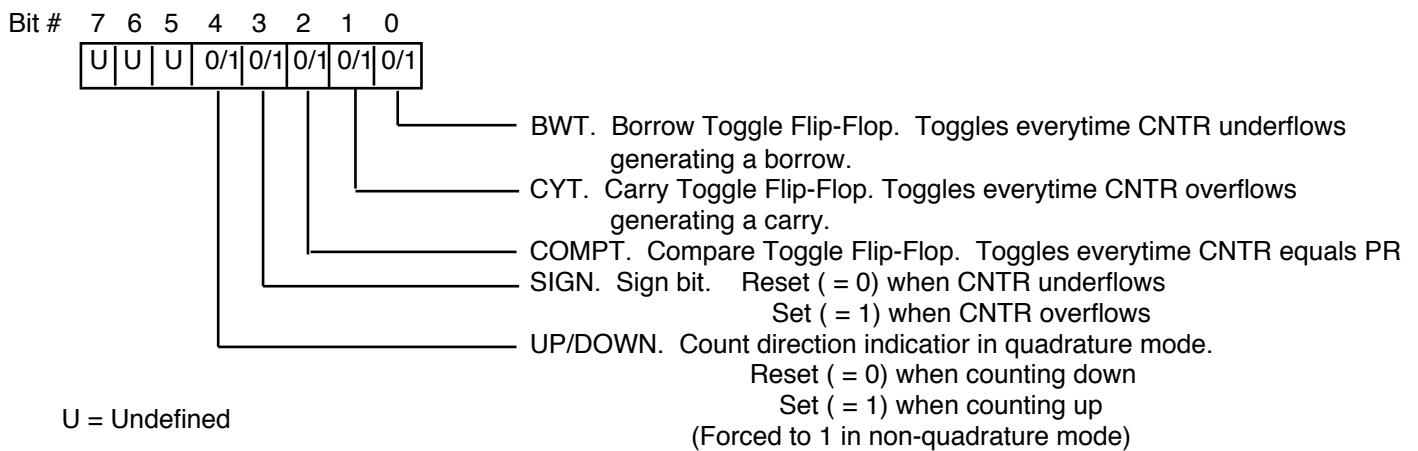
**NOTE:** Control functions may be combined.

**TABLE 1 - Register Addressing Modes**

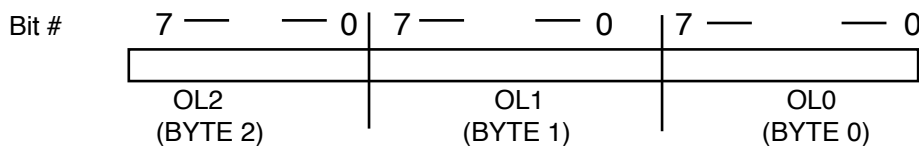
| D7 | D6 | C/D | R $\bar{D}$ | WR        | C $\bar{S}$ | COMMENT   |
|----|----|-----|-------------|-----------|-------------|---|
| X  | X  | X   | X           | X         | 1           | Disable Chip for READ/WRITE   |
| 0  | 0  | 1   | 1           | $\bar{1}$ | 0           | Write to Master Control Register (MCR)                                |
| 0  | 1  | 1   | 1           | $\bar{1}$ | 0           | Write to input control register (ICR)                                 |
| 1  | 0  | 1   | 1           | $\bar{1}$ | 0           | Write to output/counter control register (OCCR)                       |
| 1  | 1  | 1   | 1           | $\bar{1}$ | 0           | Write to quadrature register (QR)                                     |
| X  | X  | 0   | 1           | $\bar{1}$ | 0           | Write to preset register (PR) and increment register address counter. |
| X  | X  | 0   | $\bar{1}$   | 1         | 0           | Read output latch (OL) and increment register address counter         |
| X  | X  | 1   | $\bar{1}$   | 1         | 0           | Read output status register (OSR).                                    |

X = Don't Care

**OSR (Output Status Register).** Indicates CNTR status: Accessed by: READ when C/D = 1, C $\bar{S}$  = 0.



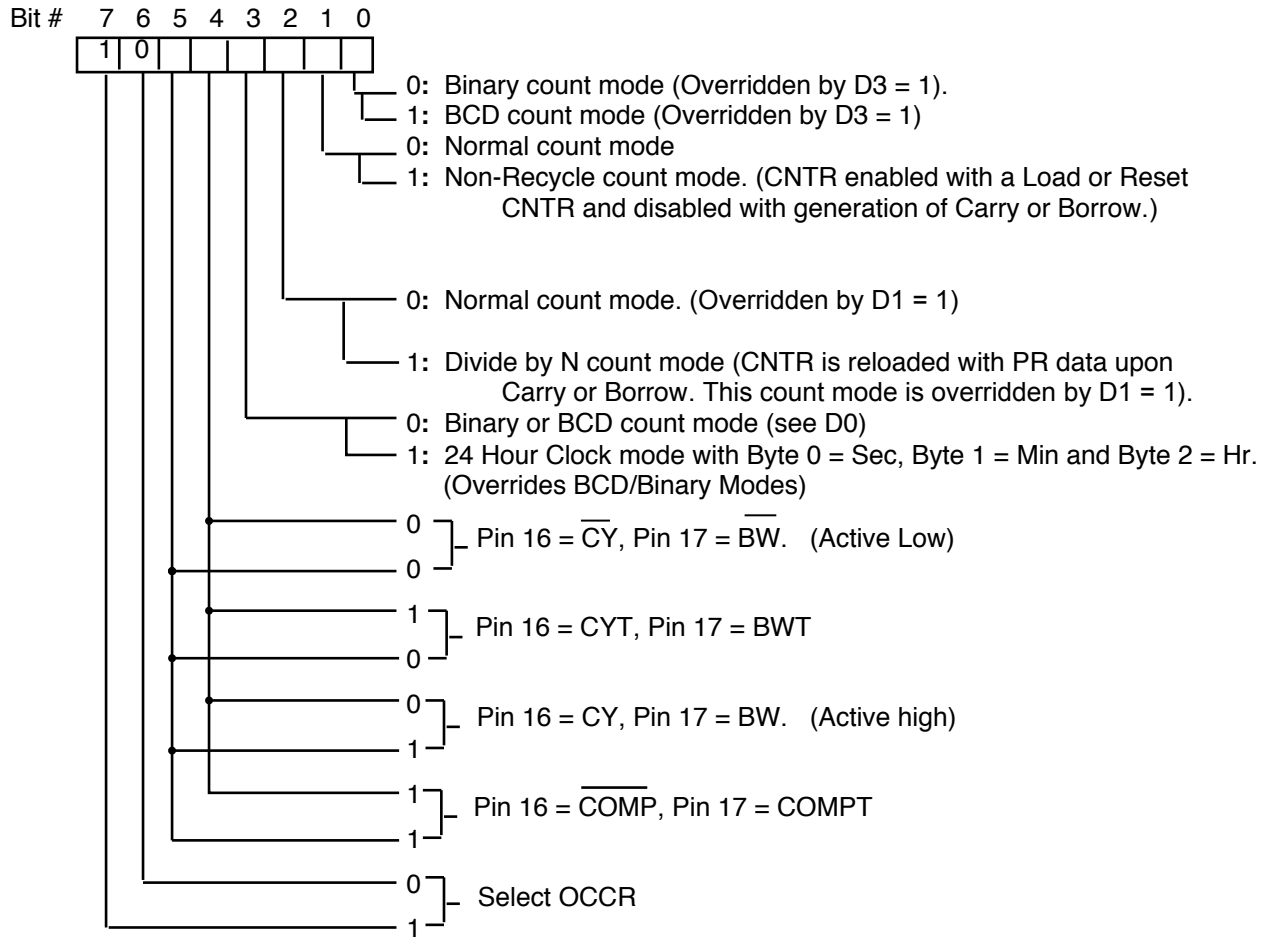
**OL(Output latch).** The OL is the output port for the CNTR. The 24 bit CNTR Value at any instant can be accessed by performing a CNTR to OL transfer and then reading the OL in 3 READ cycle sequence of Byte 0 (OL0), Byte 1 (OL1) and Byte 2 (OL2). The address pointer for OL0/OL1/OL2 is automatically incremented with each READ cycle. Accessed by: READ when C/D = 0, C $\bar{S}$  = 0.



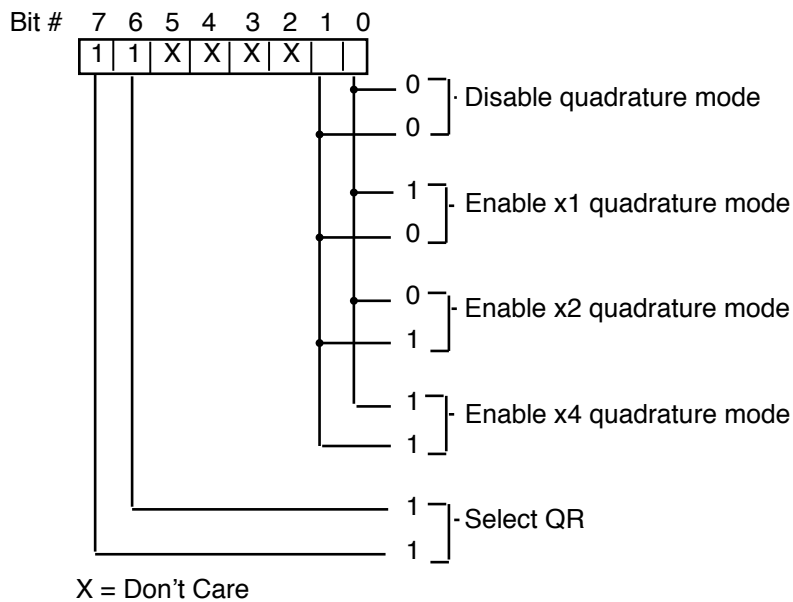
Standard Sequence for Loading and Reading OL:

- 3 → MCR ; Reset OL address pointer and Transfer CNTR to OL
- READ OL ; Read Byte 0 and increment address
- READ OL ; Read Byte 1 and increment address
- READ OL ; Read Byte 2 and increment address

**OCCR (Output Control Register)** Initializes CNTR and output operating modes.  
 Accessed by : WRITE when  $\overline{C/D} = 1$ ,  $\overline{CS} = 0$ .



**QR (Quadrature Register).** Selects quadrature count mode (See Fig. 7)  
 Accessed by: WRITE when  $\overline{C/D} = 1$ ,  $\overline{CS} = 0$ .



**I/O DESCRIPTION:****(See REGISTER DESCRIPTION for I/O Prgramming.)**

**Data-Bus (D0 - D7)** (Pin 8 - Pin 15). The 8-line data bus is a three-state I/O bus for interfacing with the system bus.

**$\overline{CS}$  (Chip Select Input)** (Pin 2). A logical "0" at this input enables the chip for Read and Write.

**$\overline{RD}$  (Read Input)** (Pin 19). A logical "0" at this input enables the OSR and the OL to be read on the data bus.

**$\overline{WR}$  (Write Input)** (Pin 1). A logical "0" at this input enables the data bus to be written into the control and data registers.

**$C/\overline{D}$  (Control/Data Input)** (Pin 18). A logical "1" at this input enables a control word to be written into one of the four control registers or the OSR to be read on the I/O bus. A logical "0" enables a data word to be written into the PR, or the OL to be read on the I/O bus.

**A** (Pin 6). Input A is a programmable count input capable of functioning in three different modes, such as up count input, down count input and quadrature input. In non-quadrature mode, the counter advances on the rising edge of Input A

**B** (Pin 7). Input B is also a programmable count input that can be programmed to function either as down count input, or count direction control gate for input A, or quadrature input. In non-quadrature mode, and when programmed as the Down Count input, the counter advances on the rising edge of Input B. When B is programmed as the count direction control gate, B = 0 enables A as the Up Count input and B = 1 enables A as the Down Count input. When programmed as the direction input, B can switch state only when A is high.

**$\overline{ABGT}/\overline{RCTR}$**  (Pin 4). This input can be programmed to function as either inputs A and B enable gate or as external counter reset input. A logical "0" is the active level on this input. In non-quadrature mode, if Pin 4 is programmed as A and B enable gate input, it may switch state only when A is high (if A is clock and B is direction) or when both A and B are high (if A and B are clocks). In quadrature mode, if Pin 4 is programmed as A and B enable gate, it may switch state only when either A or B switches.

**$\overline{LCTR}/\overline{LLTC}$**  (Pin 3) This input can be programmed to function as the external load command input for either the CNTR or the OL. When programmed as counter load input, the counter is loaded with the data contained in the PR. When programmed as the OL load input, the OL is loaded with data contained in the CNTR. A logical "0" is the active level on this input.

**$\overline{CY}$**  (Pin 16) This output can be programmed to serve as one of the following:

- A.  $\overline{CY}$ . Complemented Carry out (active "0").
- B. CY. True Carry out (active "1").
- C. CYT. Carry Toggle flip-flop out.
- D.  $\overline{COMP}$ . Comparator out (active "0")

**$\overline{BW}$**  (Pin 17) This output can be programmed to serve as one of the following:

- A.  $\overline{BW}$ . Complemented Borrow out (active "0").
- B. BW. True Borrow out (active "1").
- C. BWT. Borrow Toggle flip-flop out.
- D. COMPT. Comparator Toggle output.

**VDD** (Pin 5) Supply voltage positive terminal.

**VSS** (Pin 20) Supply voltage negative terminal.

**Absolute Maximum Ratings:**

| Parameter             | Symbol                            | Values   | Unit |
|-----------------------|-----------------------------------|--|------|
| Voltage at any input  | V <sub>IN</sub>                   | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Operating Temperature | T <sub>A</sub>                    | -40 to +125                                    | °C   |
| Storage Temperature   | T <sub>STG</sub>                  | -65 to +150                                    | °C   |
| Supply Voltage        | V <sub>DD</sub> - V <sub>SS</sub> | +7.0   | V    |

**DC Electrical Characteristics.** (All voltages referenced to V<sub>SS</sub>.)

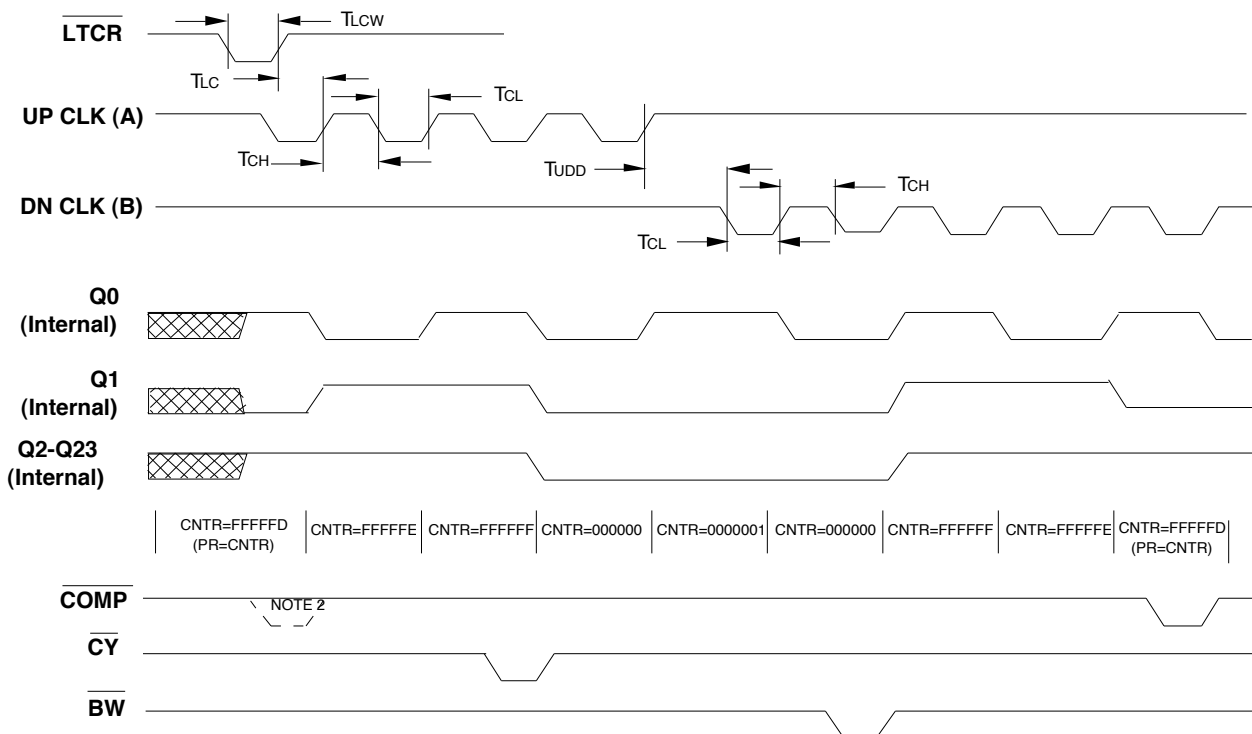
T<sub>A</sub> = 0° to 85°C, V<sub>DD</sub> = 3V to 5.5V, f<sub>c</sub> = 0, unless otherwise specified)

| Parameter                          | Symbol            | Min. Value | Max. Value      | Unit | Remarks                                      |
|------------------------------------|-------------------|------------|-----------------|------|--|
| Supply Voltage                     | V <sub>DD</sub>   | 3.0        | 5.5             | V    | -  |
| Supply Current                     | I <sub>DD</sub>   | -          | 350             | μA   | Outputs open                                 |
| Input Low Voltage                  | V <sub>IL</sub>   | 0          | 0.8             | V    | -  |
| Input High Voltage                 | V <sub>IH</sub>   | 2.0        | V <sub>DD</sub> | V    | -  |
| Output Low Voltage                 | V <sub>OL</sub>   | -          | 0.5             | V    | 4mA Sink, V <sub>DD</sub> = 5V               |
| Output High Voltage                | V <sub>OH</sub>   | 4.4        | -               | V    | 4mA Source, V <sub>DD</sub> = 5V             |
| Input Current                      | -                 | -          | 15              | nA   | Leakage current                              |
| Output Source Current              | I <sub>SRC</sub>  | 4          | -               | mA   | V <sub>OH</sub> = 4.4V, V <sub>DD</sub> = 5V |
| Output Sink Current                | I <sub>SINK</sub> | 4          | -               | mA   | V <sub>OL</sub> = 0.5V, V <sub>DD</sub> = 5V |
| Data Bus Off-State Leakage Current | -                 | -          | 15              | nA   | -  |

**TRANSIENT CHARACTERISTICS** (See Timing Diagrams in Fig. 2 thru Fig. 7,  
VDD = 3V to 5.5V, TA = 0° to 85°C, unless otherwise specified)

| Parameter  | Symbol | Min.Value | Max.Value | Unit          |
|--|--------|-----------|-----------|---------------|
| Clock A/B "Low" (Note 1)   | Tcl    | 15        | No Limit  | ns            |
| Clock A/B "High" (Note 1)  | Tch    | 10        | No Limit  | ns            |
| Clock A/B Frequency<br>(Note 1)  | fc     | 0         | 40        | MHz           |
| UP/DN Reversal Delay<br>(Note 1)   | Tudd   | 30        | -         | ns            |
| LCTR Positive edge to<br>the next A/B positive or<br>negative edge delay | TLC    | 30        | -         | ns            |
| Clock A/B to<br>CY/BW/COMP "low"<br>propagation delay                    | TCBL   | -         | 65        | ns            |
| Clock A/B to<br>CY/BW/COMP "high"<br>propagation delay                   | TCBH   | -         | 85        | ns            |
| LCTR and LLTC pulse<br>width   | TLCW   | 60        | -         | ns            |
| Clock A/B to CYT, BWT<br>and COMPT "high"<br>propagation delay           | TTFH   | -         | 100       | ns            |
| Clock A/B to CYT, BWT<br>and COMPT "low"<br>propagation delay            | TTFL   | -         | 100       | ns            |
| WR pulse width   | TWR    | 60        | -         | ns            |
| RD to data out delay<br>(CL=20pF)  | TRD    | -         | 11        | ns            |
| CS, RD Terminate to<br>Data-Bus Tri-State                                | TRT    | -         | 30        | ns            |
| Data-Bus set-up<br>time for WR   | TDS    | 30        | -         | ns            |
| Data-Bus hold time for WR  | TDH    | 15        | -         | ns            |
| CS set-up time for RD  | TSRS   | 0         | -         | ns            |
| CS hold time for RD  | TSRH   | 0         | -         | ns            |
| Back to Back RD delay  | TRR    | 60        | -         | ns            |
| RD to WR delay   | -      | 60        | -         | ns            |
| C/D set-up time for RD   | TCRS   | 0         | -         | ns            |
| C/D hold time for RD   | TCRH   | 15        | -         | ns            |
| C/D set-up time for WR   | TCWS   | 30        | -         | ns            |
| C/D hold time for WR   | TCWH   | 15        | -         | ns            |
| CS set-up time for WR  | TSWS   | 60        | -         | ns            |
| CS hold time for WR  | TSWH   | 0         | -         | ns            |
| Back to Back WR delay  | Tww    | 60        | -         | ns            |
| WR to RD delay   | -      | 60        | -         | ns            |
| <b>Quadrature Mode:</b>  |        |           |           |               |
| Clock A/B Validation delay   | TCQV   | -         | 180       | ns, VDD = 5V  |
| A and B phase delay  | TPH    | 230       | -         | ns, VDD = 5V  |
| Clock A/B frequency  | fcQ    | -         | 1.1       | MHz, VDD = 5V |
| CY, BW, COMP pulse width   | TCBW   | 120       | 170       | ns, VDD = 5V  |

NOTE 1: In non-quadrature mode only.

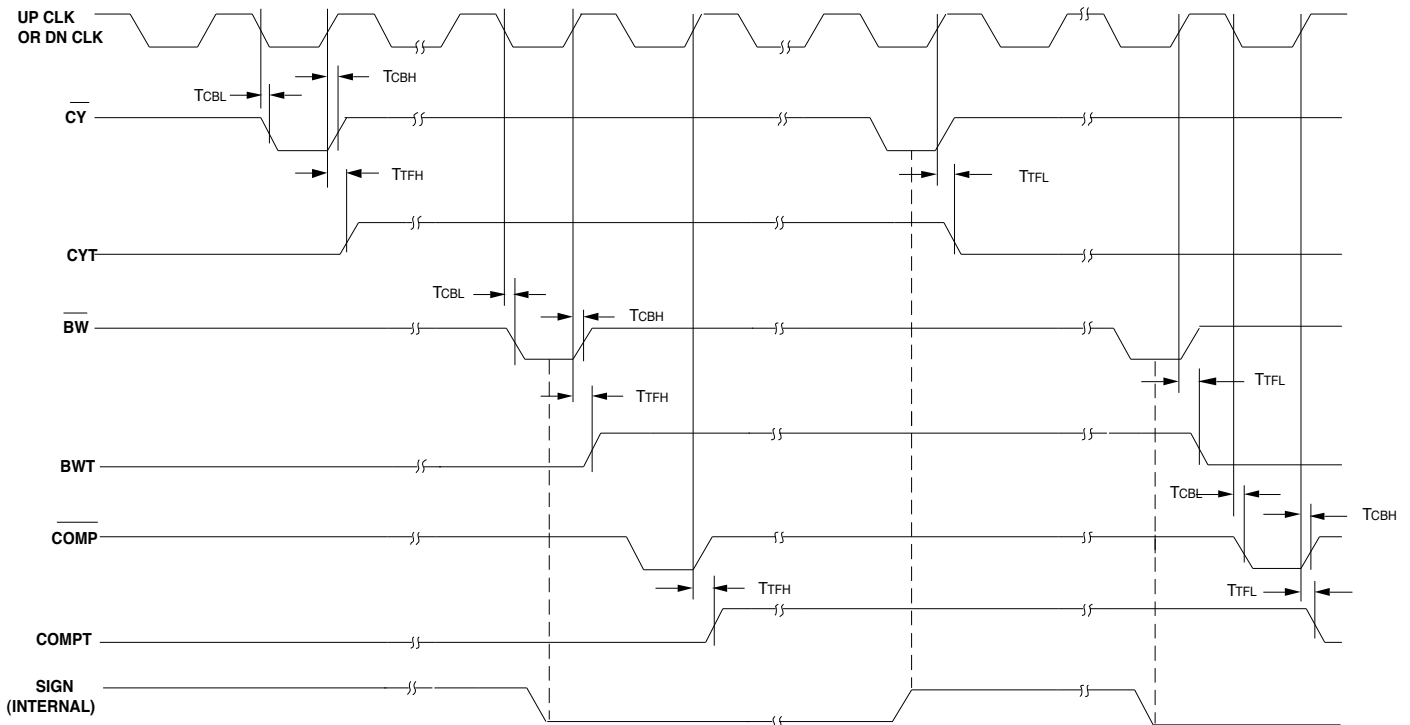


**FIGURE 2 . LOAD COUNTER, UP CLOCK, DOWN CLOCK, COMPARE OUT, CARRY, BORROW**

**NOTE 1:** The counter in this example is assumed to be operating in the binary mode.

**NOTE 2:** No COMP output is generated here, although PR = CNTR. COMP output is disabled with a counter load command and enabled with the rising edge of the next clock, thus eliminating invalid COMP outputs whenever the CNTR is loaded from the PR.

**NOTE 3:** When UP Clock is active, the DN Clock should be held "HIGH" and vice versa.



**FIGURE 3. CLOCK TO  $\overline{CY}/\overline{BW}$  OUTPUT PROPAGATION DELAYS**

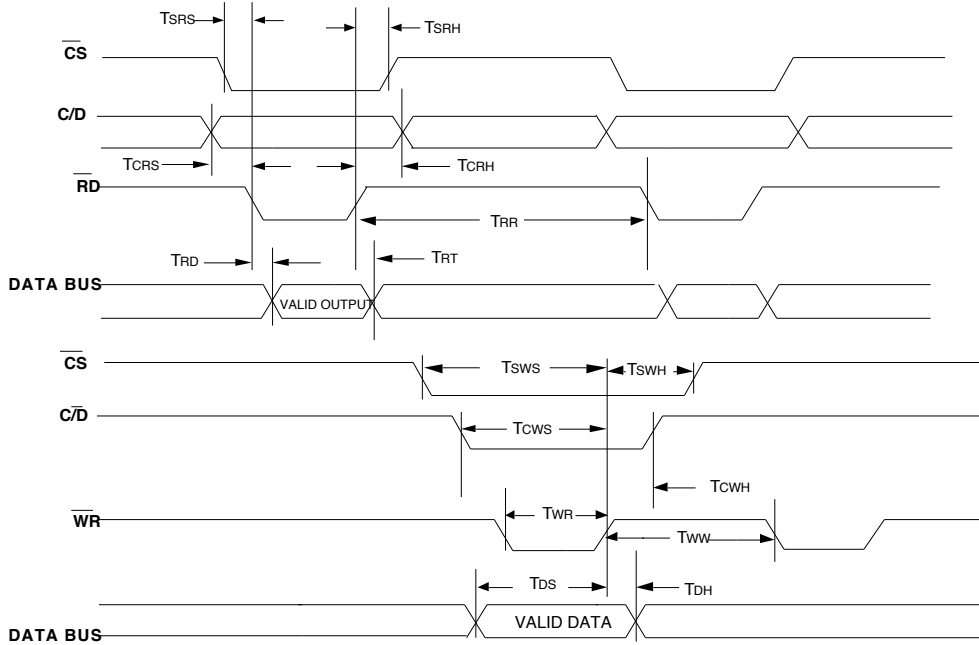
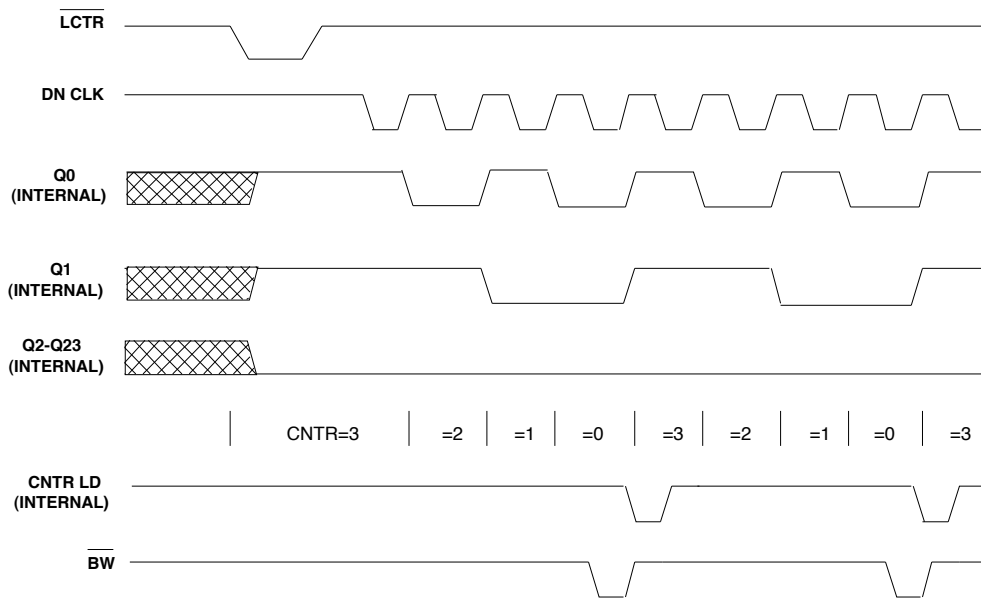


FIGURE 4. READ/WRITE CYCLES



NOTE: EXAMPLE OF DIVIDE BY 4 IN DOWN COUNT MODE

FIGURE 5. DIVIDE BY N MODE

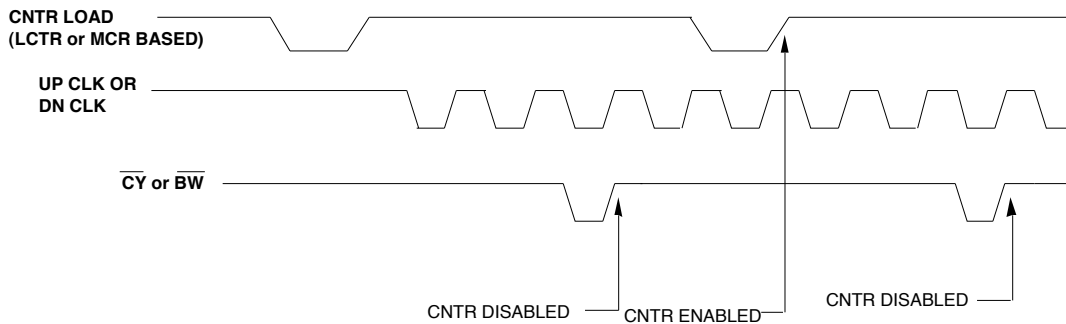
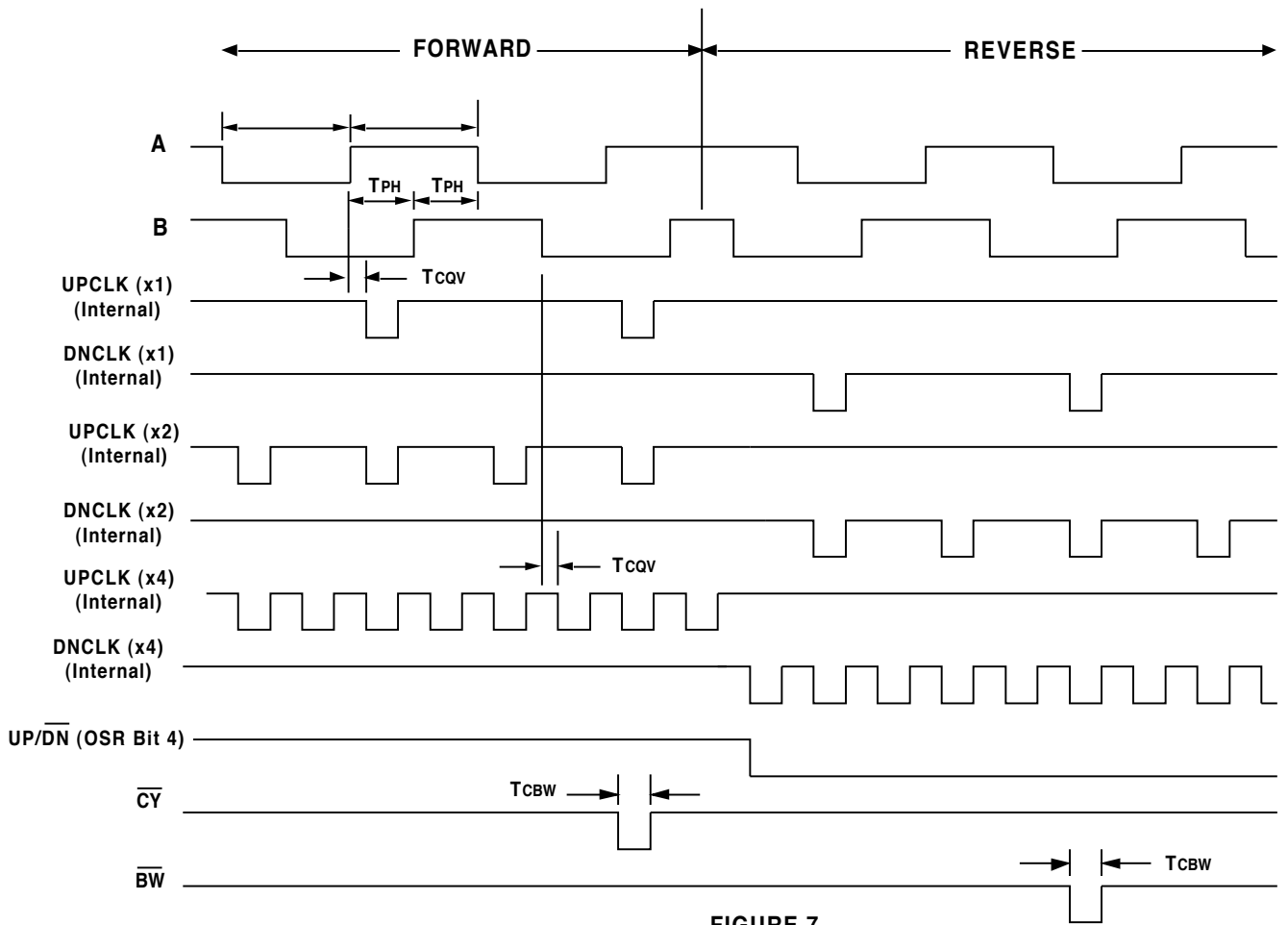
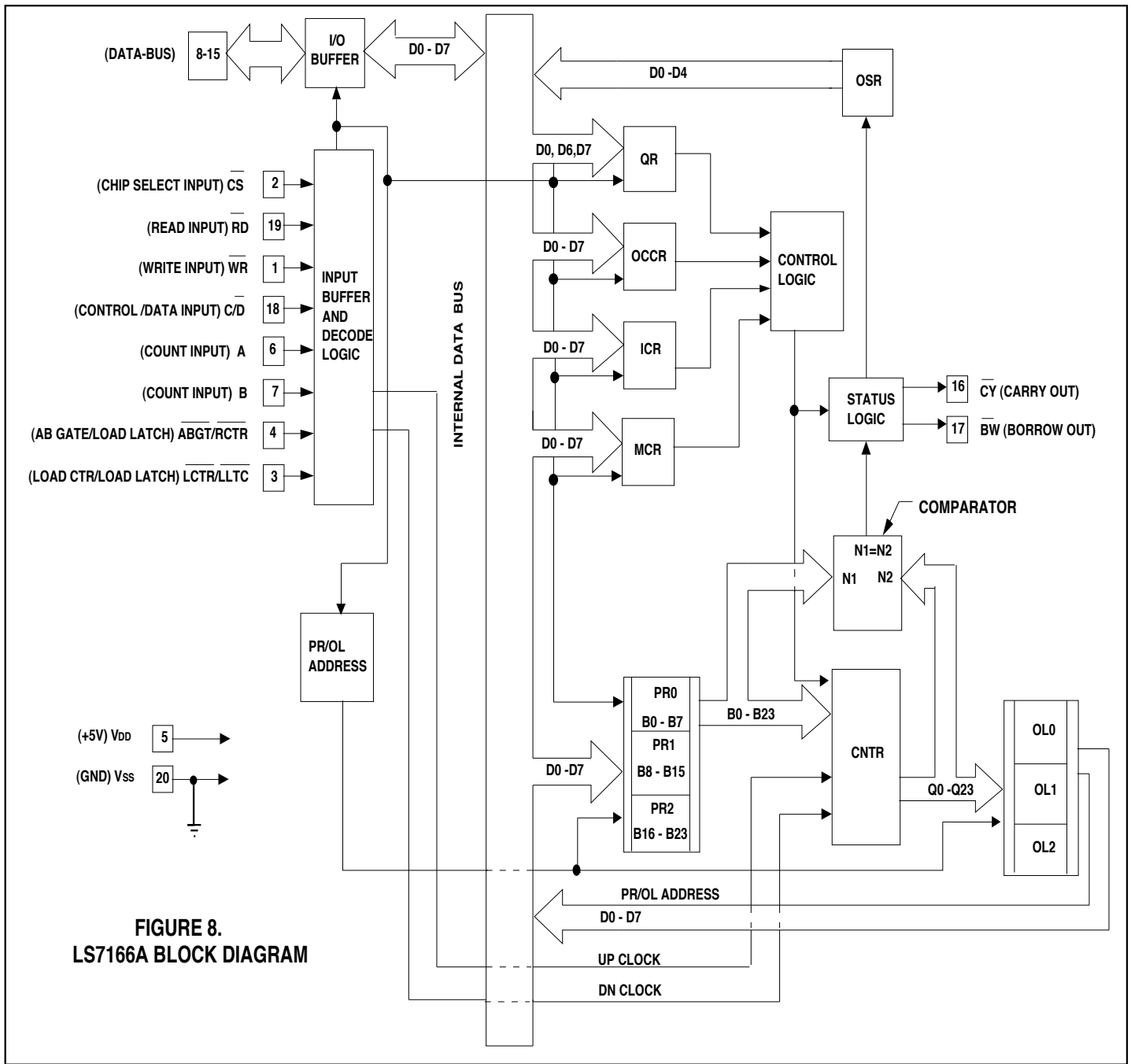


FIGURE 6. CYCLE ONCE MODE





**FIGURE 7.**  
**QUADRATURE MODE INTERNAL CLOCKS**



**FIGURE 8.**  
**LS7166A BLOCK DIAGRAM**

FIGURE 9. 8751 INTERFACE TO LS7166A IN I/O MODE

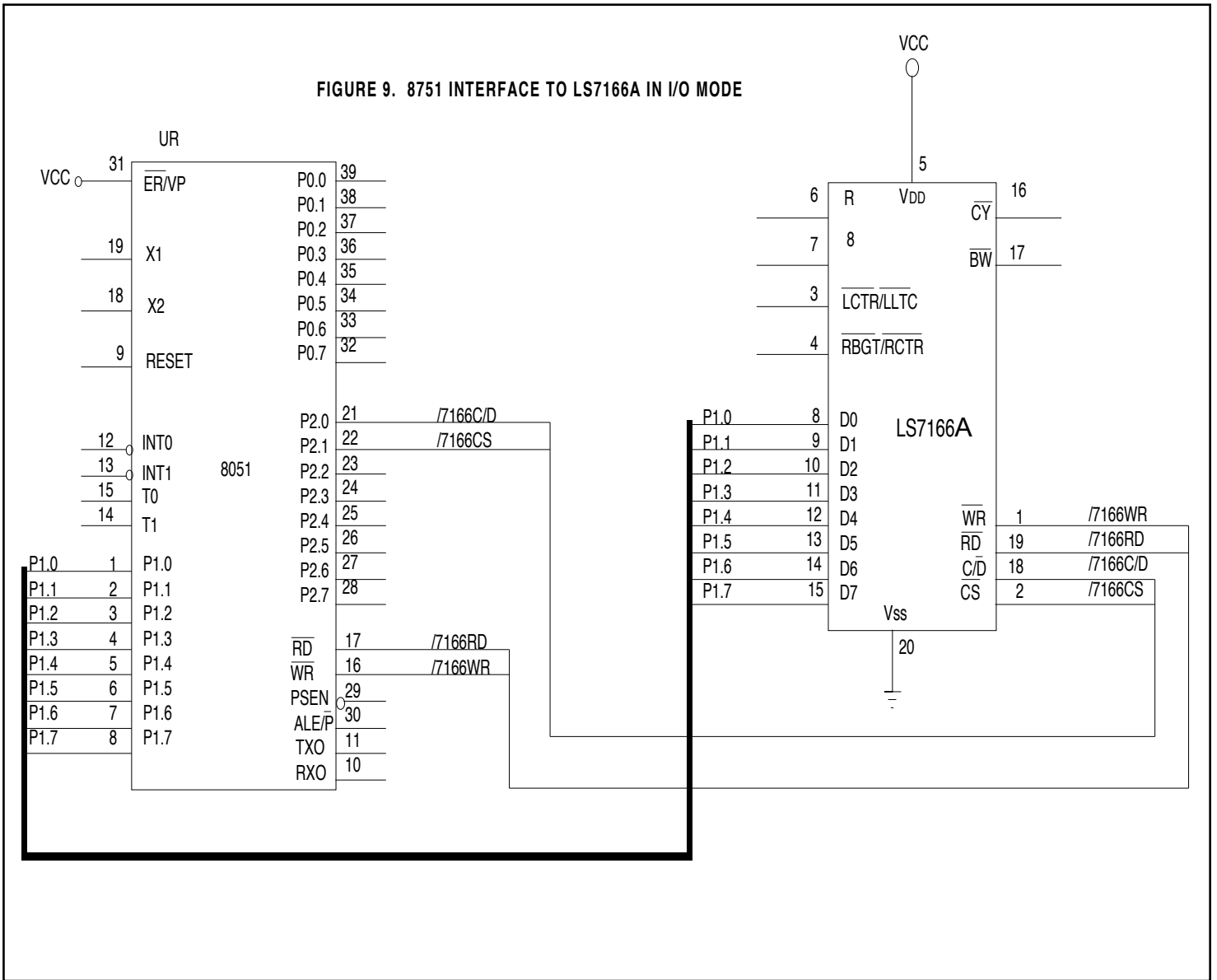
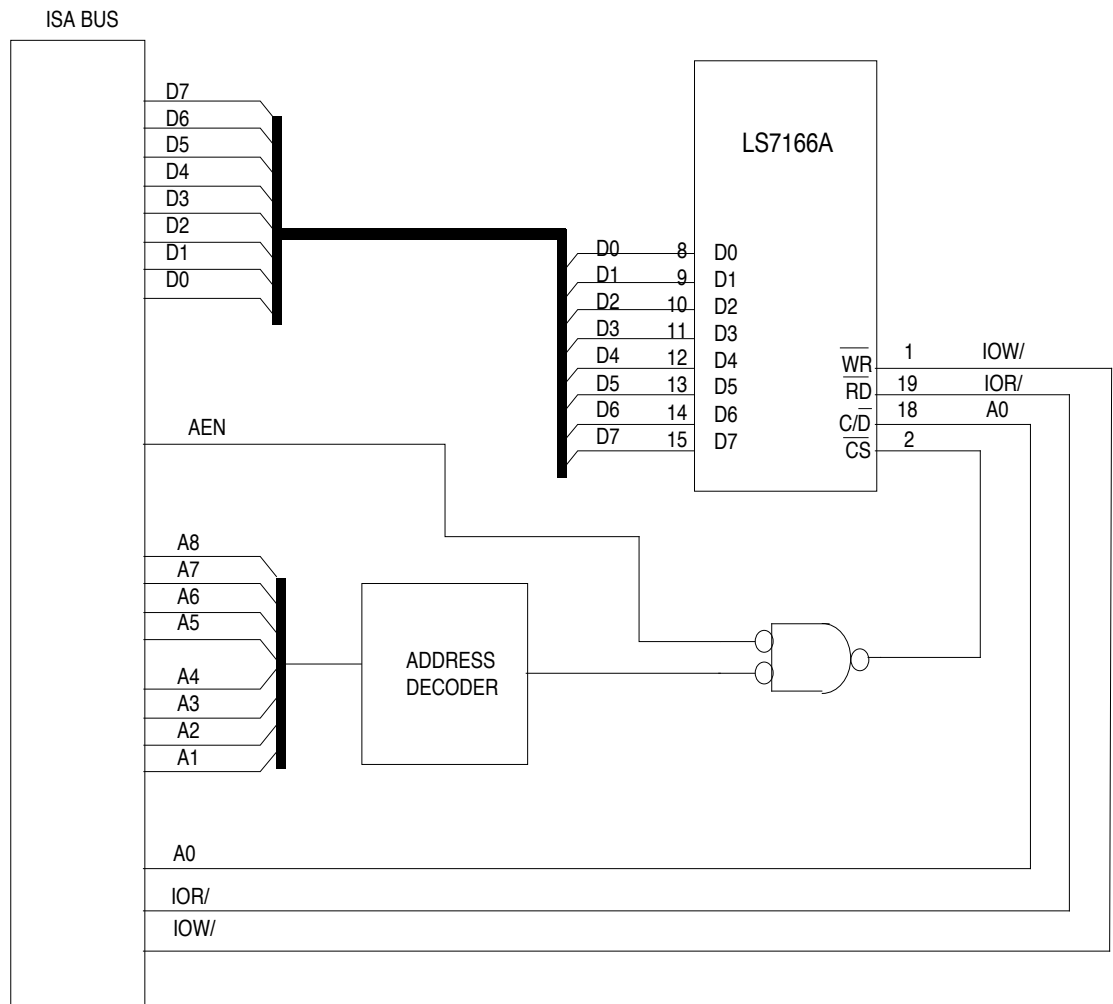


FIGURE 10. LS7166A INTERFACE EXAMPLE



## C Sample Routines for Interfacing with LS7166A

```
#include <stdio.h>
#include <stdlib.h>
#include <conio.h>

#define DATAMODE(arg) (arg + 0)
#define CTRLMODE(arg) (arg + 1)

/*****/
/* MCR (Master Control Register) */

/* Select MCR */
#define MCR(arg) (arg | 0x00)

/* Master Reset */
/* Reset CNTR, ICR, OCCR, QR, BWT, CYT, OL, COMPT, and PR/OL Byte Pointer */
/* Set PR and SIGN */
#define Rst_Master 0x20

/* Reset COMPT */
#define Rst_COMPT 0x10

/* Transfer PR to CNTR (24 bits) */
#define Trf_PR_CNTR 0x08

/* Reset CNTR, BWT and CYT */
/* Set SIGN bit */
#define Rst_CNTR_BWT_CYT_Set_SIGN 0x04

/* Transfer CNTR to OL (24 bits) */
#define Trf_CNTR_OL 0x02

/* Reset PR/OL Byte Pointer */
#define Rst_BP 0x01

/*****/
/* ICR (Input Control Register) */

/* Select ICR */
#define ICR(arg) (arg | 0x40)

/* Select  $\overline{\text{LCTR}}$  /  $\overline{\text{LLTC}}$  as Load-CNTR Input */
#define LCNTR 0x00

/* Select  $\overline{\text{LCTR}}$  /  $\overline{\text{LLTC}}$  as Load-OL Input */
#define LOL 0x20

/* Select  $\overline{\text{ABGT}}$  /  $\overline{\text{RCTR}}$  as Reset-CNTR Input */
#define RCNTR 0x00

/* Select  $\overline{\text{ABGT}}$  /  $\overline{\text{RCTR}}$  as Enable / Disable Gate for A / B Inputs */
#define ABGate 0x10

/* Disable A / B Inputs */
#define DisAB 0x00

/* Enable A / B Inputs */
#define EnAB 0x08
```

```

/* Decrement CNTR once for A / B = 1, if A / B inputs are enabled */
#define Decr_CNTR    0x04

/* Increment CNTR once for A / B = 1, if A / B inputs are enabled */
#define Incr_CNTR    0x02

/* Set Input A = Up Count Input, Input B = Down Count Input */
#define AUP_BDN     0x00

/* Set Input A = Count Input, Input B = Count Direction Input */

/* B = 0 selects Up Count Mode */
/* B = 1 selects Down Count Mode */
#define AIN_BDIR   0x01

/*****/
/* OCCR (Output Control Register) */

/* Select OCCR */
#define OCCR(arg)  (arg | 0x80)

/* Set  $\overline{CY}$  =  $\overline{COMP}$  Comparator Out (active "0") */

/* Set  $\overline{BW}$  =  $\overline{COMPT}$  Comparator Toggle Output */
#define COMPN_COMPT 0x30

/* Set  $\overline{CY}$  =  $\overline{CY}$  */

/* Set  $\overline{BW}$  =  $\overline{BW}$  */
#define CY_BW      0x20

/* Set  $\overline{CY}$  =  $\overline{CY}$  */

/* Set  $\overline{BW}$  =  $\overline{BW}$  */
#define CYN_BWN   0x00

/* Set Binary or BCD Count Mode */
#define Bin_BCD_Cnt 0x00

/* Set 24 Hr Clock Mode – Overrides BCD / Binary Modes */
#define Clk_24HR_Cnt 0x08

/* Set Normal Count Mode */
#define Nrml_Cnt 0x00

/* Set Divide by N Count Mode */
#define div_N_Cnt 0x04

/* Set Non Recycle Count Mode */
#define Nrcyc_Cnt 0x02

/* Set Binary Count Mode */
#define Bin_Cnt 0x00

/* Set BCD Count Mode */
#define BCD_Cnt 0x01

/*****/

```

```

/* QR (Quadrature Register) */

/* Select QR */
#define QR(arg) (arg | 0xC0)

/* Enable x4 Quadrature Mode */
#define En_x4QM 0x03

/* Enable x2 Quadrature Mode */
#define En_x2QM 0x02

/* Enable x1 Quadrature Mode */
#define En_x1QM 0x01

/* Disable Quadrature Mode */
#define Dis_QM 0x00

/*****/
/* Initialize 7166A */

void Init_7166A(int Addr)

/* Initialize 7166A as follows
Do a Master Reset
Set ICR as follows
Set Input A = Up Count
Set Input B = Down Count
Disable Inputs A/B
Enable Reset_CNTR input
Enable Load_CNTR input
Set OCCR – Normal Count Mode
Disable QM
Enable A and B Inputs
*/

void Init_7166A(int Addr){
/* Master Reset */
outp(CTRLMODE(Addr), MCR(Rst_Master));

/* Set ICR */
outp(CTRLMODE(Addr), ICR(AUP_BDN + DisAB + RCNTR + LCNTR));

/* Set OCCR */
outp(CTRLMODE(Addr), OCCR(Nrml_Cnt));

/* Set QR */
outp(CTRLMODE(Addr), QR( Dis_QM));

/*Enable A and B inputs */
outp(CTRLMODE(Addr), ICR(EnAB));
}

```

```
/* Write data into 7166A Preset Register
Addr has address of 7166A counter
Data has 24 bit data to be written to PR register */
```

```
void Write_7166A_PR(int Addr, unsigned long Data);
```

```
void Write_7166A_PR(int Addr, unsigned long Data){
outp(CTRLMODE(Addr), MCR(Rst_BP));
outp(DATAMODE(Addr), (unsigned char)Data);
Data >>= 8;
outp(DATAMODE(Addr), (unsigned char)Data);
Data >>= 8;
outp(DATAMODE(Addr), (unsigned char)Data);
}
```

```
/* Read 7166A Output Latch
Addr has address of 7166A counter
Data returns 24 bit OL register value. */
```

```
unsigned long Read_7166A_OL(int Addr);
```

```
unsigned long Read_7166A_OL(int Addr){
unsigned long Data = 0;
outp(CTRLMODE(Addr), MCR(Rst_BP + Trf_CNTR_OL));
Data |= (unsigned long) inp(DATAMODE(Addr));
lrotr(Data,8);
Data |= (unsigned long) inp(DATAMODE(Addr));
lrotr(Data,8);
Data |= (unsigned long) inp(DATAMODE(Addr));
lrotr(Data,16);
return(Data);
}
```

```
/* Read Output Status Register
Addr has address of 7166A counter
returns OSR data */
```

```
unsigned long Read_7166A_OSR(int Addr);
```

```
unsigned long Read_7166A_OSR(int Addr){
return(inp(CNTRLMODE(Addr)));
}
```