High Speed CMOS Presettable Synchronous 4-Bit Binary Counters

QS54/74FCT193T

QS54/74FCT2193T

FEATURES/BENEFITS

- Pin and function compatible to the 74F193 74FCT193 and 74FCT193T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 193T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- Std. and A speed grades with 6.5 ns t_{PD} for A
- I_{OL} =48 mA Com., 32 mA Mil.

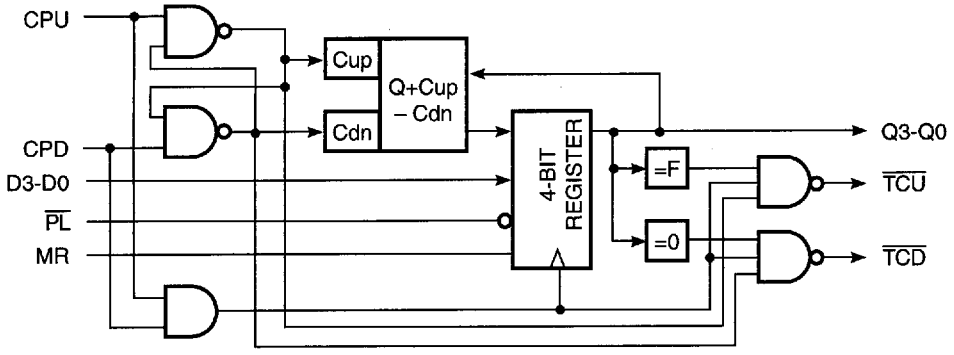
FCT-T 2193T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std. and A speed grades with 6.5 ns t_{PD} for A
- I_{OL} = 12 mA Com.

DESCRIPTION

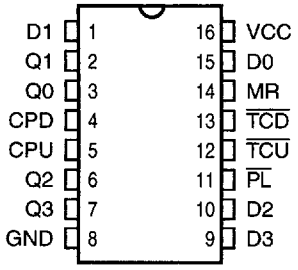
The QSFCT193 is a high-speed CMOS 4-bit binary up/down counter. It has separate up and down clock inputs, up/down ripple clock outputs and an asynchronous clear input. The '193 has asynchronous preload inputs which override the count inputs. The '2193 is a 25Ω resistor output version of the193, and is useful for driving transmission lines and reducing system noise. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM

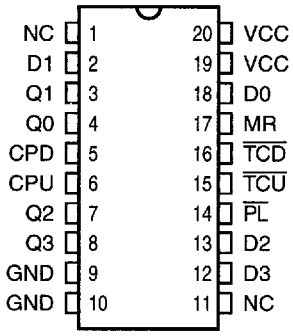


PIN CONFIGURATIONS (All Pins Top View)

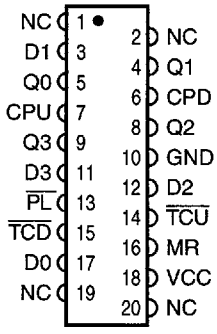
PDIP, SOIC, QSOP



HQSOP



ZIP



Note:
Available in both 150 mil wide SOIC (package code S1) and 300 mil SOIC (package code SO).

PIN DESCRIPTION

Name	I/O	Description
D3-D0	I	Data Inputs
Q3-Q0	O	Data Outputs
$\overline{PL}$	I	Pre Load
MR	I	Master Reset
CPU	I	Count Up Clock
CPD	I	Count Down Clock
$\overline{TCU}$	O	Terminal Count Up
$\overline{TCD}$	O	Terminal Count Down

FUNCTION TABLE

Inputs					Outputs			
$\overline{PL}$	MR	CPU	CPD	Di	Q3-Q0	$\overline{TCU}$	$\overline{TCD}$	Function
X	H	X	L	X	0000	X	L	Reset
X	H	X	H	X	0000	X	H	Reset
L	L	X	X	D3-D0	D3-D0	X	X	Load Data
H	L	↑	H	X	Q+1	X	X	Count Up
H	L	H	↑	X	Q-1	X	X	Count Down
H	L	L	H	X	F	L	H	Count Up = 1111
H	L	H	H	X	0-E	H	H	Count Up ≠ 1111
H	L	H	L	X	0	H	L	Count Down = 0000
H	L	H	H	X	1-F	H	H	Count Down ≠ 0000

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20 mA
DC Output Diode Current with $V_{OUT} < 0$	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1, 4, 5, 9-11, 14, 15	4	4	5	7	pF
2, 3, 6, 7, 12, 13	6	6	7	9	pF
—	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	V_{CC} = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX)	V_{CC} = Max., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	V_{CC} = Min., I_{OL} = 32 mA (MIL) I_{OL} = 48 mA (COM)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX- 25Ω)	V_{CC} = Min., I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX- 25Ω)	V_{CC} = Min., I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		193 2193 Min	193 2193 Max	193A 2193A Min	193A 2193A Max	Unit
t_{CPTC}	Propagation Delay CPU/D to $\overline{TCU}/\overline{TCD}$	Com	2.0	10	2.0	6.5	ns
		Mil	2.0	10.5	2.0	6.9	
t_{CPQ}	Propagation Delay CPU/D to Qi	Com	2.0	13.5	2.0	8.8	ns
		Mil	2.0	14	2.0	9.1	
t_{DQ}	Propagation Delay Di to Qi	Com	2.0	15.5	2.0	10.1	ns
		Mil	1.5	16.5	2.0	10.8	
t_{PLQ}	Propagation Delay $\overline{PL}$ to Qi	Com	2.0	14	2.0	8.8	ns
		Mil	2.0	13.5	2.0	9.1	
t_{MRQ}	Propagation Delay MR to Qi	Com	3.0	15.5	3.0	10.1	ns
		Mil	3.0	16	3.0	10.4	
t_{MRTCU}	Propagation Delay MR to $\overline{TCU}$	Com	3.0	14.5	3.0	9.4	ns
		Mil	3.0	15	3.0	9.8	
t_{MRTCD}	Propagation Delay MR to $\overline{TCD}$	Com	3.0	15.5	3.0	10.1	ns
		Mil	3.0	16	3.0	10.4	
t_{PLTC}	Propagation Delay $\overline{PL}$ to $\overline{TCU}/\overline{D}$	Com	3.0	16.5	3.0	10.8	ns
		Mil	3.0	18.5	3.0	12	
t_{DTC}	Propagation Delay Di to $\overline{TCU}/\overline{D}$	Com	3.0	15.5	3.0	10.1	ns
		Mil	3.0	16.5	3.0	10.8	

Notes:
1. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

TIMING REQUIREMENTS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		193 2193 Min	193 2193 Max	193A 2193A Min	193A 2193A Max	Unit
t_{DPLS}	Di to $\overline{PL}$	Com Mil	5.0 6.0		4.0 5.0		ns
t_{DPLH}	Di to $\overline{PL}$	Com Mil	2.0 2.0		1.5 1.5		ns
t_{PLW}	$\overline{PL}$ Low Time	Com Mil	6.0 7.5		5.0 6.5		ns
t_{CP}	CPU/D Pulse Width HIGH and LOW	Com(1) Mil(1)	5.0 7.0		4.0 6.0		ns
t_{CPL}	CPU/D Pulse Width LOW (change of direction)	Com(1) Mil(1)	10 12		8.0 10		ns
t_{MRH}	MR High Time	Com(1) Mil(1)	6.0 6.0		5.0 5.0		ns
t_{RPLCR}	$\overline{PL}$ to CPU/D Recovery	Com(1) Mil(1)	6.0 8.0		5.0 7.0		ns
t_{RMRCP}	MR to CPU/D Recovery	Com(1) Mil(1)	4.0 4.5		3.0 3.5		ns

Notes:

1. This parameter is guaranteed by design but not tested.
2. See Test Circuit and Waveforms.