



Integrated Device Technology, Inc.

# FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161T/AT/CT  
IDT54/74FCT163T/AT/CT

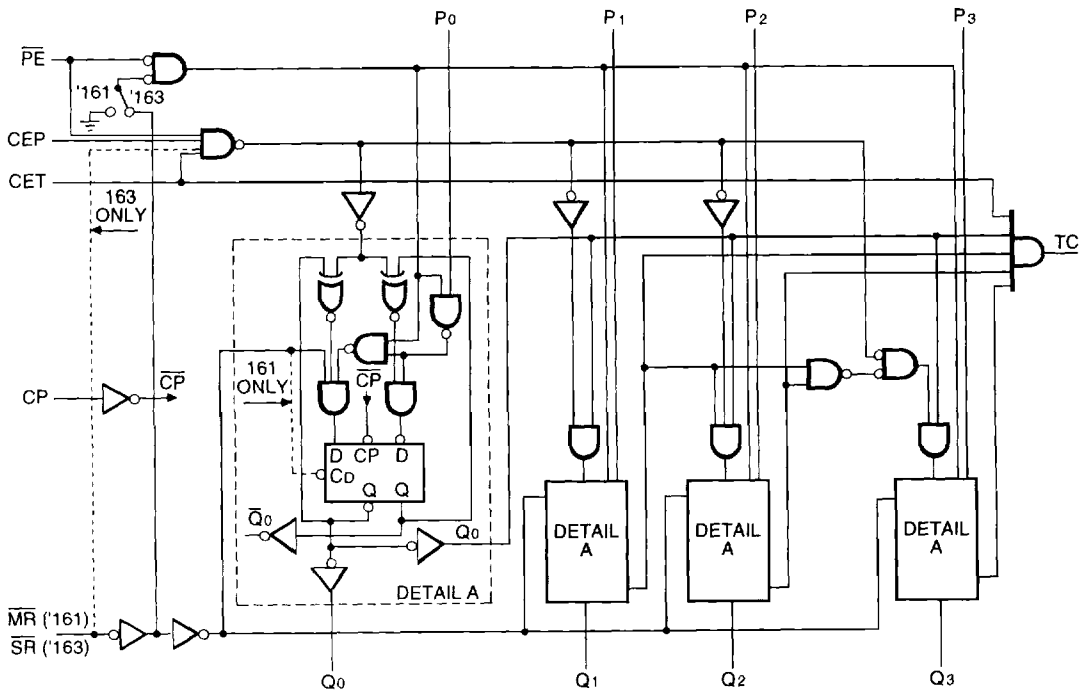
## FEATURES:

- Std., A and C speed grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- High drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

## DESCRIPTION:

The IDT54/74FCT161T/163T, IDT54/74FCT161AT/163AT and IDT54/74FCT161CT/163CT are high-speed synchronous modulo-16 binary counters built using an advanced dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161T/AT/CT have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163T/AT/CT have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

## FUNCTIONAL BLOCK DIAGRAMS



2611 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

OCTOBER 1994

©1995 Integrated Device Technology, Inc.

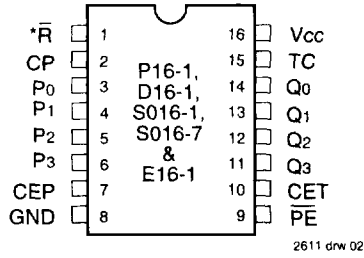
6.7

DSC-42194

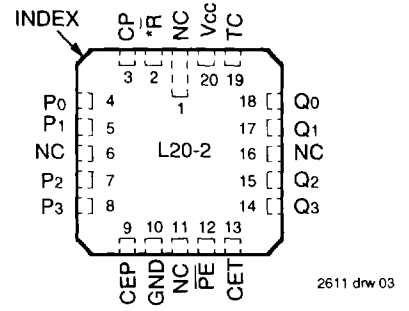
1

6

**PIN CONFIGURATIONS**



DIP/SOIC/QSOP/CERPACK  
TOP VIEW



LCC  
TOP VIEW

\*MR for '161  
\*SR for '163

**PIN DESCRIPTION**

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
MR ('161)	Asynchronous Master Reset Input (Active LOW)
SR ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

2611 lbl 01

**FUNCTION TABLE<sup>(2)</sup>**

SR <sup>(1)</sup>	PE	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:  
1. 163 only.  
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

2611 tbl 0:

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	-0.5 to Vcc +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2611 lnk 03

- NOTES:  
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.  
2. Input and Vcc terminals only.  
3. Outputs and I/O terminals only.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unl
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE:  
1. This parameter is measured at characterization but not tested.

2611 nk

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		COM'L <sup>(5)</sup>	2.0V	—	V
				MIL	2.7V	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IiH	Input HIGH Current <sup>(4)</sup>	VCC = Max.	VI = 2.7V	—	—	±1	µA
IiL	Input LOW Current <sup>(4)</sup>	VCC = Max.	VI = 0.5V	—	—	±1	µA
Ii	Input HIGH Current <sup>(4)</sup>	VCC = Max., VI = VCC (Max.)		—	—	±1	µA
Vik	Clamp Diode Voltage	VCC = Min., IN = -18mA		—	-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. <sup>(3)</sup> , VO = GND		-60	-120	-225	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL		IOH = -6mA MIL.	2.4	3.3	V
				IOH = -8mA COM'L.	—	—	—
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL		IOH = -12mA MIL.	2.0	3.0	V
				IOH = -15mA COM'L.	—	—	—
VH	Input Hysteresis	—		—	200	—	mV
Icc	Quiescent Power Supply Current	VCC = Max. VIN = GND or VCC		—	0.01	1	mA

**NOTES:**

2611 tbi 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at TA = -55°C.
5. Clock pin requires a minimum VIH of 2.5V.



**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $\overline{CEP} = \overline{CET} = \overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25 mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{CEP} = \overline{CET} = \overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5 mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.5
		$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{CEP} = \overline{CET} = \overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ Four Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 <sup>(5)</sup>
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.0	12.3 <sup>(5)</sup>

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{DH} \text{NT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $\text{NT} = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

2611 tbl 0f

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT161T IDT54/74FCT163T				IDT54/74FCT161AT IDT54/74FCT163AT				IDT54/74FCT161CT IDT54/74FCT163CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to Q <sub>n</sub> (PE Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to Q <sub>n</sub> (PE Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
tPHL	Propagation Delay MR to Q <sub>n</sub> ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
tPHL	Propagation Delay MR to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
tsu	Set-up Time, HIGH or LOW P <sub>n</sub> to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
th	Hold Time, HIGH or LOW P <sub>n</sub> to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
tsu	Set-up Time, HIGH or LOW PE or SR to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
th	Hold Time, HIGH or LOW PE or SR to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tsu	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
th	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tw	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	ns
tw	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
tw	MR Pulse Width, LOW ('161)	5.0	—	5.0	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	ns	
tREM	Recovery Time MR to CP ('161)	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	

**NOTES:**

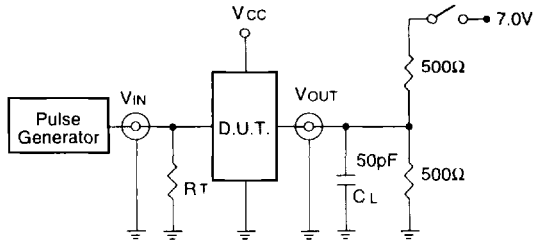
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

2611 tbl 07

**6**

**TEST CIRCUITS AND WAVEFORMS**

**TEST CIRCUITS FOR ALL OUTPUTS**



2611 drw 04

**SWITCH POSITION**

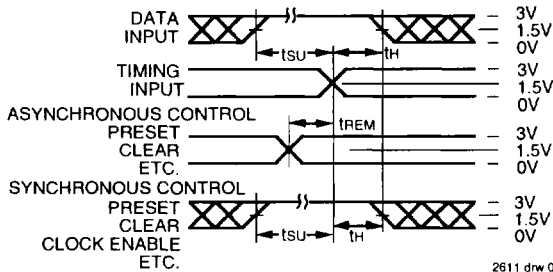
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

**DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.  
 RT = Termination resistance: should be equal to Zout of the Pulse Generator.

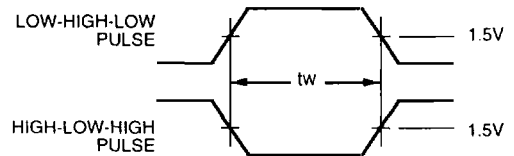
2611 Ink 08

**SET-UP, HOLD AND RELEASE TIMES**



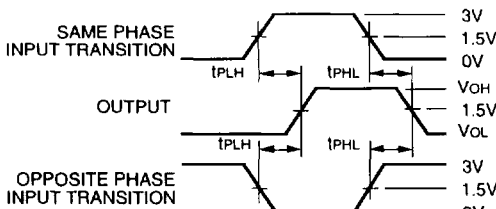
2611 drw 05

**PULSE WIDTH**



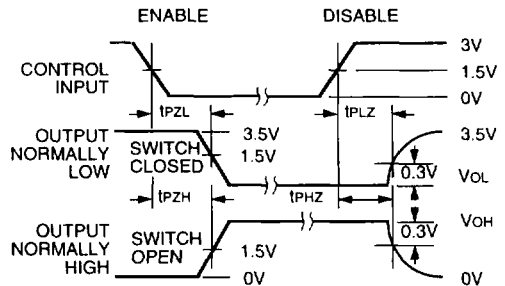
2611 drw 06

**PROPAGATION DELAY**



2611 drw 07

**ENABLE AND DISABLE TIMES**

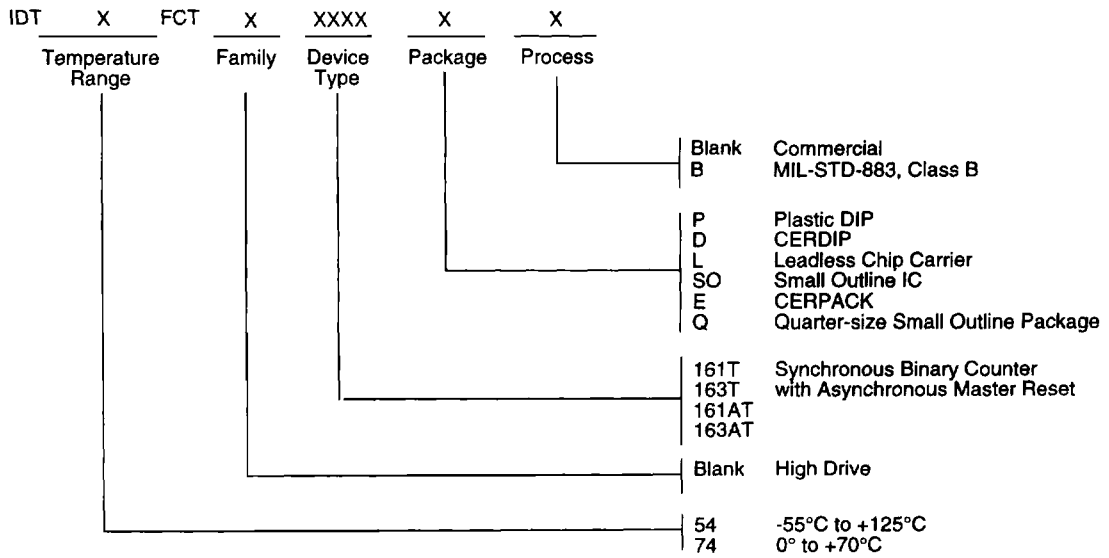


2611 drw 08

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tr ≤ 2.5ns

**ORDERING INFORMATION**



2611 drw 09