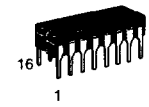
Presettable Counters
High–Performance Silicon–Gate CMOS

MC54/74HCT161A
MC54/74HCT163A

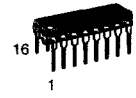
The MC54/74HCT161A and HCT163A are identical in pinout to the LS161A and LS163A. These devices may be used as level converters for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT161A and HCT163A are programmable 4–bit binary counters with asynchronous and synchronous reset, respectively.

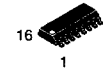
- Output Drive Capability: 10 LSTTL Loads
- TTL, NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 200 FETs or 50 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620–10



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

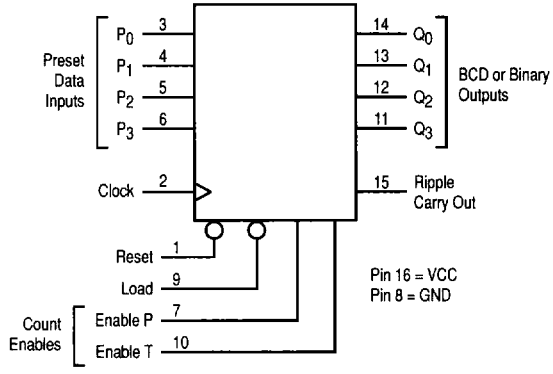


D SUFFIX
SOIC PACKAGE
CASE 751B–05

ORDERING INFORMATION

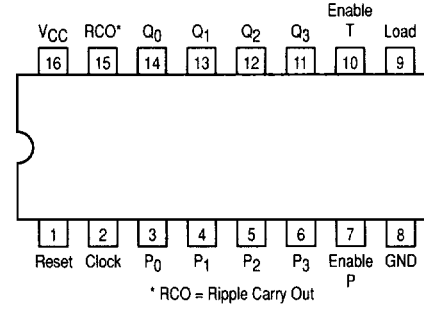
MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC

LOGIC DIAGRAM



Device	Count Mode	Reset Mode
HCT161A	Binary	Asynchronous
HCT163A	Binary	Synchronous

Pinout: 16–Lead Package (Top View)



* RCO = Ripple Carry Out

FUNCTION TABLE

Inputs					Output Q
Clock	Reset*	Load	Enable P	Enable T	
↑	L	X	X	X	Reset
↑	H	L	X	X	Load Preset Data
↑	H	H	H	H	Count
↑	H	H	L	X	No Count
↑	H	H	X	L	No Count

H = High Level; L = Low Level; X = Don't Care
* = HCT163A only. HCT161A is an "Asynchronous–Reset" device.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package Ceramic DIP	 260 300	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

3

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	Guaranteed Limit			Unit
			V	– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} = –1.0V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.80 0.80	0.80 0.80	0.80 0.80	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98	3.84	3.70	V
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	4.5 5.5	0.10 0.10	0.10 0.10	0.10 0.10	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.40	V
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.10	± 1.00	± 1.00	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in} = V_{CC} or GND I_{out} – 0 μA	5.5	4	40	160	μA
I_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input V_{IN} = V_{CC} or GND Other Inputs I_{out} – 0 μA	 5.5	≥–55°C 2.9	25 to +125°C 2.4		mA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%: C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig	Guaranteed Limit			Unit
			– 55 to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)*	1,7	30	24	20	MHz
t_{PLH}	Maximum Propagation Delay Clock to Q	1,7	20	23	28	ns
t_{PHL}		1,7	25	30	32	ns
t_{PHL}	Maximum Propagation Delay Reset to Q (HCT161A Only)	2,7	25	29	33	ns
t_{PLH}	Maximum Propagation Delay Enable T to Ripple Carry Out	3,7	16	18	20	ns
t_{PHL}		3,7	21	24	28	ns
t_{PLH}	Maximum Propagation Delay Clock to Ripple Carry Out	1,7	22	25	28	ns
t_{PHL}		1,7	28	33	35	ns
t_{PHL}	Maximum Propagation Delay Reset to Ripple Carry Out (HCT161A Only)	2,7	24	28	32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2,7	15	19	22	ns
C_{in}	Maximum Input Capacitance	1,7	10	10	10	pF

* Applies to noncascaded/nonsynchronous clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f_{max}. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f_{max} in the table above is applicable. See Applications information in this data sheet.

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	60	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

3

TIMING REQUIREMENTS (V_{CC} = 5.0 V ±10%: C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			– 55 to 25°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock	5	12	18	20	ns
	Minimum Setup Time, Load to Clock	5	12	18	20	ns
	Minimum Setup Time, Reset to Clock (HCT163A Only)	4	12	18	20	ns
	Minimum Setup Time, Enable T or Enable P to Clock	6	12	18	20	ns
t_h	*Minimum Hold Time, Clock to Preset Data Inputs*	5	3	3	3	ns
	Minimum Hold Time, Clock to Load	5	3	3	3	ns
	Minimum Hold Time, Clock to Reset (HCT163A Only)	4	3	3	3	ns
	Minimum Hold Time, Clock to En T or En P	6	3	3	3	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HCT161A Only)	2	12	17	23	ns
	Minimum Recovery Time, Load Inactive to Clock	2	12	17	23	ns
t_w	Minimum Pulse Width, Clock	1	12	15	18	ns
	Minimum Pulse Width, Reset (HCT161A Only)	1	12	15	18	ns
t_r, t_f	Maximum Input Rise and Fall Times		500	500	500	ns

FUNCTION DESCRIPTION

The HCT161A/163A are programmable 4–bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading and count–enable controls.

The HCT161A and HCT163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip–flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading occur with the rising edge of the Clock input. In addition, control functions, such as resetting (HCT163A) and loading occur with the rising edge of the Clock Input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip–flops and appear at the counter outputs. P0 (Pin 3) is the least–significant bit and P3 (Pin 6) is the most–significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least–significant bit and Q3 (Pin 11) is the most–significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state 1111, this output goes high, providing an external look–ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (pin 1) resets the internal flip–flops and sets the outputs (Q0 through Q3) to a low level. The HCT161A resets asynchronously, and the HCT163A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip–flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Count Enable/Disable

These devices have two count–enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

Count Enable = Enable P • Enable T • Load

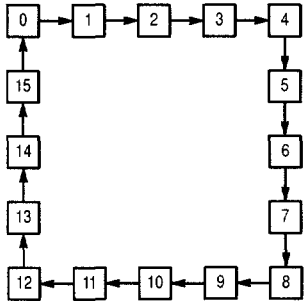
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count–enable control: Enable T is both a count–enable and a Ripple–Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0–Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.

OUTPUT STATE DIAGRAM



Binary Counters

SWITCHING WAVEFORMS

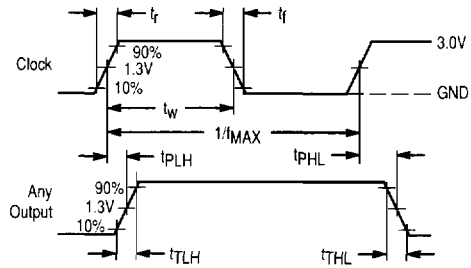


Figure 1.

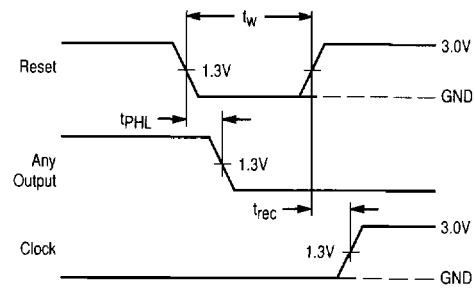


Figure 2.

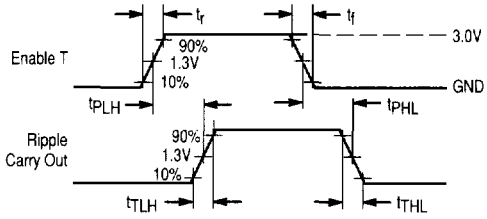


Figure 3.

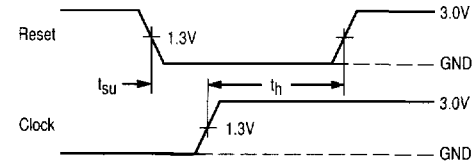


Figure 4. HCT163A Only

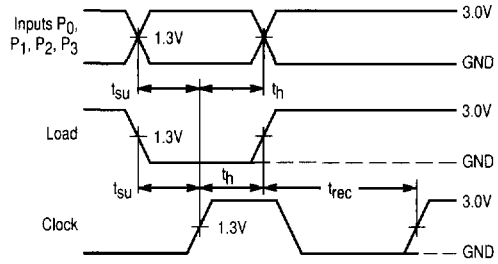


Figure 5.

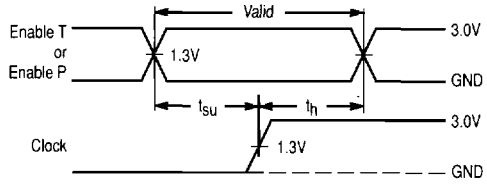
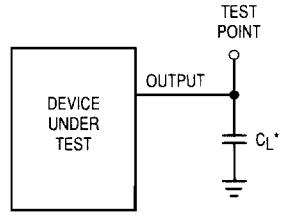
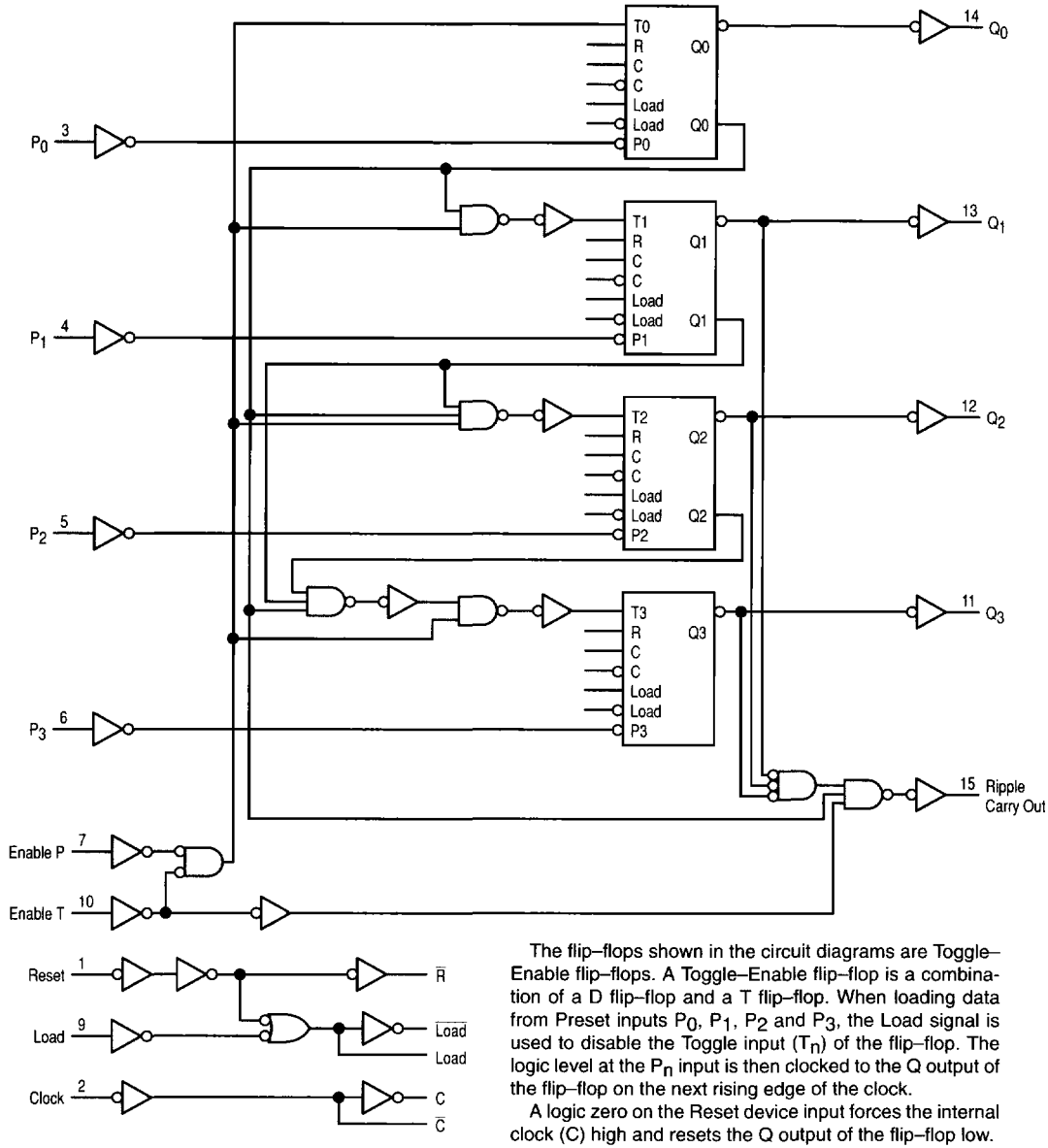


Figure 6.



*Includes all probe and jig capacitance

Figure 7. Test Circuit



The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P_0, P_1, P_2 and P_3, the Load signal is used to disable the Toggle input (T_n) of the flip–flop. The logic level at the P_n input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 8. 4–Bit Binary Counter with Asynchronous Reset (MC54/74HCT161A)

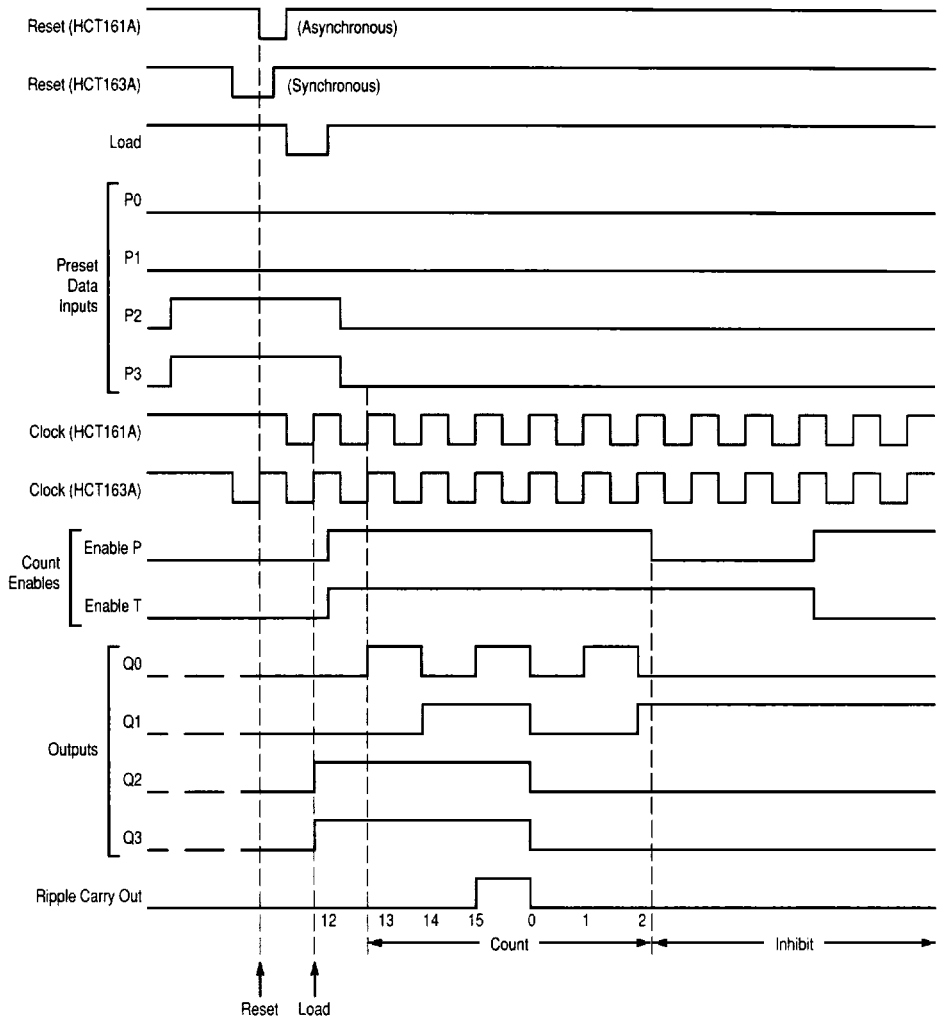
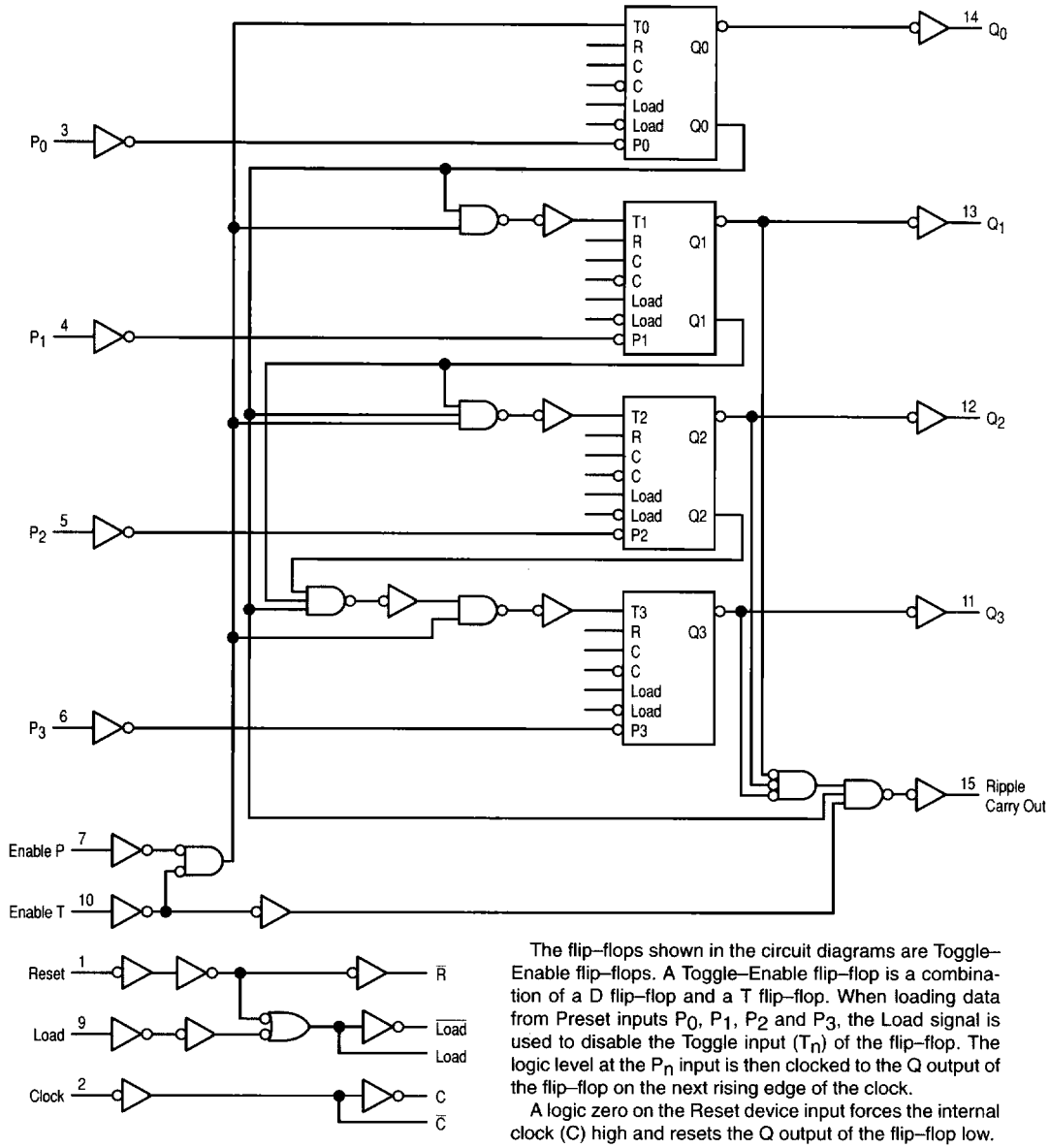


Figure 9. Timing Diagram

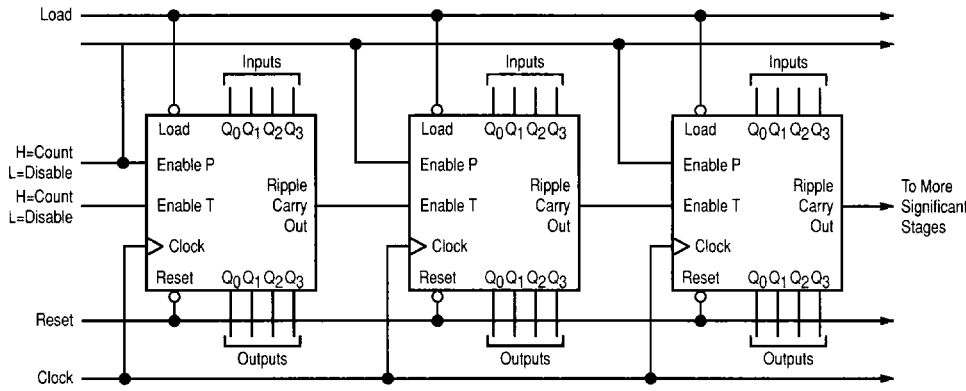


The flip–flops shown in the circuit diagrams are Toggle–Enable flip–flops. A Toggle–Enable flip–flop is a combination of a D flip–flop and a T flip–flop. When loading data from Preset inputs P_0, P_1, P_2 and P_3, the Load signal is used to disable the Toggle input (T_n) of the flip–flop. The logic level at the P_n input is then clocked to the Q output of the flip–flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip–flop low.

Figure 10. 4–Bit Binary Counter with Synchronous Reset (MC54/74HCT163A)

TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set–up times between Enable (port) and clock.

Figure 11. N–Bit Synchronous Counters

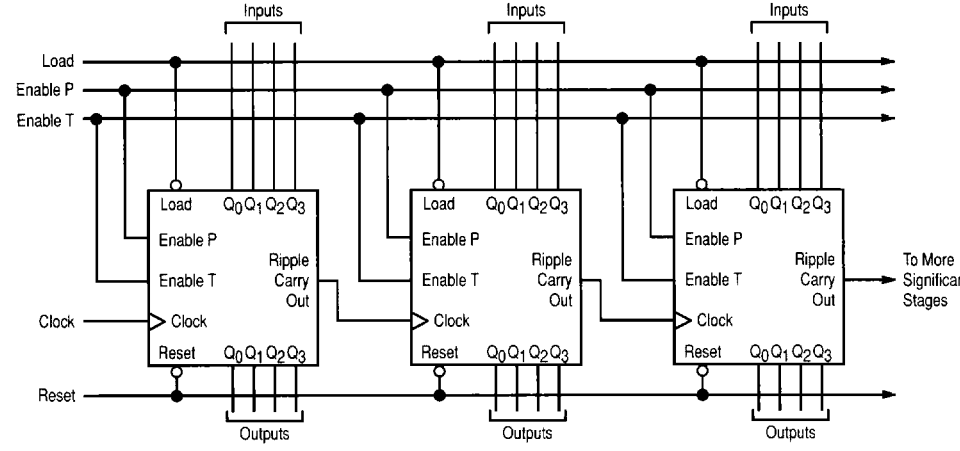


Figure 12. Nibble Ripple Counter

TYPICAL APPLICATIONS VARYING THE MODULUS

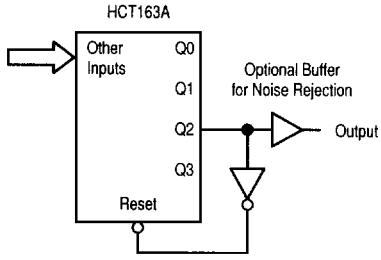


Figure 13. Modulo–5 Counter

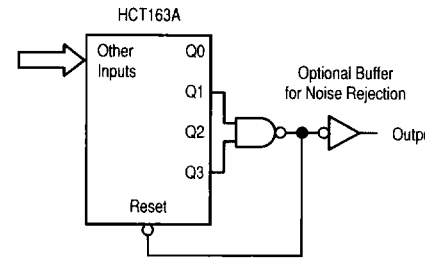


Figure 14. Modulo–11 Counter

The HCT163A facilitates designing counters of any modulus with minimal external logic. The output is glitch–free due to the synchronous Reset.

3