



**FAST CMOS  
SYNCHRONOUS  
PRESETTABLE  
BINARY COUNTERS**

**IDT54/74FCT161/A  
IDT54/74FCT163/A**

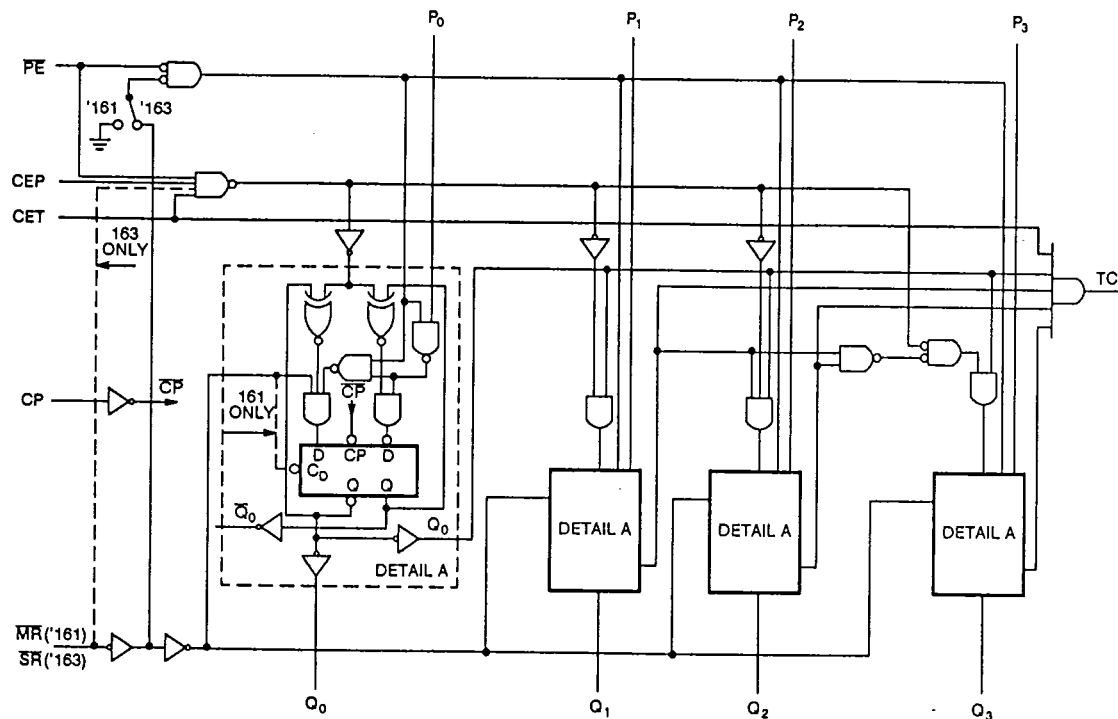
**FEATURES:**

- IDT54/74FCT161/163 equivalent to FAST™ speed;  
IDT54/74FCT161A/163A 35% faster than FAST™
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- $I_{OL} = 48\text{mA}$  (commercial), 32mA (military)
- CMOS power levels (5 $\mu\text{W}$  typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST™ (5 $\mu\text{A}$  max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

**DESCRIPTION:**

The IDT54/74FCT161/163 and IDT54/74FCT161A/163A are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161 and IDT54/74FCT161A have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163 and IDT54/74FCT163A have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

**FUNCTIONAL BLOCK DIAGRAM**



CEMOS is a trademark of Integrated Device Technology, Inc.  
FAST is a trademark of Fairchild Semiconductor Company

**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

DECEMBER 1987

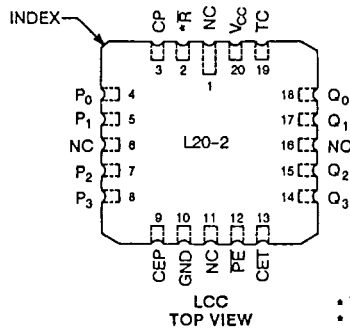
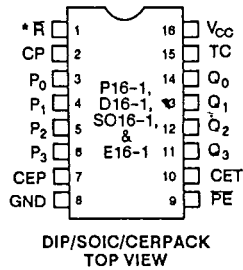
4825771 INTEGRATED DEVICE

97D 02271 D

IDT54/74FCT161/A & IDT54/74FCT163/A FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS



\* MR FOR '161  
\* SR FOR '163

ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

T-45-23-17

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Commercial: T<sub>A</sub> = 0°C to +70°C; V<sub>CC</sub> = 5.0V ± 5%

Military: T<sub>A</sub> = -55°C to +125°C; V<sub>CC</sub> = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT		
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic High Level	2.0	-	-	V		
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic Low Level	-	-	0.8	V		
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max. V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V V <sub>I</sub> = 0.5V V <sub>I</sub> = GND	-	-	5	μA		
I <sub>IL</sub>	Input LOW Current		-	-	-5 <sup>(4)</sup>			
V <sub>IK</sub>	Clamp Diode Voltage		V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	-	-0.7		-1.2	V
I <sub>OS</sub>	Short Circuit Current		V <sub>CC</sub> = Max <sup>(3)</sup> , V <sub>O</sub> = GND	-60	-120		-	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32 μA	V <sub>HC</sub>	V <sub>CC</sub>	-	V		
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -300 μA	V <sub>HC</sub>	V <sub>CC</sub>			
			I <sub>OH</sub> = -12mA MIL. I <sub>OH</sub> = -15mA COM'L.	2.4	4.3		-	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300 μA	-	GND	V <sub>LC</sub>	V		
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 300 μA	-	GND		V <sub>LC</sub>	
			I <sub>OL</sub> = 32mA MIL.	-	0.3		0.5	
			I <sub>OL</sub> = 48mA COM'L.	-	0.3		0.5	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

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97D 02272 D

IDT54/74FCT161/A & IDT54/74FCT163/A FAST  
CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT161/A)

T-45-23-17

$V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)	MIN.	TYP.(2)	MAX.	UNIT	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{CC} \geq V_{HC}; V_{IN} \leq V_{LC}$ $I_{CP} = I_I = 0$	-	0.001	1.5	mA	
$\Delta I_{CC}$	Power Supply Current per TTL Input HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V(3)$	-	0.5	2.0	mA	
$I_{CCD}$	Dynamic Power Supply Current (4)	$V_{CC} = \text{Max.}$ Outputs Open Load Mode CEP = CET = PE = GND MR = $V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} \text{ (FCT)}$	-	0.15	0.25	mA/MHz
$I_C$	Total Power Supply Current (6)	$V_{CC} = \text{Max.}$ Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle CEP = CET = PE = GND MR = $V_{CC}$ Four Bits Toggling at $f_I = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} \text{ (FCT)}$	-	3.75	7.75(5)	mA
			$V_{IN} = 3.4V \text{ or}$ $V_{IN} = \text{GND}$	-	5.0	12.75(5)	

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT163/A)

$V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS (1)	MIN.	TYP.(2)	MAX.	UNIT	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{CC} \geq V_{HC}; V_{IN} \leq V_{LC}$ $I_{CP} = I_I = 0$	-	0.001	1.5	mA	
$\Delta I_{CC}$	Power Supply Current per TTL Input HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V(3)$	-	0.5	2.0	mA	
$I_{CCD}$	Dynamic Power Supply Current (4)	$V_{CC} = \text{Max.}$ Outputs Open Load Mode CEP = CET = PE = GND SR = $V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} \text{ (FCT)}$	-	0.15	0.25	mA/MHz
$I_C$	Total Power Supply Current (6)	$V_{CC} = \text{Max.}$ Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle CEP = CET = PE = GND SR = $V_{CC}$ Four Bits Toggling at $f_I = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} \text{ (FCT)}$	-	3.75	7.75(5)	mA
			$V_{IN} = 3.4V \text{ or}$ $V_{IN} = \text{GND}$	-	5.0	12.75(5)	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
  - Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient and maximum loading.
  - Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
  - This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
  - Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (I_{CP}/2 + f_I N_I)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_I = \text{Input Frequency}$   
 $N_I = \text{Number of Inputs at } f_I$   
 All currents are in milliamperes and all frequencies are in megahertz.

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97D 02273 D

IDT54/74FCT161/A & IDT54/74FCT163/A FAST  
CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
MR ('161)	Asynchronous Master Reset Input (Active LOW)
SR ('163)	Synchronous Reset Input (Active LOW)
P <sub>0-3</sub>	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q <sub>0-3</sub>	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE (2)

SR (1)	PE	CET	CEP	ACTION ON THE RISING CLOCK EDGE (S)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P <sub>n</sub> → Q <sub>n</sub> )
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:

- For FCT163/163A only.
- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		(1)	IDT54/74FCT161 IDT54/74FCT163					IDT54/74FCT161A IDT54/74FCT163A					
			TYP.(3)	MIL		COM'L		TYP.(3)	MIL		COM'L		
				MIN.(2)	MAX.	MIN.(2)	MAX.		MIN.(2)	MAX.	MIN.(2)	MAX.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> (PE Input HIGH)	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	7.0	2.0	11.5	2.0	11.0	4.5	2.0	7.5	2.0	7.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> (PE Input LOW)		7.0	2.0	10.0	2.0	9.5	4.5	2.0	6.5	2.0	6.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC		10.0	2.0	16.5	2.0	15.0	6.5	2.0	10.8	2.0	9.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC		4.5	1.5	9.0	1.5	8.5	3.0	1.5	5.9	1.5	5.5	ns
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub> (F161)		9.0	2.0	14.0	2.0	13.0	5.9	2.0	9.1	2.0	8.5	ns
t <sub>PHL</sub>	Propagation Delay MR to TC		8.0	2.0	12.5	2.0	11.5	5.2	2.0	8.2	2.0	7.5	ns
t <sub>SU(H)</sub> t <sub>SU(L)</sub>	Set-up Time, HIGH or LOW P <sub>n</sub> to CP		5.0	5.5	-	5.0	-	4.0	4.5	-	4.0	-	ns
t <sub>H(H)</sub> t <sub>H(L)</sub>	Hold Time, HIGH or LOW P <sub>n</sub> to CP		2.0	2.0	-	1.5	-	1.5	2.0	-	1.5	-	ns
t <sub>SU(H)</sub> t <sub>SU(L)</sub>	Set-up Time, HIGH or LOW PE or SR to CP		11.0	13.5	-	11.5	-	9.0	11.5	-	9.5	-	ns
t <sub>H(H)</sub> t <sub>H(L)</sub>	Hold Time, HIGH or LOW PE or SR to CP		2.0	1.5	-	1.5	-	1.5	1.5	-	1.5	-	ns
t <sub>SU(H)</sub> t <sub>SU(L)</sub>	Set-up Time, HIGH or LOW CEP or CET to CP		11.0	13.0	-	11.5	-	9.0	11.0	-	9.5	-	ns
t <sub>H(H)</sub> t <sub>H(L)</sub>	Hold Time, HIGH or LOW CEP or CET to CP		0	0	-	0	-	0	0	-	0	-	ns
t <sub>w(H)</sub> t <sub>w(L)</sub>	Clock Pulse Width (Load) HIGH or LOW		5.0	5.0	-	5.0	-	4.0	4.0	-	4.0	-	ns
t <sub>w(H)</sub> t <sub>w(L)</sub>	Clock Pulse Width (Count) HIGH or LOW		6.0	8.0	-	7.0	-	5.0	7.0	-	6.0	-	ns
t <sub>w(L)</sub>	MR Pulse Width, LOW (F161)		5.0	5.0	-	5.0	-	4.0	4.0	-	4.0	-	ns
t <sub>REM</sub>	Recovery Time MR to CP (F161)		6.0	6.0	-	6.0	-	5.0	5.0	-	5.0	-	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.

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97D 02274 D

IDT54/74FCT161/A & IDT54/74FCT163/A FAST  
CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION

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