

# Am93S10 • Am93S16

## BCD Decade/Four-Bit Binary Counters

### Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading

- Edge-triggered clock action
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

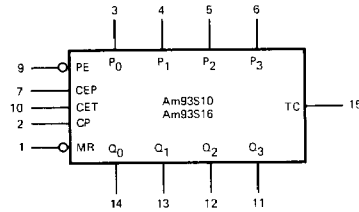
### FUNCTIONAL DESCRIPTION

The Am93S10 and Am93S16 are fully synchronous 4-bit decimal and binary counters. With the parallel enable ( $\overline{PE}$ ) LOW, data on the  $P_0$ - $P_3$  inputs is parallel loaded on the positive clock transition. When  $\overline{PE}$  is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am93S10 and 1111 for the Am93S16) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both counters have an asynchronous master reset ( $\overline{MR}$ ). A LOW on the  $\overline{MR}$  input forces the Q outputs LOW independent of all other inputs. The only requirements on the  $\overline{PE}$ , CEP, CET and  $P_0$ - $P_3$  inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

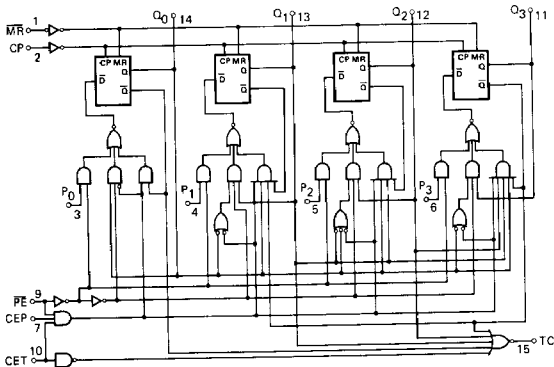
### LOGIC SYMBOL



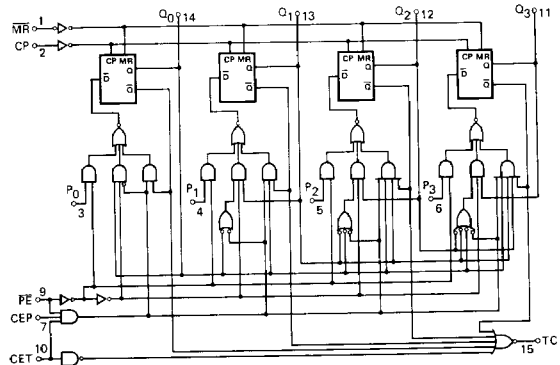
$V_{CC}$  = Pin 16  
GND = Pin 8

### LOGIC DIAGRAMS

Am93S10



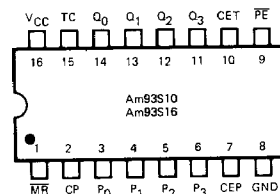
Am93S16



### ORDERING INFORMATION

Package Type	Temperature Range	Am93S10 Order Number	Am93S16 Order Number
Molded DIP	0° C to +75° C	93S10PC	93S16PC
Hermetic DIP	0° C to +75° C	93S10DC	93S16DC
Dice	0° C to +75° C	93S10XC	93S16XC
Hermetic DIP	-55° C to +125° C	93S10DM	93S16DM
Hermetic Flat Pak	-55° C to +125° C	93S10FM	93S16FM
Dice	-55° C to +125° C	93S10XM	93S16XM

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

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# Am93S10/93S16

## MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	-0.5V to +V <sub>CC</sub> max.
DC Input Voltage	-0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

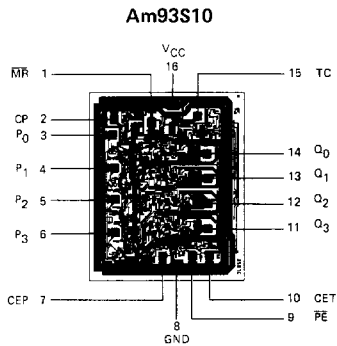
## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93S10XC, Am93S16XC	T <sub>A</sub> = 0°C to 75°C	V <sub>CC</sub> = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S10XM, Am93S16XM	T <sub>A</sub> = -55°C to +125°C	V <sub>CC</sub> = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

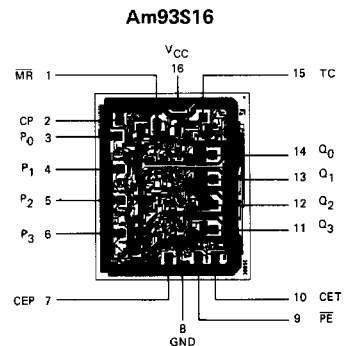
Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -1mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	XM	2.5	3.4	Volts
			XC	2.7	3.4	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 20mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		0.35	0.5	Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN., I <sub>IN</sub> = -18mA			-1.2	Volts
I <sub>IL</sub> (Note 3)	Input LOW Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 0.5V	P; MR; CEP		-2.0	mA
			CET		-3.0	
			PE		-4.0	
			CP		-5.0	
I <sub>IH</sub> (Note 3)	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 2.7V	P; MR; CEP		50	μA
			CET		75	
			PE		100	
			CP		125	
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = 5.5V			1.0	mA
I <sub>SC</sub>	Output Short Circuit Current (Note 4)	V <sub>CC</sub> = MAX.	-40	-65	-100	mA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX. (Note 5)		82	127	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.  
 3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).  
 4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 5. Outputs open; MR = 0V; all other inputs HIGH.

### Metallization and Pad Layouts



DIE SIZE 0.078" X 0.096"



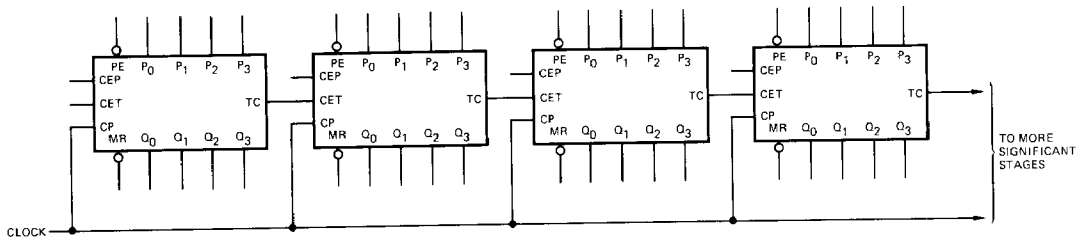
DIE SIZE 0.078" X 0.096"

SWITCHING CHARACTERISTICS ( $T_A = +25^\circ$ )

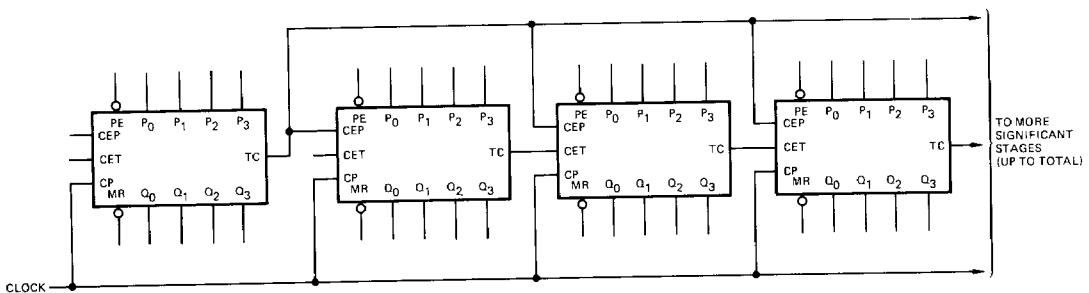
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$f_{MAX}$	Count Frequency	$V_{CC} = 5.0V, C_L = 15 \text{ pF}, R_L = 280\Omega$	70	100		MHz
$t_{PLH}$	Clock to Q			6	9	ns
$t_{PHL}$				8.5	13	
$t_{PLH}$	Clock to TC			12	18	ns
$t_{PHL}$				8	12	
$t_{PLH}$	CET to TC			6.5	10	ns
$t_{PHL}$				6.5	10	
$t_{PHL}$	$\overline{MR}$ to Q			14	20	ns
$t_s$	Recovery Time for MR (inactive)			6		ns
$t_{pw}$	Master Reset Pulse Width			13		ns
$t_{pw}$	Clock Pulse Width HIGH			6		ns
	Clock Pulse Width LOW			10		
$t_s$	Data to Clock			8		ns
$t_h$				0		
$t_s$	$\overline{PE}$ to Clock			16		ns
$t_h$			0			
$t_s$	CEP or CET to Clock		12		ns	
$t_h$			0			

## APPLICATIONS

## SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY



## FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



**DEFINITION OF FUNCTIONAL TERMS**

**PE** Parallel Enable. When  $\overline{PE}$  is LOW, the parallel inputs, P<sub>0</sub> through P<sub>3</sub>, are enabled. When  $\overline{PE}$  is HIGH, the count function is possible.

**CEP** Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

**CET** Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

**CP** Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

**MR** Master Reset. When the asynchronous master reset is LOW, the Q<sub>0</sub> through Q<sub>3</sub> outputs will be LOW regardless of the other inputs.

**P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>** The parallel data inputs for the four internal flip-flops.

**Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>** The four parallel outputs from the counter.

**TC** Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am93S10 or CET HIGH and binary 15 on the Am93S16.

**LOADING RULES (In Unit Loads)**

Input/Output	Pin No.'s	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
$\overline{MR}$	1	1	—	—
CP	2	2.5	—	—
P <sub>0</sub>	3	1	—	—
P <sub>1</sub>	4	1	—	—
P <sub>2</sub>	5	1	—	—
P <sub>3</sub>	6	1	—	—
CEP	7	1	—	—
GND	8	—	—	—
$\overline{PE}$	9	2	—	—
CET	10	1.5	—	—
Q <sub>3</sub>	11	—	20	10
Q <sub>2</sub>	12	—	20	10
Q <sub>1</sub>	13	—	20	10
Q <sub>0</sub>	14	—	20	10
TC	15	—	20	10
V <sub>CC</sub>	16	—	—	—

A Schottky TTL Unit Load is defined as 50µA measured at 2.7V HIGH and -2.0mA measured at 0.5V LOW.

**FUNCTION TABLE**

INPUTS									OUTPUTS			
CP	MR	PE	CEP	CET	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
X	L	X	X	X	X	X	X	X	L	L	L	L
†	H	L	X	X	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
†	H	H	L	L	X	X	X	X	NC	NC	NC	NC
†	H	H	L	H	X	X	X	X	NC	NC	NC	NC
†	H	H	H	L	X	X	X	X	NC	NC	NC	NC
†	H	H	H	H	X	X	X	X	COUNT			

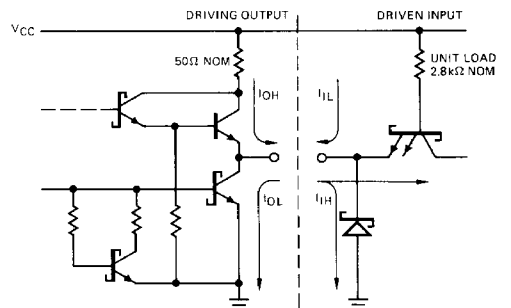
H = HIGH  
L = LOW  
X = Don't Care  
NC = No Change  
D<sub>i</sub> may be either HIGH or LOW  
† LOW-to-HIGH Transition

**TERMINAL COUNT (TC) TRUTH TABLE**

Am93S10					Am93S16					TC
CET	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	CET	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
H	H	L	L	H	H	H	H	H	H	H
L	X	X	X	X	L	X	X	X	X	L
X	L	X	X	X	X	L	X	X	X	L
X	X	H	X	X	X	X	L	X	X	L
X	X	X	H	X	X	X	X	L	X	L
X	X	X	X	L	X	X	X	X	L	L

H = HIGH  
L = LOW  
X = Don't Care

**SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS**



Note: Actual current flow direction shown.