National Semiconductor

74VHC393
Dual 4-Bit Binary Counter

General Description

The 'VHC393 is an advanced high speed CMOS 4-bit Binary Counter fabricated with silicon gate C2MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. It contains two indepedent counter circuits in one package, so that counting or frequency division of 8 binary bits can be achieved with one IC. This device changes state on the negative going transition of the $\overline{CLOCK}$ pulse. The counter can be reset to "0" (Q_0–Q_3 = "L") by a high at the CLEAR input regardless of other inputs.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

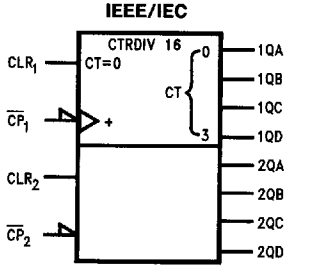
- Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC393

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC393M	M14B	14-Lead Molded JEDEC SOIC
74VHC393SJ	M14D	14-Lead Molded EIAJ SOIC
74VHC393MSC	MSC14	14-Lead Molded EIAJ Type 1 SSOP
74VHC393MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC393N	N14A	14-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code EIAJ Type 1 SSOP available on Tape and Reel only, order MSCX.

Logic Symbol



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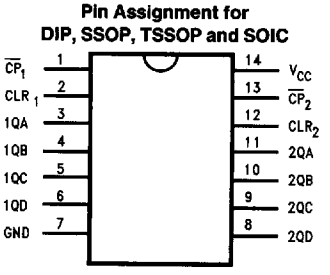
Connection Diagram



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Pin Description

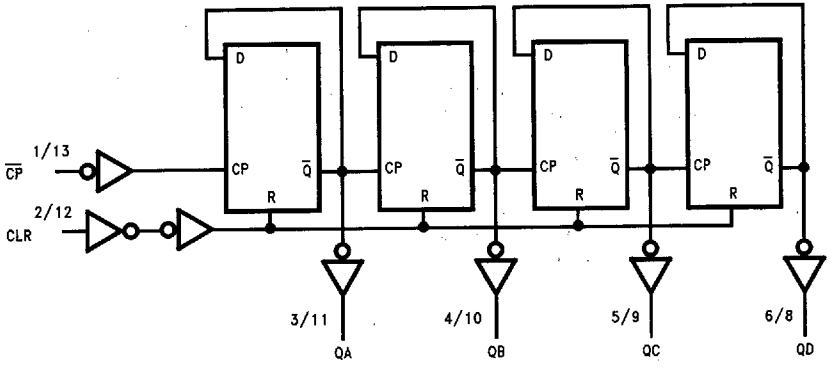
Pin Names	Description
CLR1, CLR2	Clear Inputs
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs
QA, QB, QC, QD	Outputs

Truth Table

Inputs		Outputs			
$\overline{CP}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count Up			
↑	L	No Change			

X: Don't Care

System Diagram



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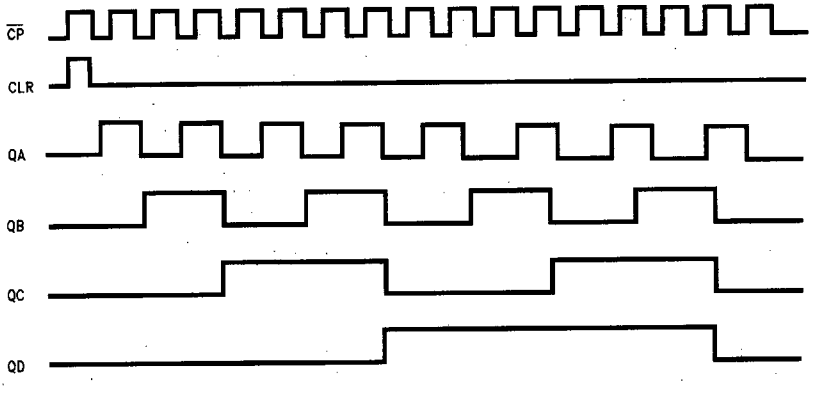
Timing Chart



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Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR}) 74 VHC	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics for 'VHC Family Devices : See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions		Fig. No.
			Min	Typ	Max	Min	Max				
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CP}$-QA)	3.3 ±0.3		8.6	13.2	1.0	15.5	ns		C_L = 15 pF	2-5, 6
				11.1	16.7	1.0	19.0			C_L = 50 pF	2-5, 6
		5.0 ±0.5		5.8	8.5	1.0	10.0	ns		C_L = 15 pF	2-5, 6
				7.3	10.5	1.0	12.0			C_L = 50 pF	2-5, 6
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CP}$-QB)	3.3 ±0.3		10.2	15.8	1.0	18.5	ns		C_L = 15 pF	2-5, 6
				12.7	19.3	1.0	22.0			C_L = 50 pF	2-5, 6
		5.0 ±0.5		6.8	9.8	1.0	11.5	ns		C_L = 15 pF	2-5, 6
				8.3	11.8	1.0	13.5			C_L = 50 pF	2-5, 6
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CP}$-QC)	3.3 ±0.3		11.7	18.0	1.0	21.0	ns		C_L = 15 pF	2-5, 6
				14.2	21.5	1.0	24.5			C_L = 50 pF	2-5, 6
		5.0 ±0.5		7.7	11.2	1.0	13.0	ns		C_L = 15 pF	2-5, 6
				9.2	13.2	1.0	15.0			C_L = 50 pF	2-5, 6
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CP}$-QD)	3.3 ±0.3		13.0	19.7	1.0	23.0	ns		C_L = 15 pF	2-5, 6
				15.5	23.2	1.0	26.5			C_L = 50 pF	2-5, 6
		5.0 ±0.5		8.5	12.5	1.0	14.5	ns		C_L = 15 pF	2-5, 6
				10.0	14.5	1.0	16.5			C_L = 50 pF	2-5, 6
t_{PLH} t_{PHL}	Propagation Delay Time (CLR-Qn)	3.3 ±0.3		7.9	12.3	1.0	14.5	ns		C_L = 15 pF	2-5, 6
				10.4	15.8	1.0	18.0			C_L = 50 pF	2-5, 6
		5.0 ±0.5		5.4	8.1	1.0	9.5	ns		C_L = 15 pF	2-5, 6
				6.9	10.1	1.0	11.5			C_L = 50 pF	2-5, 6

AC Electrical Characteristics for 'VHC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$			74VHC $T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
f_{MAX}	Maximum Clock	3.3 ±0.3	75	120		65		MHz		C_L = 15 pF
			45	65		35				C_L = 50 pF
		5.0 ±0.5	125	170		105				C_L = 15 pF
			85	115		75				C_L = 50 pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open	
C_{PD}	Power Dissipation Capacitance			23				pF	(Note 1)	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load Average operating current can be obtained by the equation:

$I_{CC(opr.)} = C_{PD} * V_{CC} * f_{IN} + I_{CC/2}$ (per Counter)

AC Operating Requirements for 'VHC Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$		74VHC $T_A = -40°C$ to $+85°C$	Units	Conditions	Fig. No.
			Typ	Guaranteed Minimum				
$t_{W(L)}$	Minimum Pulse Width ($\overline{CP}$)	3.3 ±0.3		5.0	5.0	ns		2-6
$t_{W(H)}$		5.0 ±0.5		5.0	5.0			
$t_{W(H)}$	Minimum Pulse Width (CLR)	3.3 ±0.3		5.0	5.0	ns		2-6
		5.0 ±0.5		5.0	5.0			
t_{REM}	Minimum Removal Time	3.3 ±0.3		5.0	5.0	ns		2-6, 9
		5.0 ±0.5		4.0	4.0			