

74HC4024

7-stage binary ripple counter

Rev. 9 — 28 April 2016

Product data sheet

1. General description

The 74HC4024 is a 7-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6). The counter advances on the HIGH-to-LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- CMOS input levels
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+80\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

3. Applications

- Frequency dividing circuits
- Time delay circuits.

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4024D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC4024PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Functional diagram

001aab906

001aab908

001aab907

Fig 1. Logic symbol

Fig 2. Functional diagram

Fig 3. IEC logic symbol

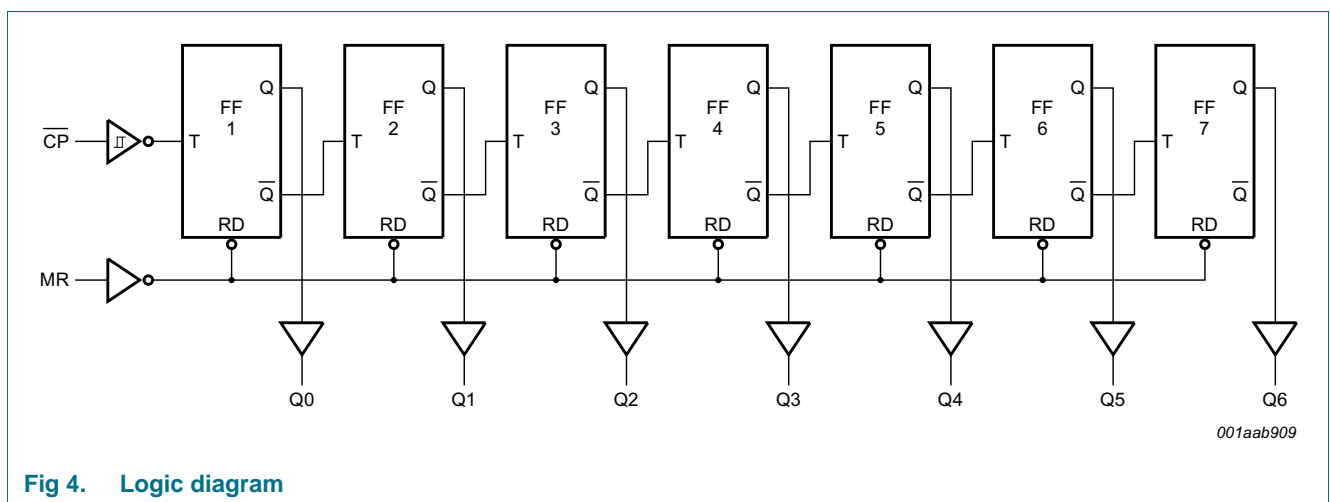


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

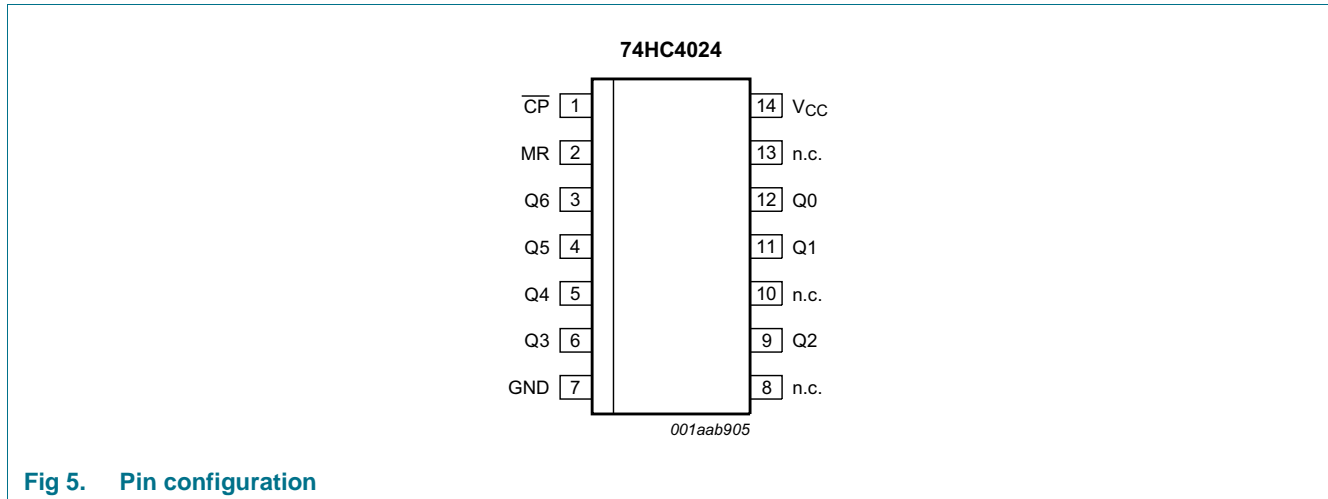


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{\text{CP}}$	1	clock input (HIGH-to-LOW, edge-triggered)
MR	2	master reset input (active HIGH)
Q6, Q5, Q4, Q3, Q2, Q1, Q0	3, 4, 5, 6, 9, 11, 12	parallel output
GND	7	ground (0 V)
n.c.	8, 10, 13	not connected
V _{CC}	14	positive supply voltage

7. Functional description

Table 3. Function table^[1]

Input		Output
MR	$\overline{\text{CP}}$	Q _n
H	X	L
L	↑	no change
	↓	count

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 ↓ = HIGH-to-LOW clock transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO14 package [1]	-	500	mW
		TSSOP14 package [2]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For TSSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V
T_{amb}	ambient temperature		-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	μA
C _I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.84	-	-	V
I _O	HIGH-level output voltage	I _O = -5.2 mA; V _{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ °C}$						
t_{pd}	propagation delay	\overline{CP} to Q0; see Figure 6 ^[1]				
		$V_{CC} = 2.0\text{ V}$	-	47	175	ns
		$V_{CC} = 4.5\text{ V}$	-	17	35	ns
		$V_{CC} = 6.0\text{ V}$	-	14	30	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	14	-	ns
		Qn to Qn+1; see Figure 6 ^[1]				
		$V_{CC} = 2.0\text{ V}$	-	25	80	ns
		$V_{CC} = 4.5\text{ V}$	-	9	16	ns
$V_{CC} = 6.0\text{ V}$	-	7	14	ns		
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	-	63	200	ns
		$V_{CC} = 4.5\text{ V}$	-	23	40	ns
		$V_{CC} = 6.0\text{ V}$	-	18	34	ns
t_t	transition time	see Figure 6 ^[2]				
		$V_{CC} = 2.0\text{ V}$	-	19	75	ns
		$V_{CC} = 4.5\text{ V}$	-	7	15	ns
		$V_{CC} = 6.0\text{ V}$	-	6	13	ns
t_w	pulse width	\overline{CP} HIGH or LOW; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	80	17	-	ns
		$V_{CC} = 4.5\text{ V}$	16	6	-	ns
		$V_{CC} = 6.0\text{ V}$	14	5	-	ns
		MR HIGH; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	80	22	-	ns
		$V_{CC} = 4.5\text{ V}$	16	8	-	ns
		$V_{CC} = 6.0\text{ V}$	14	6	-	ns
t_{rec}	recovery time	MR to \overline{CP} ; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	50	6	-	ns
		$V_{CC} = 4.5\text{ V}$	10	2	-	ns
		$V_{CC} = 6.0\text{ V}$	9	2	-	ns
f_{max}	maximum frequency	CP; see Figure 6				
		$V_{CC} = 2.0\text{ V}$	6.0	27	-	MHz
		$V_{CC} = 4.5\text{ V}$	30	82	-	MHz
		$V_{CC} = 6.0\text{ V}$	35	98	-	MHz
		$V_{CC} = 5.0\text{ V}$; $C_L = 15\text{ pF}$	-	90	-	MHz
C_{PD}	power dissipation capacitance	$V_1 = GND$ to V_{CC} ^[3]	-	25	-	pF

Table 7. Dynamic characteristics ...continued
 $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}$						
t_{pd}	propagation delay	$\overline{\text{CP}}$ to Q0; see Figure 6 ^[1]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	220	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	44	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	37	ns
		Qn to Qn+1; see Figure 6 ^[1]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	100	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	20	ns
$V_{\text{CC}} = 6.0\text{ V}$	-	-	17	ns		
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	250	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	50	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	43	ns
t_t	transition time	see Figure 6 ^[2]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	95	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	19	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	16	ns
t_w	pulse width	$\overline{\text{CP}}$ HIGH or LOW; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	100	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	20	-	-	ns
		$V_{\text{CC}} = 6.0\text{ V}$	17	-	-	ns
		MR HIGH; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	100	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	20	-	-	ns
$V_{\text{CC}} = 6.0\text{ V}$	17	-	-	ns		
t_{rec}	recovery time	MR to $\overline{\text{CP}}$; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	65	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	13	-	-	ns
		$V_{\text{CC}} = 6.0\text{ V}$	11	-	-	ns
f_{max}	maximum frequency	CP; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	4.8	-	-	MHz
		$V_{\text{CC}} = 4.5\text{ V}$	24	-	-	MHz
		$V_{\text{CC}} = 6.0\text{ V}$	28	-	-	MHz

Table 7. Dynamic characteristics ...continued
 $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 7](#).

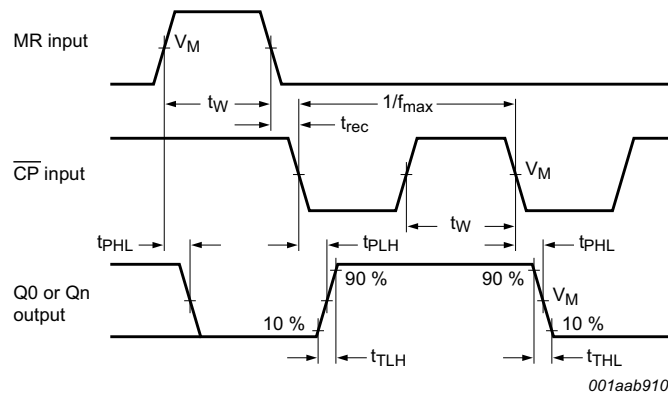
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}$						
t_{pd}	propagation delay	$\overline{\text{CP}}$ to Q0; see Figure 6 ^[1]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	265	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	53	ns
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	45	ns
		Qn to Qn+1; see Figure 6 ^[1]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	120	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	24	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Q0; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	300	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	60	ns
t_t	transition time	see Figure 6 ^[2]				
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	110	ns
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	22	ns
t_w	pulse width	$\overline{\text{CP}}$ HIGH or LOW; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	120	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	24	-	-	ns
		$V_{\text{CC}} = 6.0\text{ V}$	20	-	-	ns
		MR HIGH; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	120	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	24	-	-	ns
t_{rec}	recovery time	MR to $\overline{\text{CP}}$; see Figure 6				
		$V_{\text{CC}} = 2.0\text{ V}$	75	-	-	ns
		$V_{\text{CC}} = 4.5\text{ V}$	15	-	-	ns
		$V_{\text{CC}} = 6.0\text{ V}$	13	-	-	ns

Table 7. Dynamic characteristics ...continued
GND = 0 V; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency	CP; see Figure 6				
		$V_{\text{CC}} = 2.0 \text{ V}$	4.0	-	-	MHz
		$V_{\text{CC}} = 4.5 \text{ V}$	20	-	-	MHz
		$V_{\text{CC}} = 6.0 \text{ V}$	24	-	-	MHz

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW).
 $P_{\text{D}} = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \sum(C_L \times V_{\text{CC}}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs.

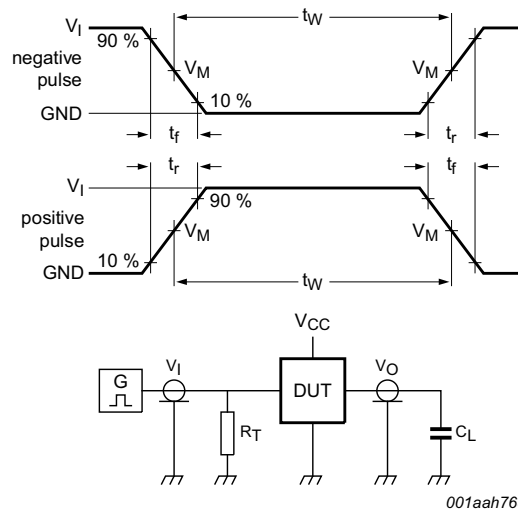
12. Waveforms



Also showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) recovery time.

$$V_M = 0.5 \times V_I$$

Fig 6. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Test data is given in [Table 8](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 8. Test data

Supply	Input	Load
V_{CC}	V_I	C_L
2.0 V	V_{CC}	50 pF
4.5 V	V_{CC}	50 pF
6.0 V	V_{CC}	50 pF
5.0 V	V_{CC}	15 pF

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

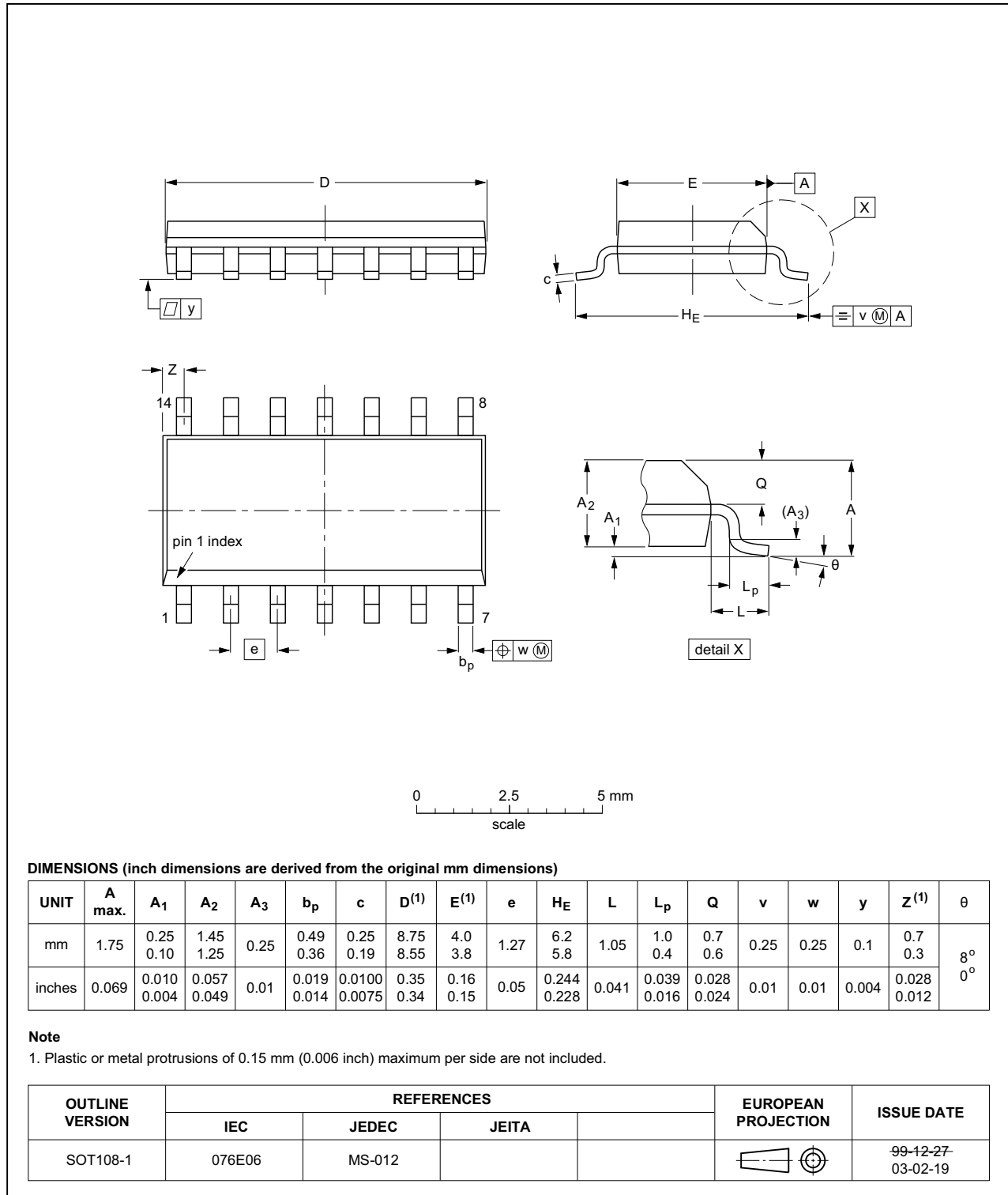


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

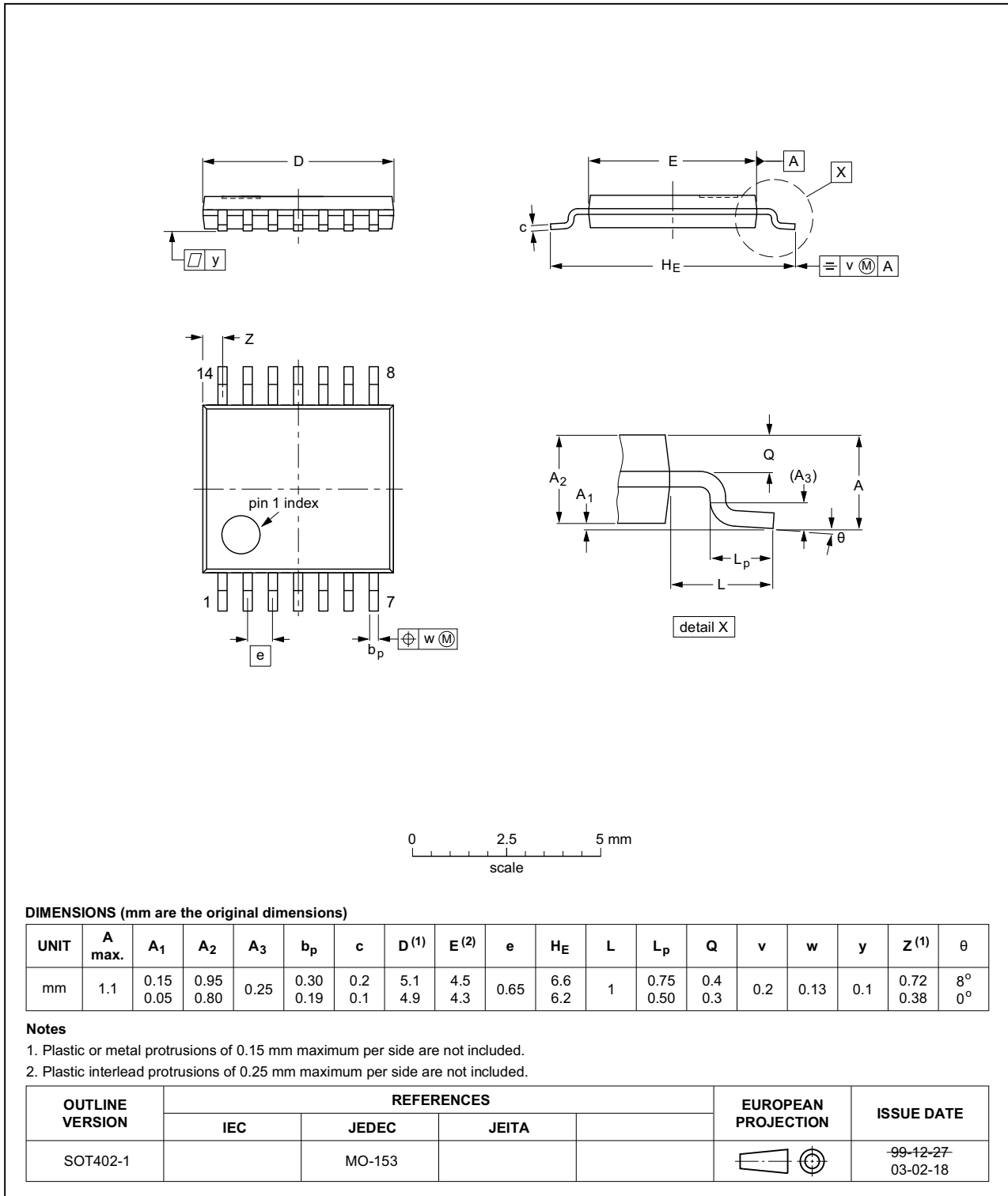


Fig 9. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4024 v.9	20160428	Product data sheet	-	74HC4024 v.8
Modifications:	<ul style="list-style-type: none"> Type number 74HC4024DB (SOT337-1) removed. 			
74HC4024 v.8	20151202	Product data sheet	-	74HC4024 v.7
Modifications:	<ul style="list-style-type: none"> Type number 74HC4024N (SOT27-1) removed. 			
74HC4024 v.7	20131031	Product data sheet	-	74HC4024 v.6
Modifications:	<ul style="list-style-type: none"> General description updated. 			
74HC4024 v.6	20120823	Product data sheet	-	74HC4024 v.5
74HC4024 v.4	20100929	Product data sheet	-	74HC4024 v.3
74HC4024 v.3	20041112	Product data sheet	-	74HC_HCT4024_CNV v.2
74HC_HCT4024_CNV v.2	19970901	Product specification	-	74HC_HCT4024 v.1
74HC_HCT4024 v.1	19901201	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

16.2 Definitions

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18. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	3
8	Limiting values	4
9	Recommended operating conditions	4
10	Static characteristics	5
11	Dynamic characteristics	7
12	Waveforms	10
13	Package outline	12
14	Abbreviations	14
15	Revision history	14
16	Legal information	15
16.1	Data sheet status	15
16.2	Definitions	15
16.3	Disclaimers	15
16.4	Trademarks	16
17	Contact information	16
18	Contents	17