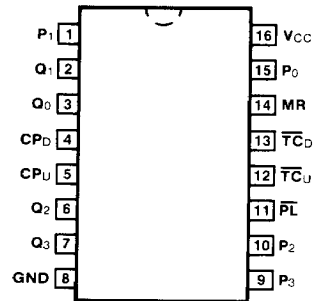## 54/74193 010492
54LS/74LS193 010494

UP/DOWN BINARY COUNTER
(With Separate Up/down Clocks)

DESCRIPTION — The '193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description and detail specifications please refer to the '192 data sheet.
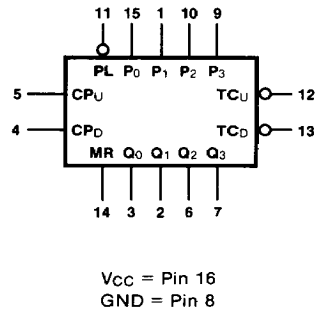
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE Vcc = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE Vcc = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74193PC, 74LS193PC		9B
Ceramic DIP (D)	A	74193DC, 74LS193DC	54193DM, 54LS193DM	6B
Flatpak (F)	A	74193FC, 74LS193FC	54193FM, 54LS193FM	4L

CONNECTION DIAGRAM
PINOUT A

P_1	1	16	V_{CC}
Q_1	2	15	P_0
Q_0	3	14	MR
CP_D	4	13	$\overline{TC}_D$
CP_U	5	12	$\overline{TC}_U$
Q_2	6	11	$\overline{PL}$
Q_3	7	10	P_2
GND	8	9	P_3

LOGIC SYMBOL

```
        11  15  1  10  9
        PL  P0  P1 P2  P3
    5 — CPU          TCU o— 12
    4 — CPD          TCD o— 13
        MR  Q0  Q1 Q2  Q3
        14   3   2  6   7
```

V_{CC} = Pin 16
GND = Pin 8

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INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/1.0	0.5/0.25
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	20/10	10/5.0 (2.5)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	20/10	10/5.0 (2.5)

MODE SELECT TABLE

MR	$\overline{PL}$	CP$_U$	CP$_D$	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐⌐	H	Count Up
L	H	H	⌐⌐	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

STATE DIAGRAM

—▶ COUNT UP
---▶ COUNT DOWN
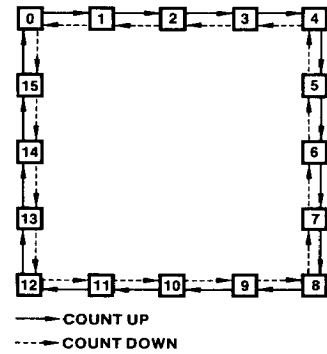
LOGIC EQUATIONS
FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

LOGIC DIAGRAM

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