

HEF4520B-Q100

Dual binary counter

Rev. 2 — 1 March 2022

Product data sheet

1. General description

The HEF4520B-Q100 is a dual 4-bit internally synchronous binary counter with two clock inputs (nCP0 and nCP1), buffered outputs from all four bit positions (nQ0 to nQ3) and an asynchronous master reset input (nMR). The counter advances on either the LOW-to-HIGH transition of nCP0 if nCP1 is HIGH or the HIGH-to-LOW transition of nCP1 if nCP0 is LOW. Either nCP0 or nCP1 may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ0 to nQ3 = LOW) independent of nCP0 and nCP1. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Standardized symmetrical output characteristics
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4520BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

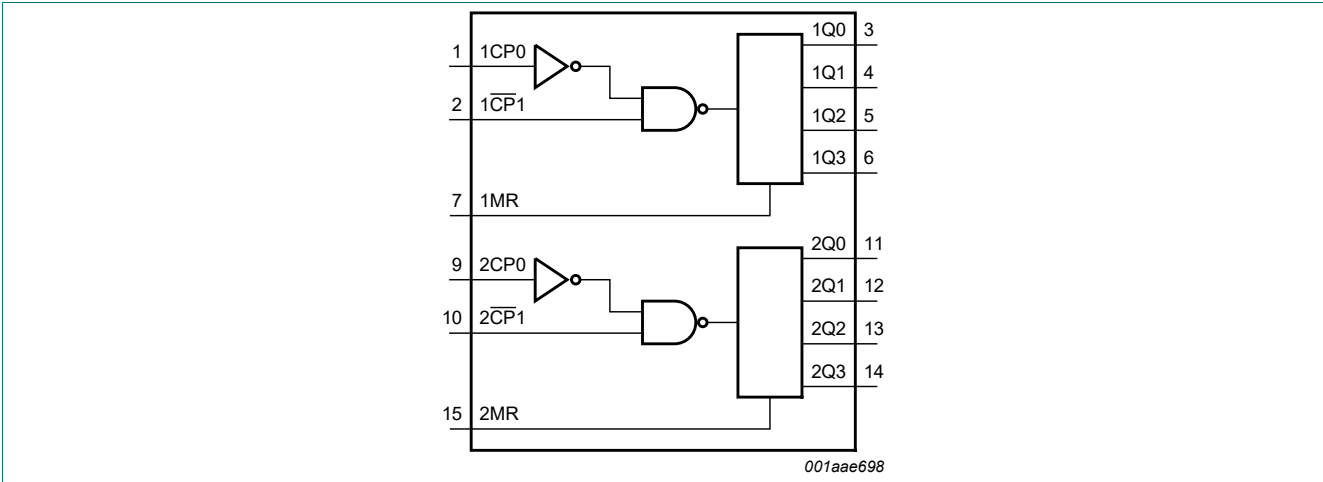


Fig. 1. Functional diagram

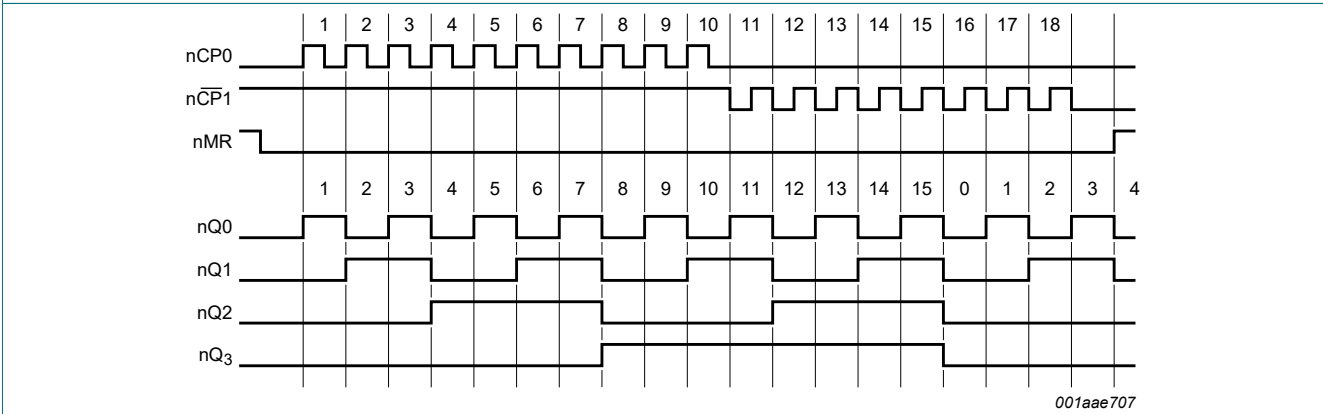


Fig. 2. Timing diagram

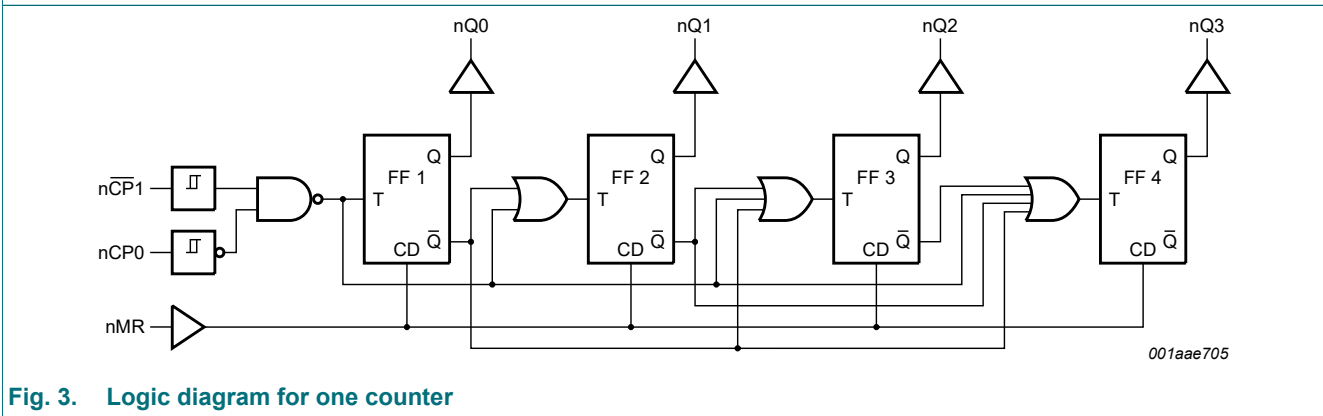


Fig. 3. Logic diagram for one counter

5. Pinning information

5.1. Pinning

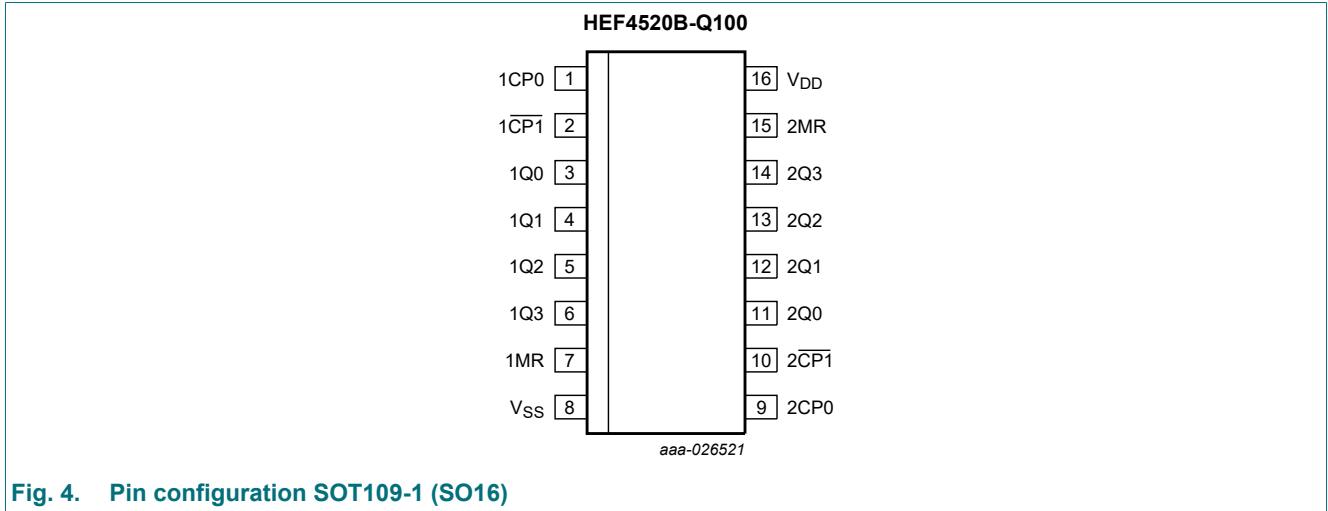


Fig. 4. Pin configuration SOT109-1 (SO16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP0, 2CP0	1, 9	clock input (LOW-to-HIGH triggered)
1CP1, 2CP1	2, 10	clock input (HIGH-to-LOW triggered)
1Q0, 1Q1, 1Q2, 1Q3	3, 4, 5, 6	output
1MR, 2MR	7, 15	master reset input
V _{SS}	8	ground supply voltage
2Q0, 2Q1, 2Q2, 2Q3	11, 12, 13, 14	output
V _{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

nCP0	nCP1	nMR	Mode
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	nQ0 to nQ3 = LOW

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0$ V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature	per output	-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	SO16 package	-	500	mW
P	power dissipation		-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10$ V	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15$ V	-	-	0.08	$\mu\text{s/V}$

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40$ °C		$T_{amb} = 25$ °C		$T_{amb} = 85$ °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1$ μA ; $V_I = V_{SS}$ or V_{DD}	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1$ μA ; $V_I = V_{SS}$ or V_{DD}	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current	V _{DD} = 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	µA
I _{DD}	supply current	I _O = 0 A; V _I = V _{SS} or V _{DD}	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nCP0, nCP1 to nQn; see Fig. 5	5 V	83 ns + (0.55 ns/pF)C _L	-	110	220	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
		nMR to nQn; see Fig. 5	5 V	48 ns + (0.55 ns/pF)C _L	-	75	150	ns
			10 V	24 ns + (0.23 ns/pF)C _L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
t _{PLH}	LOW to HIGH propagation delay	nCP0, nCP1 to nQn; see Fig. 5	5 V	83 ns + (0.55 ns/pF)C _L	-	110	220	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _t	transition time	nQn; see Fig. 5	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _w	pulse width	nCP0 input LOW; minimum width; see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nCP1 input HIGH; minimum width; see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR input HIGH; minimum width; see Fig. 5	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t _{su}	set-up time	nCP0 to nCP1; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nCP1 to nCP0; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t _{rec}	recovery time	see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
f _{max}	maximum frequency	nCP0, nCP1; see Fig. 5	5 V		8	16	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

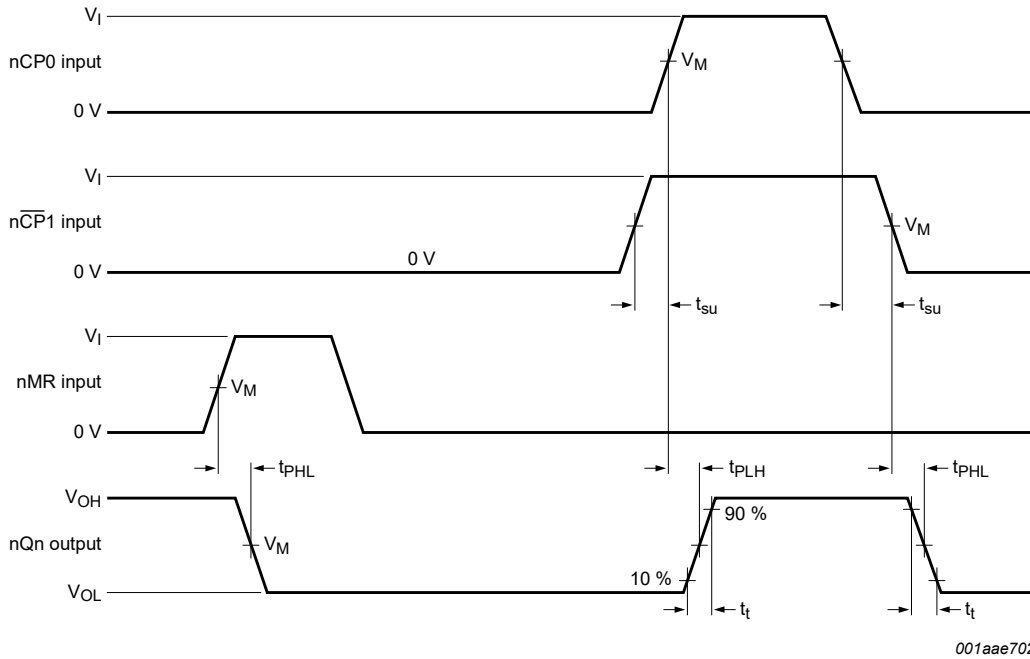
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

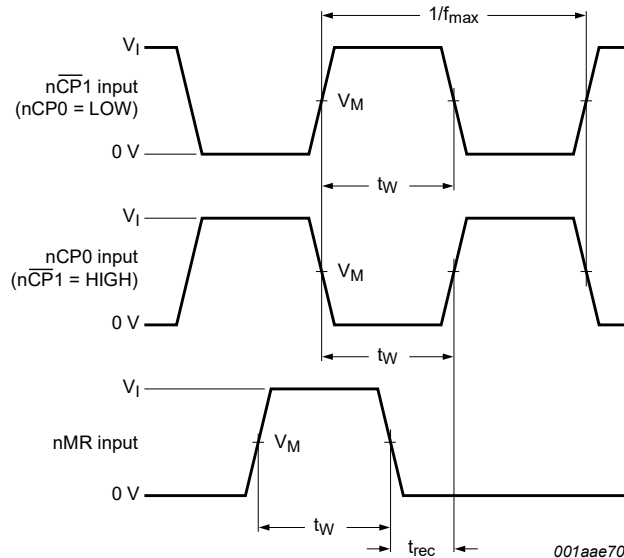
Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	Where:
P _D	dynamic power dissipation	5 V	$P_D = 850 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f _i = input frequency in MHz, f _o = output frequency in MHz, C _L = output load capacitance in pF, V _{DD} = supply voltage in V, Σ(f _o × C _L) = sum of the outputs.
		10 V	$P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 10200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

10.1. Waveforms and test circuit



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a. nCP0 and nCP1 set-up times, propagation delays and output transition times



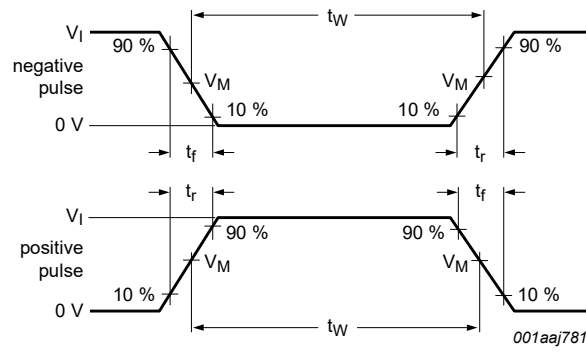
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b. nMR recovery time, minimum nCP0, nCP1, and nMR pulse widths and maximum frequency

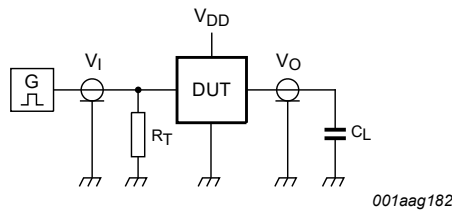
Measurement points are given in [Table 9](#).

The logic levels V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Fig. 5. Waveforms showing measurements for switching times



a. Input waveforms



b. Test circuit

Test data is given in [Table 9](#).

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
V_{DD}	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5 \times V_I$	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

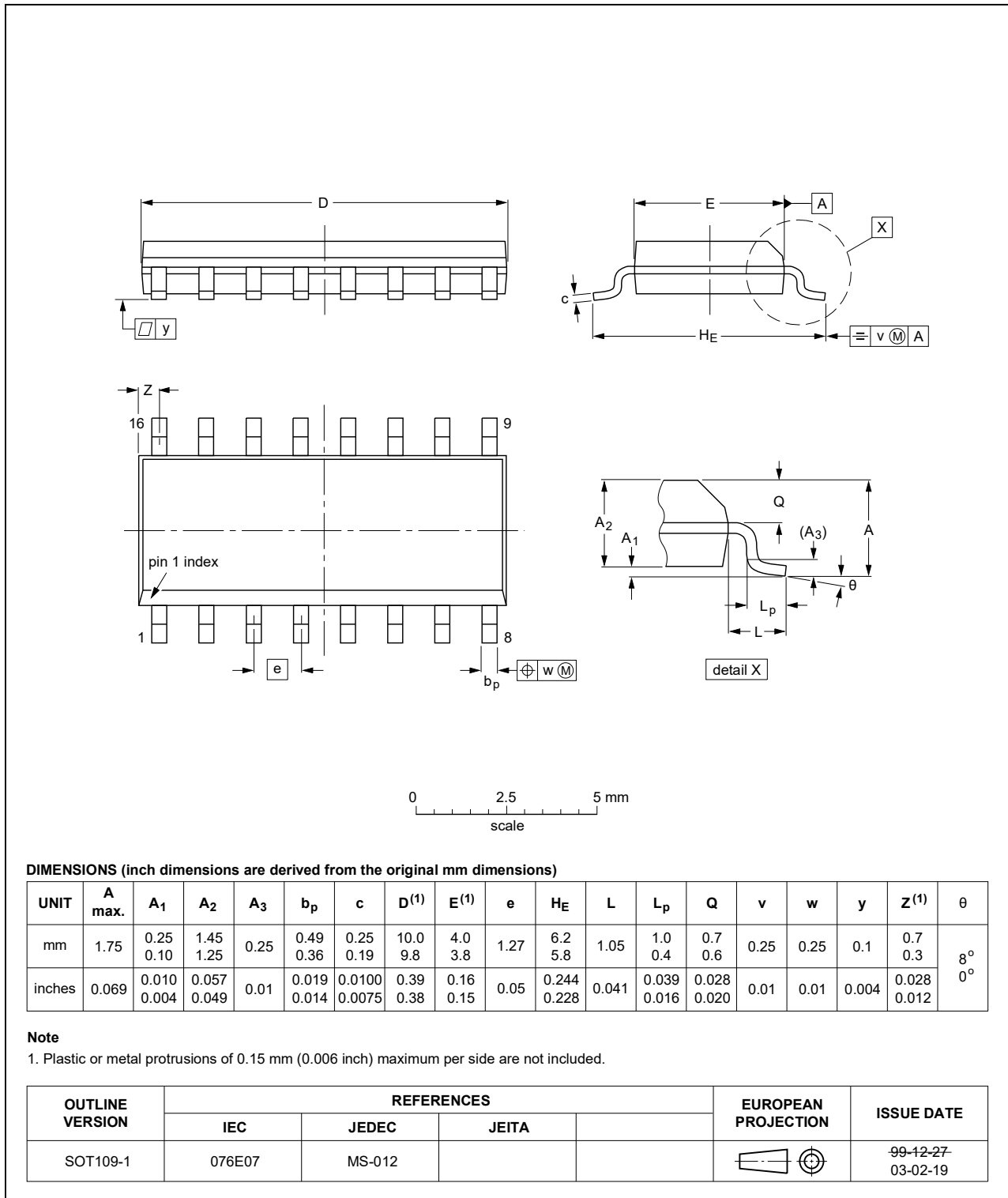


Fig. 7. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4093B_Q100 v.2	20220301	Product specification	-	HEF4093B_Q100 v.1
Modifications	<ul style="list-style-type: none"> Section 1, Section 2, and Section 12 updated. 			
HEF4093B_Q100 v.1	20120712	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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