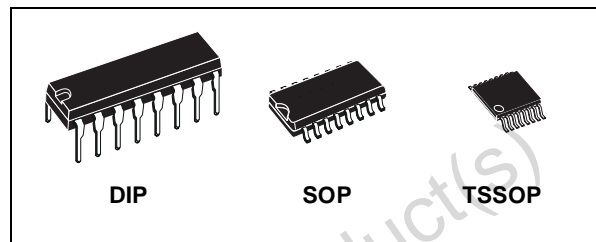




# M74HC4518

## DUAL DECADE COUNTER

- HIGH SPEED :  
 $f_{MAX} = 60 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN.)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 4518



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC4518B1R	
SOP	M74HC4518M1R	M74HC4518RM13TR
TSSOP		M74HC4518TTR

### DESCRIPTION

The M74HC4518 is an high speed CMOS DUAL BINARY COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It consist of two identical internally synchronous 4-stage counters. The counter stages are D-TYPE flip-flops having interchangeable CLOCK and ENABLE inputs for incrementing on either the positive-going or negative-going transition.

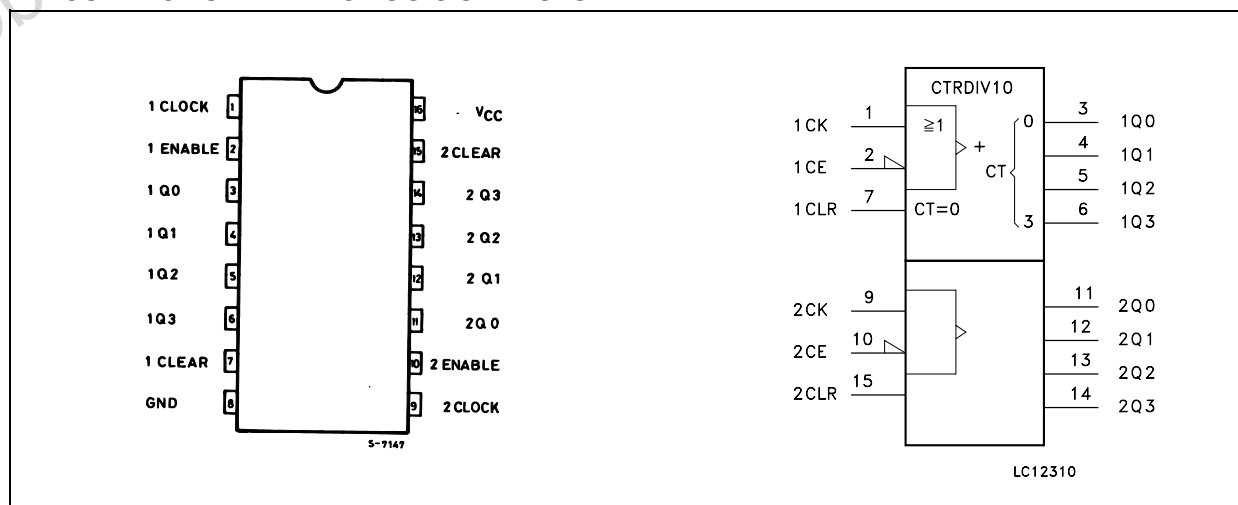
For single-unit operation the ENABLE input is maintained "high" and the counter advances on

each positive-going transition of the CLOCK. The counters are cleared by high levels on their clear lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held permanently low.

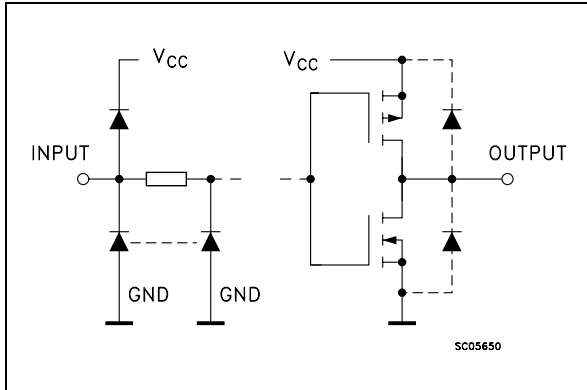
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# M74HC4518

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

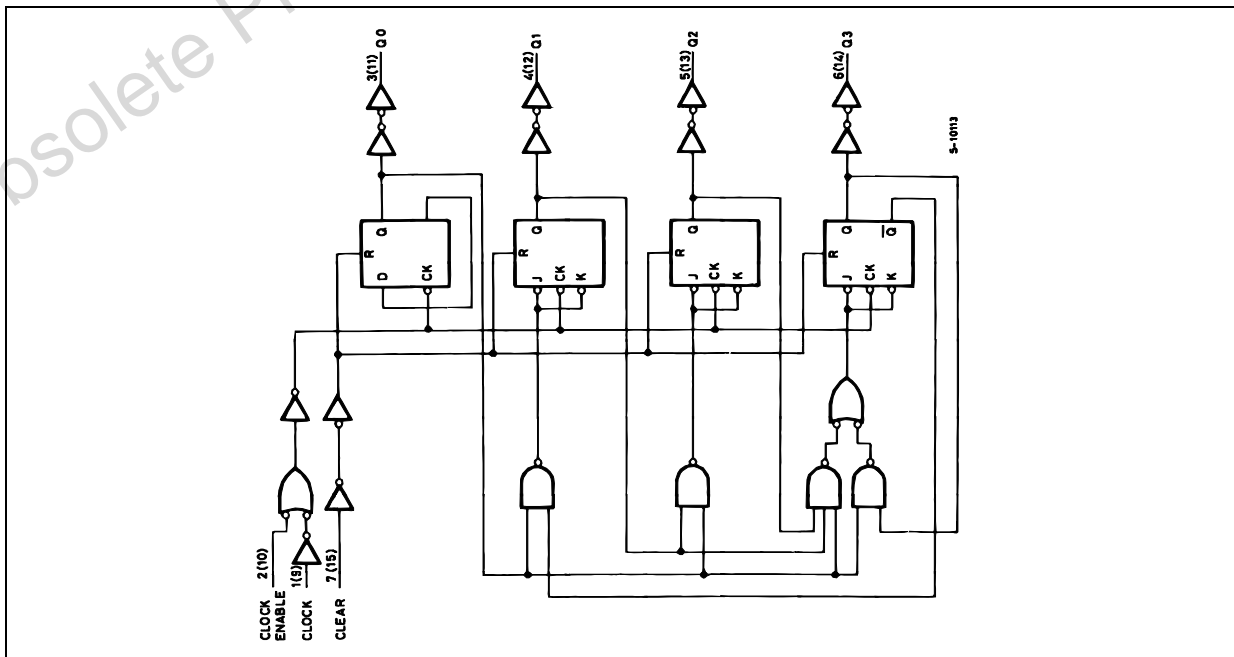
PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1CLOCK, 2CLOCK	Clock Inputs (LOW to HIGH, Edge-Triggered)
2, 10	1ENABLE, 2ENABLE	Clock Enable Inputs
3, 4, 5, 6	1Q0 to 1Q3	Data Outputs
7, 15	1CLEAR, 2CLEAR	Asynchronous Reset Inputs (Active LOW)
11, 12, 13, 14	2Q0 to 2Q3	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

## TRUTH TABLE

INPUTS			FUNCTION
CLOCK	ENABLE	CLEAR	
	H	L	INCREMENT COUNTER
L		L	INCREMENT COUNTER
	X	L	NO CHANGE
X		L	NO CHANGE
	L	L	NO CHANGE
H		L	NO CHANGE
X	X	H	Q0 THRU Q3=L

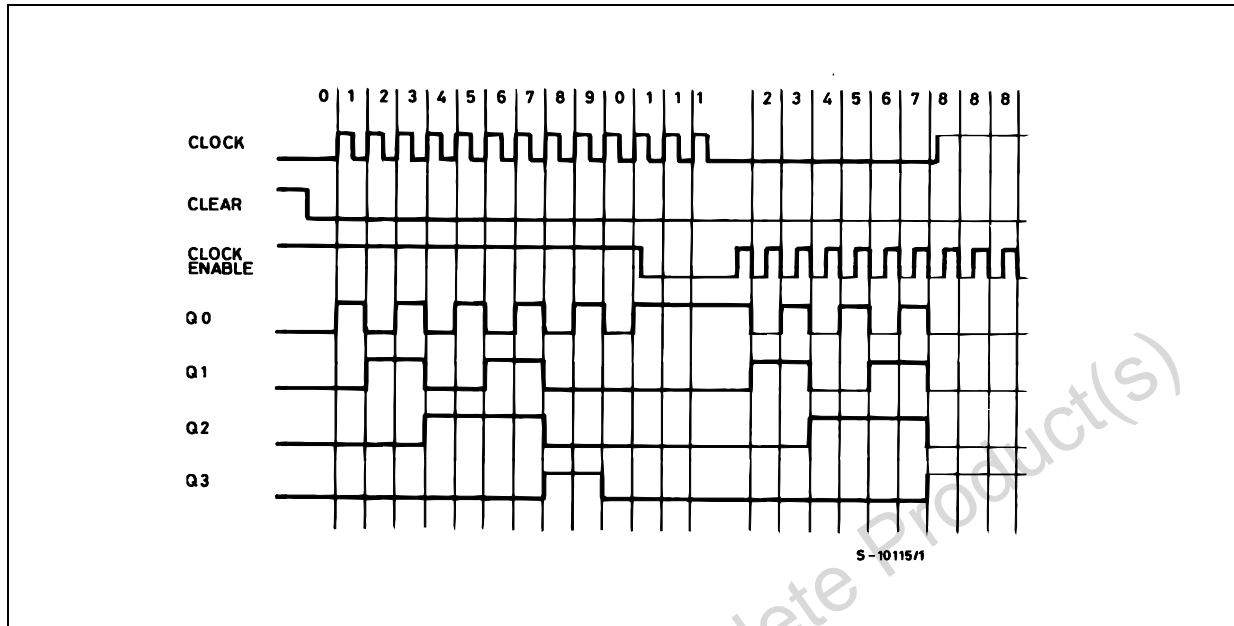
X : Don't Care  
Z : High Impedance

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

## TIMING CHART



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(\*) 500mW at 65  $^{\circ}C$ ; derate to 300mW by 10mW/ $^{\circ}C$  from 65 $^{\circ}C$  to 85 $^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	2.0									V
		4.5									
		6.0									
$V_{IL}$	Low Level Input Voltage	2.0									V
		4.5									
		6.0									
$V_{OH}$	High Level Output Voltage	2.0	$I_O = -20 \mu\text{A}$	1.9	2.0		1.9		1.9		V
		4.5	$I_O = -20 \mu\text{A}$	4.4	4.5		4.4		4.4		
		6.0	$I_O = -20 \mu\text{A}$	5.9	6.0		5.9		5.9		
		4.5	$I_O = -4.0 \text{ mA}$	4.18	4.31		4.13		4.10		
		6.0	$I_O = -5.2 \text{ mA}$	5.68	5.8		5.63		5.60		
$V_{OL}$	Low Level Output Voltage	2.0	$I_O = 20 \mu\text{A}$		0.0	0.1		0.1		0.1	V
		4.5	$I_O = 20 \mu\text{A}$		0.0	0.1		0.1		0.1	
		6.0	$I_O = 20 \mu\text{A}$		0.0	0.1		0.1		0.1	
		4.5	$I_O = 4.0 \text{ mA}$		0.17	0.26		0.37		0.40	
		6.0	$I_O = 5.2 \text{ mA}$		0.18	0.26		0.37		0.40	
$I_I$	Input Leakage Current	6.0	$V_I = V_{CC} \text{ or GND}$			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	6.0	$V_I = V_{CC} \text{ or GND}$			4		40		80	$\mu\text{A}$

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

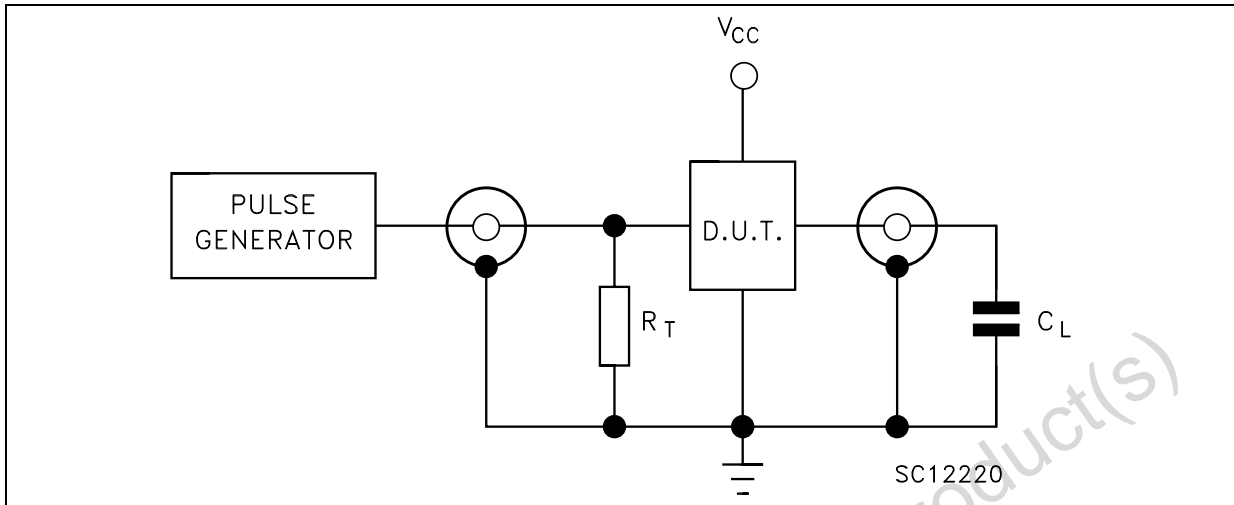
Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH}$ $t_{THL}$	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (CK, ENABLE - Qn)	2.0			72	160		200		240	ns
		4.5			22	32		40		48	
		6.0			18	27		34		41	
$t_{PHL}$	Propagation Delay Time (CLR - Qn)	2.0			65	150		190		225	ns
		4.5			20	30		38		45	
		6.0			16	26		33		38	
$f_{MAX}$	Maximum Clock Frequency	2.0		6	23		4.8		4		MHz
		4.5		30	51		24		20		
		6.0		35	60		28		24		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK, ENABLE)	2.0			25	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_{REM}$	Minimum Removal Time (CLEAR)	2.0			21	50		60		75	ns
		4.5			3	10		12		15	
		6.0			3	9		11		13	

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$C_{IN}$	Input Capacitance				5	10		10		10	pF
$C_{PD}$	Power Dissipation Capacitance (note 1)				38						pF

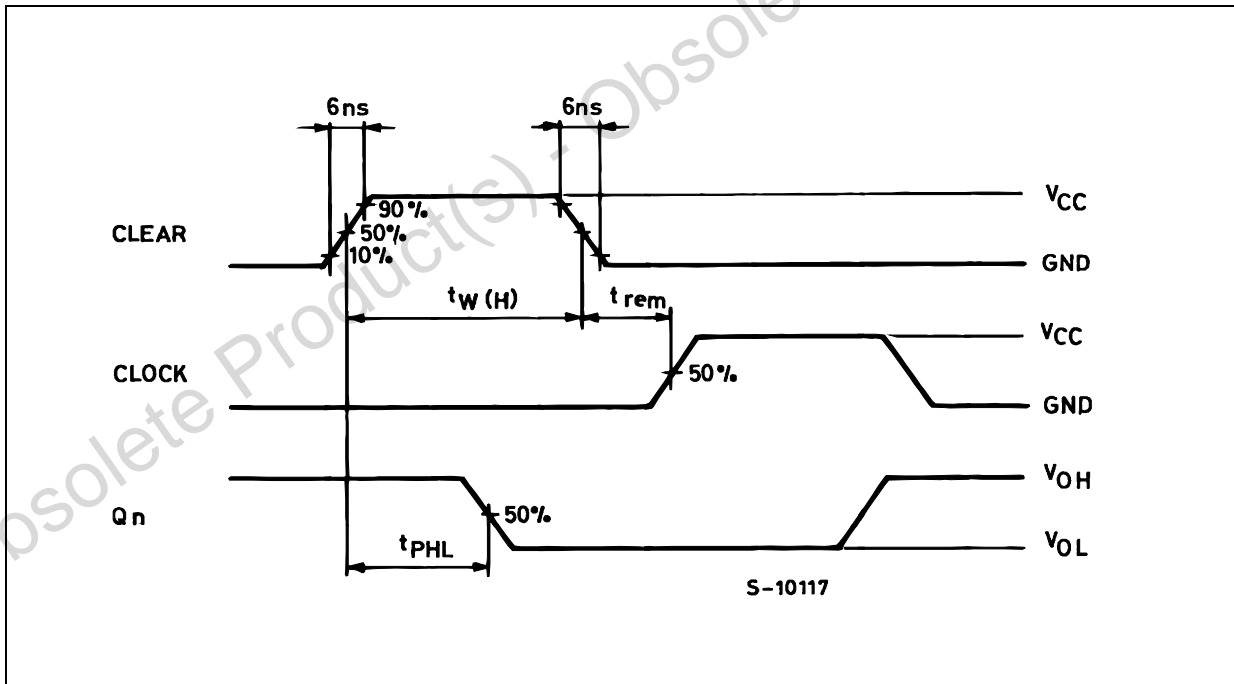
1)  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$  (per Counter)

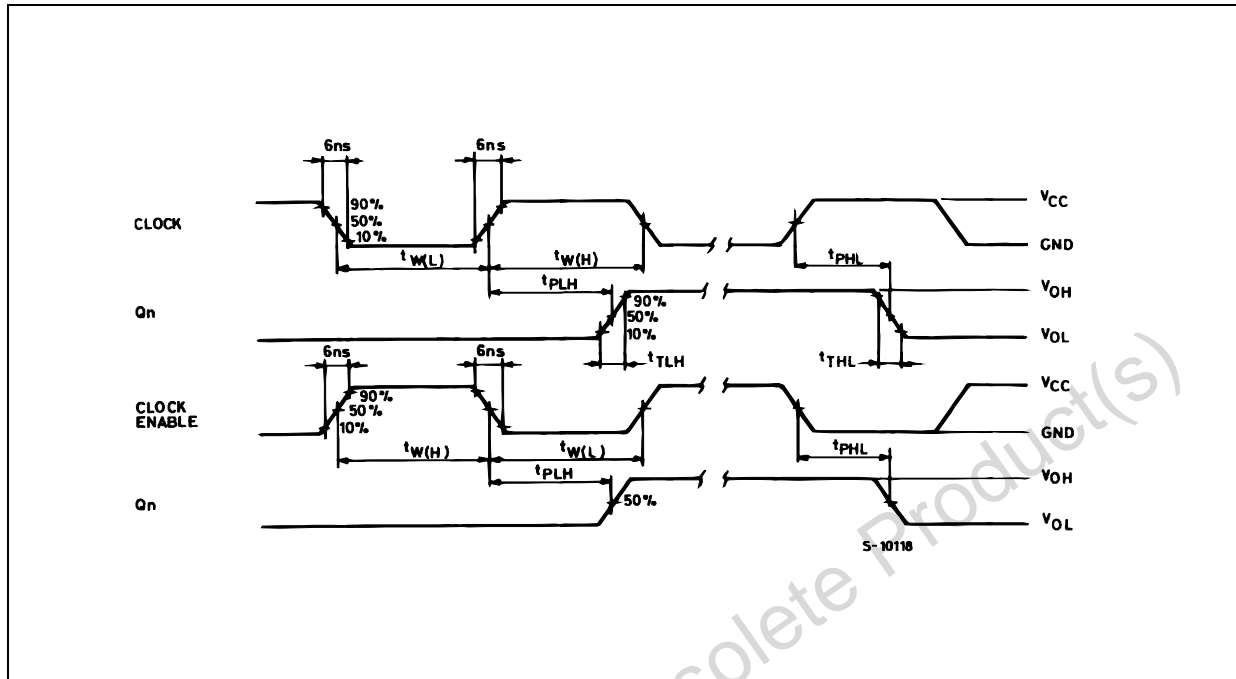
TEST CIRCUIT



$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

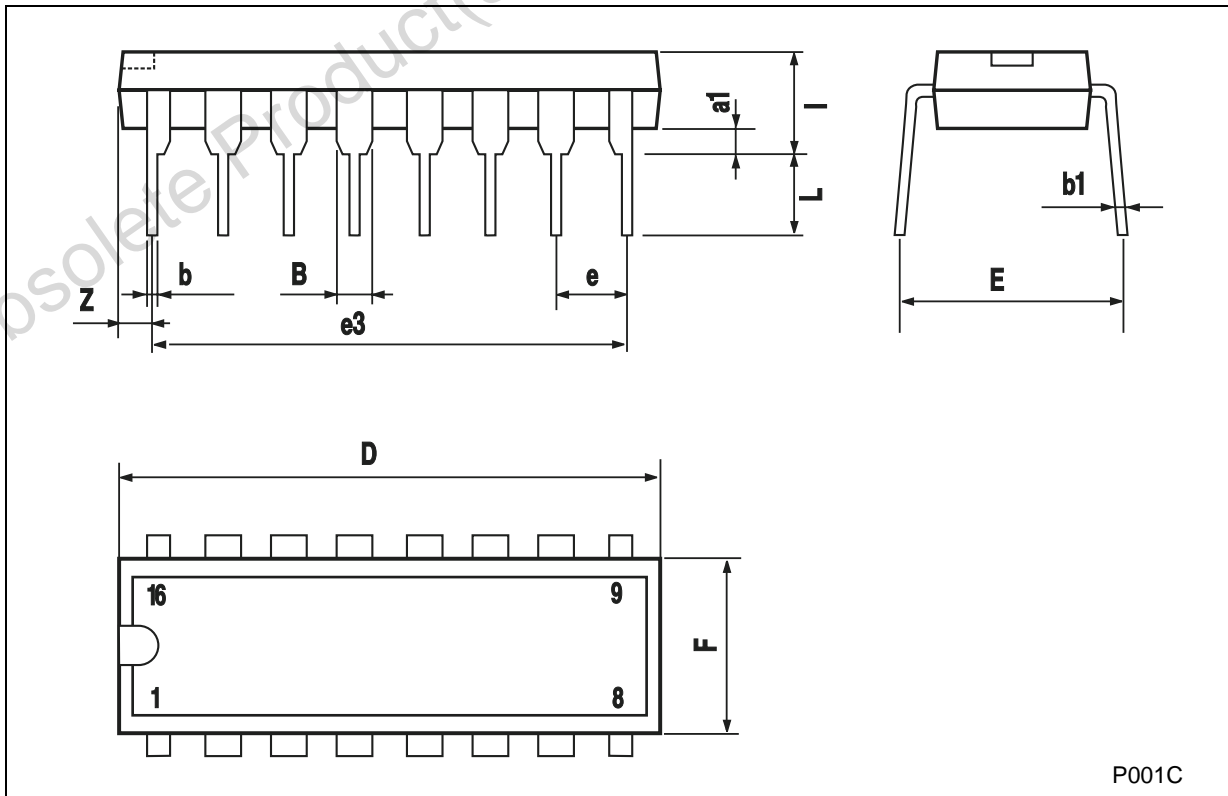
WAVEFORM 1: MINIMUM PULSE WIDTH AND REMOVAL TIME ( $f=1\text{MHz}$ ; 50% duty cycle)



WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH( $f=1\text{MHz}$ ; 50% duty cycle)

**Plastic DIP-16 (0.25) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

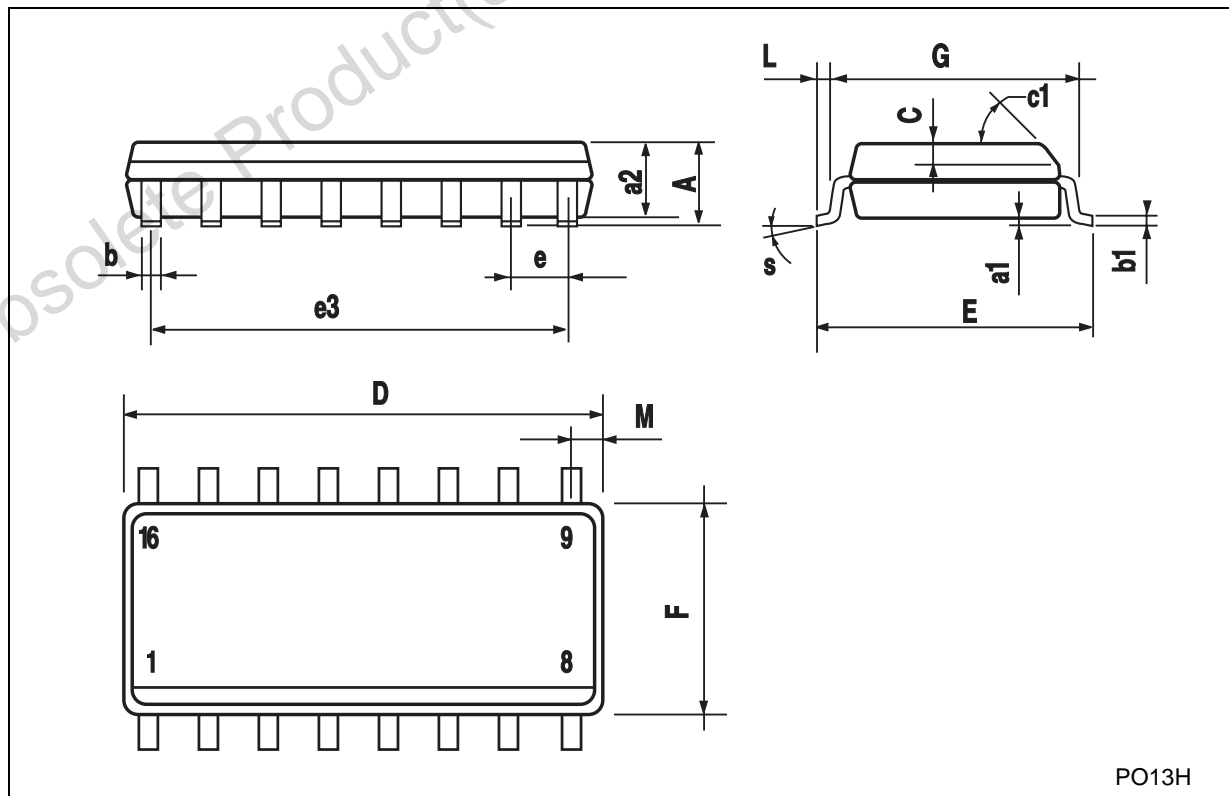


P001C



## SO-16 MECHANICAL DATA

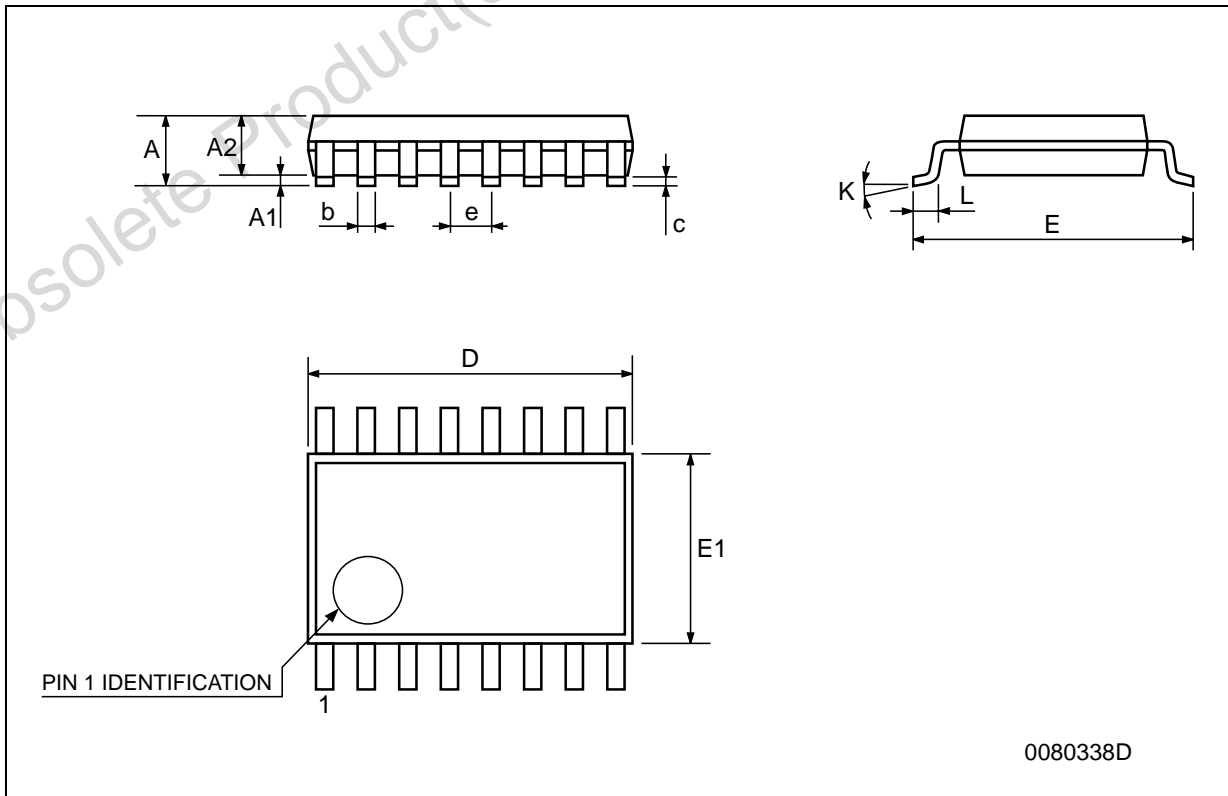
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

**TSSOP16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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