

MC74HC390A

Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections

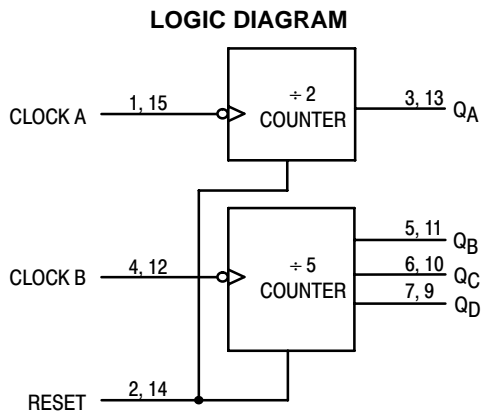
High-Performance Silicon-Gate CMOS

The MC74HC390A is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of $\div 2$ and/or $\div 5$ up to a $\div 100$ counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390A.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates



PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

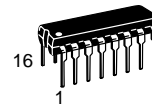
Clock		Reset	Action
A	B		
X	X	H	Reset $\div 2$ and $\div 5$
$\bar{\square}$	X	L	Increment $\div 2$
X	$\bar{\square}$	L	Increment $\div 5$



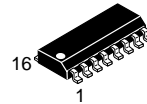
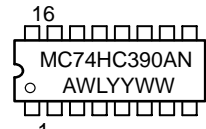
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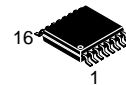
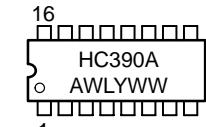
MARKING DIAGRAMS



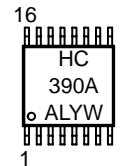
PDIP-16
N SUFFIX
CASE 648



SO-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT

CLOCK A _a	1	16	V_{CC}
RESET a	2	15	CLOCK A _b
Q _{Aa}	3	14	RESET b
CLOCK B _a	4	13	Q _{Ab}
Q _{Ba}	5	12	CLOCK B _b
Q _{Ca}	6	11	Q _{Bb}
Q _{Da}	7	10	Q _{Cb}
GND	8	9	Q _{Db}

ORDERING INFORMATION

Device	Package	Shipping
MC74HC390AN	PDIP-16	2000 / Box
MC74HC390AD	SOIC-16	48 / Rail
MC74HC390ADR2	SOIC-16	2500 / Reel
MC74HC390ADT	TSSOP-16	96 / Rail
MC74HC390ADTR2	TSSOP-16	2500 / Reel

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
PD	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/ C from 65 to 125 C

SOIC Package: - 7 mW/ C from 65 to 125 C

TSSOP Package: - 6.1 mW/ C from 65 to 125 C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	V _{CC} = 2.0 V	0	1000	
	V _{CC} = 3.0 V	0	600	
	V _{CC} = 4.5 V	0	500	
	V _{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25 C	≤ 85 C	≤ 125 C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25 C	≤ 85 C	≤ 125 C	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_f = t_r = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25 C	≤ 85 C	≤ 125 C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	10	9	8	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	24	30	36	
		6.0	20	26	31	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0	200	250	300	ns
		3.0	160	185	210	
		4.5	58	65	70	
		6.0	49	62	68	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	26	33	39	
		6.0	22	28	33	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0	90	105	180	ns
		3.0	56	70	100	
		4.5	37	46	56	
		6.0	31	39	48	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	26	33	39	
		6.0	22	28	33	
t _{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	80	95	110	ns
		3.0	48	65	75	
		4.5	30	38	44	
		6.0	26	33	39	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

- For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Counter)*	Typical @ 25°C, V _{CC} = 5.0 V	
		35	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25 C	≤ 85 C	≤ 125 C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 2)	2.0	25	30	40	ns
		3.0	15	20	30	
		4.5	10	13	15	
		6.0	9	11	13	
t_w	Minimum Pulse Width, Clock A, Clock B (Figure 1)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	20	24	30	
		6.0	18	22	28	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock A (Pins 1, 15) and Clock B (Pins 4, 15)

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

CONTROL INPUTS

Reset (Pins 2, 14)

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces Q_A through Q_D low.

OUTPUTS

Q_A (Pins 3, 13)

Output of the ÷ 2 counter.

Q_B, Q_C, Q_D (Pins 5, 6, 7, 9, 10, 11)

Outputs of the ÷ 5 counter. Q_D is the most significant bit. Q_A is the least significant bit when the counter is connected for BCD output as in Figure 4. Q_B is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 5.

SWITCHING WAVEFORMS

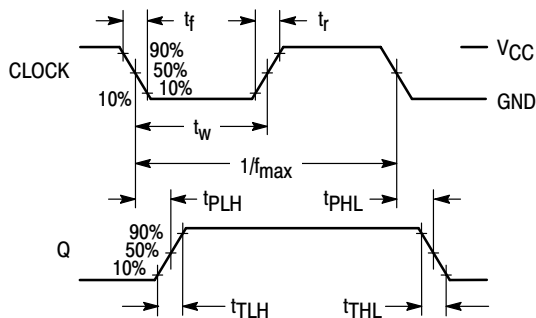


Figure 1.

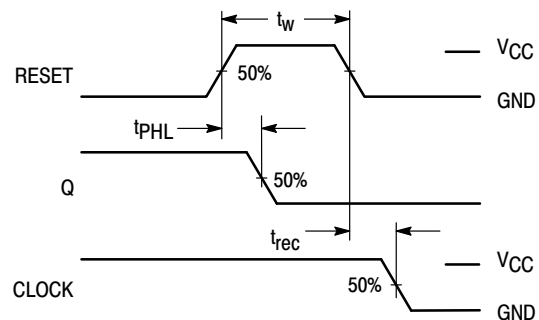
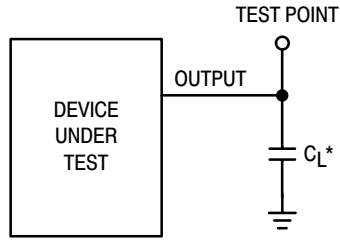


Figure 2.

MC74HC390A

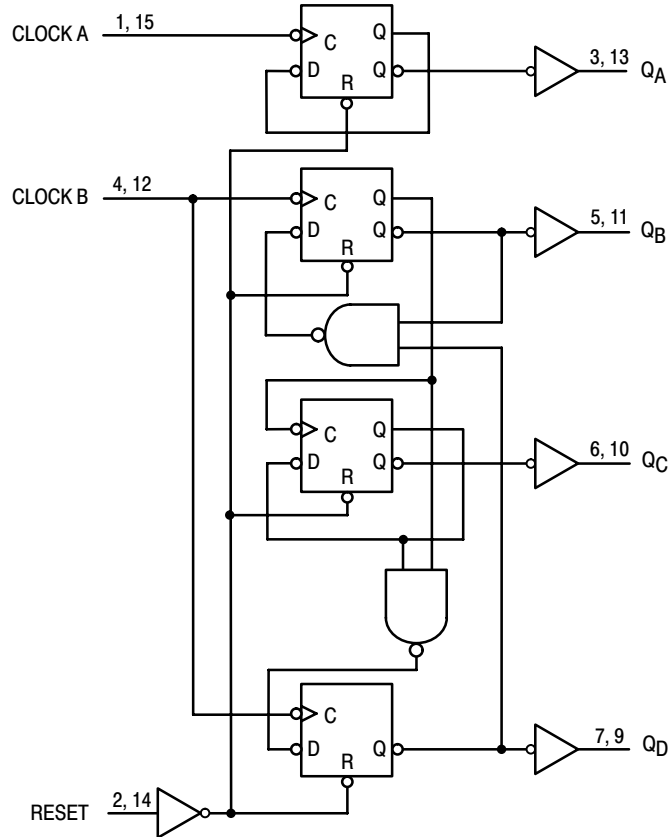
TEST CIRCUIT



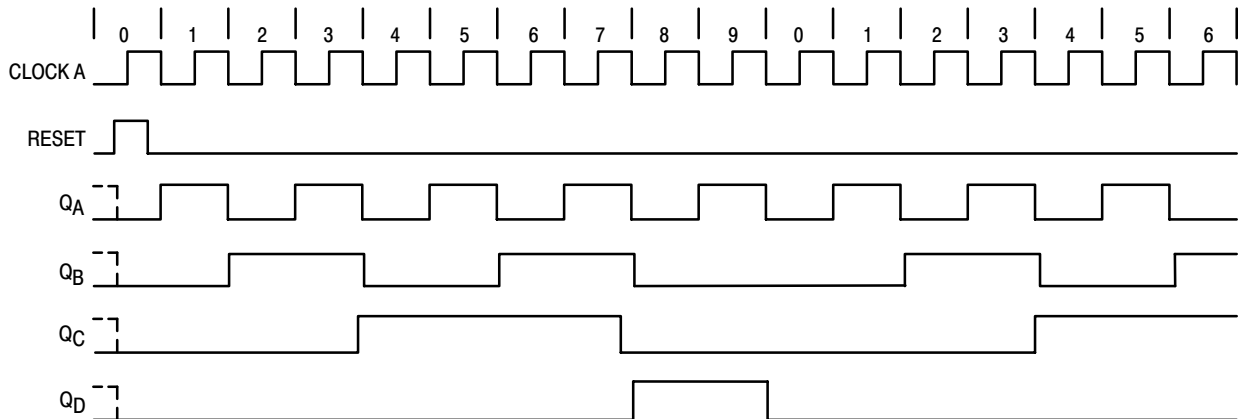
*Includes all probe and jig capacitance

Figure 3.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM (QA Connected to Clock B)



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APPLICATIONS INFORMATION

Each half of the MC54/74HC390A has independent $\div 2$ and $\div 5$ sections (except for the Reset function). The $\div 2$ and $\div 5$ counters can be connected to give BCD or bi-quinary (2–5) count sequences. If Output Q_A is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

To obtain a bi-quinary count sequence, the input signals connected to the Clock B input, and output Q_D is connected to the Clock A input (Figure 5). The bi-quinary count sequence function table is given in Table 2.

Table 1. BCD Count Sequence*

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

* Q_A connected to Clock B input.

Table 2. Bi-Quinary Count Sequence**

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

** Q_D connected to Clock A input.

CONNECTION DIAGRAMS

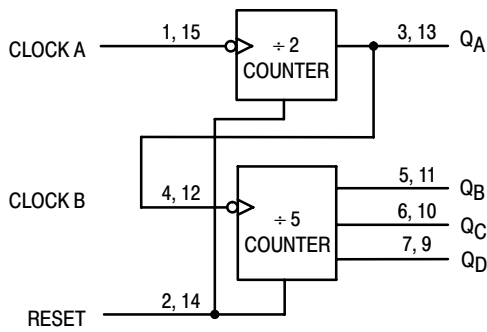


Figure 4. BCD Count

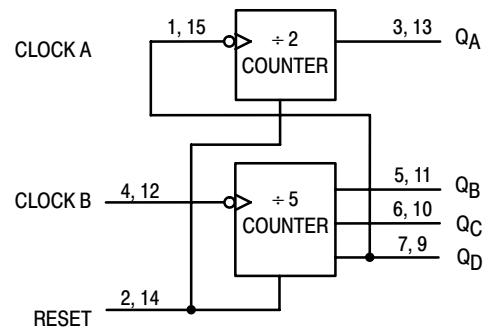


Figure 5. Bi-Quinary Count