

MITSUBISHI HIGH SPEED CMOS M74HC390P/FP/DP

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH $\div 2$ AND $\div 5$ SECTIONS

DESCRIPTION

The M74HC390 is a semiconductor integrated circuit consisting of two asynchronous decade counters with direct reset input.

FEATURES

- High-speed: (clock frequency) 60MHz typ. ($C_L=15\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation: $20\mu\text{W}/\text{package}$, max ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin: 30% of V_{CC} , min ($V_{CC}=4.5\text{V}$, 6V)
- Capable of driving 10 74LS TTL loads
- Wide operating voltage range: $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range: $T_a=-40\sim +85^\circ\text{C}$

APPLICATION

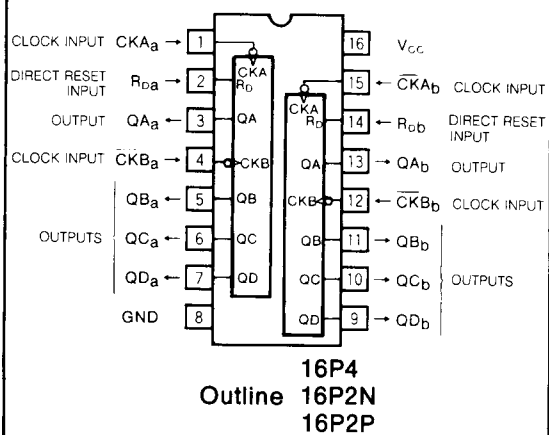
General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC390 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS390.

Each decade counter consists of a binary counter and a divide-by-5 counter. When using a binary counter, by applying the count pulse to clock input $\overline{\text{CKA}}$ a frequency-demultiplied signal will be output to QA. When using a divide-by-5 counter, by applying the count pulse to clock input $\overline{\text{CKB}}$ a frequency-demultiplied signal will be output to QB through QD.

PIN CONFIGURATION (TOP VIEW)

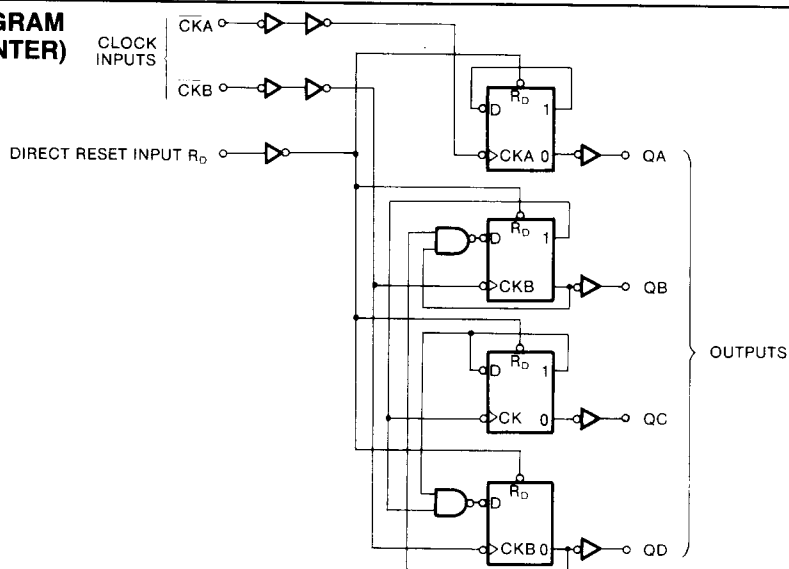


When using the decade counter to output BCD code from QA through QD, connect QA and $\overline{\text{CKB}}$ together and apply the count pulse to $\overline{\text{CKA}}$. When outputting a signal with a 50% duty cycle from QA, connect QD and CKA together and apply the count pulse to $\overline{\text{CKB}}$.

Counting takes place when the clock input changes from high-level to low-level.

When direct reset input R_D is high, QA through QB will become low irrespective of other inputs. Maintain the low-level state when counting.

LOGIC DIAGRAM (EACH COUNTER)



DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷ 2 AND ÷ 5 SECTIONS

FUNCTION TABLE (Note 1)

Inputs		Outputs			
CK	R _p	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	Count			

Note 1 : ↓ : Change from high to low level
X : Irrelevant

Count number	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

With QA and CKB connected and CKA used as input.

ABSOLUTE MAXIMUM RATINGS (T_a = -40~+85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
V _i	Input voltage		-0.5~V _{CC} +0.5	V
V _o	Output voltage		-0.5~V _{CC} +0.5	V
I _{iK}	Input protection diode current	V _i < 0V	-20	mA
		V _i > V _{CC}	20	
I _{oK}	Output parasitic diode current	V _o < 0V	-20	mA
		V _o > V _{CC}	20	
I _o	Output current per output pin		±25	mA
I _{CC}	Supply/GND current	V _{CC} , GND	±50	mA
P _d	Power dissipation	(Note 2)	500	mW
T _{stg}	Storage temperature range		-65~+150	°C

Note 2 : M74HC390FP, T_a = -40~+70°C and T_a = 70~85°C are derated at -6mW/°C.
M74HC390DP, T_a = -40~+50°C and T_a = 50~85°C are derated at -5mW/°C.

RECOMMENDED OPERATING CONDITIONS (T_a = -40~+85°C)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	2		6	V
V _i	Input voltage	0		V _{CC}	V
V _o	Output voltage	0		V _{CC}	V
T _{opr}	Operating temperature range	-40		+85	°C
t _r , t _f	Input risetime, falltime	V _{CC} = 2.0V	0	1000	ns
		V _{CC} = 4.5V	0	500	
		V _{CC} = 6.0V	0	400	

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷ 2 AND ÷ 5 SECTIONS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	V _{CC} (V)	Limits					Unit	
				25°C			-40~+85°C			
				Min	Typ	Max	Min	Max		
V _{IH}	High-level input voltage	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA	2.0	1.5			1.5		V	
			4.5	3.15			3.15			
			6.0	4.2			4.2			
V _{IL}	Low-level input voltage	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA	2.0					0.5	V	
			4.5				1.35	1.35		
			6.0				1.8	1.8		
V _{OH}	High-level output voltage	V _I = V _{IH} , V _{IL}	I _{OH} = -20μA	2.0	1.9			1.9	V	
				4.5	4.4			4.4		
			I _{OH} = -20μA	6.0	5.9			5.9		
				4.5	4.18			4.13		
			I _{OH} = -5.2mA	6.0	5.68			5.63		
V _{OL}	Low-level output voltage	V _I = V _{IH} , V _{IL}	I _{OL} = 20μA	2.0				0.1	V	
				4.5				0.1		0.1
			I _{OL} = 20μA	6.0				0.1		0.1
				4.5				0.26		0.33
			I _{OL} = 5.2mA	6.0				0.26		0.33
I _{IH}	High-level input current	V _I = 6V	6.0				0.1	1.0	μA	
I _{IL}	Low-level input current	V _I = 0V	6.0				-0.1	-1.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} , GND, I _O = 0μA	6.0				4.0	40.0	μA	

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f _{max}	Maximum clock frequency	C _L = 15pF (Note 4)	30			MHz
t _{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t _{THL}	Low-level to high-level and high-level to low-level output transition time				10	ns
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time (CKA - QA)				20	ns
t _{PHL}	Low-level to high-level and high-level to low-level output propagation time (CKA - QC, with QA and CKB connected)				20	ns
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time (CKB - QB)				50	ns
t _{PHL}	Low-level to high-level and high-level to low-level output propagation time (CKB - QC)				50	ns
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time (CKB - QD)				21	ns
t _{PHL}	Low-level to high-level and high-level to low-level output propagation time (CKB - QD)				21	ns
t _{PLH}	High-level to low-level output propagation time (R _D - QA, QB, QC, QD)				21	ns
t _{PHL}	High-level to low-level output propagation time (R _D - QA, QB, QC, QD)				21	ns
t _{PHL}	High-level to low-level output propagation time (R _D - QA, QB, QC, QD)				28	ns

DUAL 4-STAGE BINARY RIPPLE COUNTER WITH ÷ 2 AND ÷ 5 SECTIONS

SWITCHING CHARACTERISTICS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85^\circ C$)

Symbol	Parameter	Test conditions	Limits					Unit	
			V _{CC} (V)	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
f _{max}	Maximum clock frequency		2.0	5			4	MHz	
			4.5	27			21		
			6.0	31			24		
t _{TLH}	Low-level to high-level and high-level to low-level		2.0			75	95	ns	
			4.5			15	19		
			6.0			13	16		
t _{THL}	output transition time		2.0			75	95	ns	
			4.5			15	19		
			6.0			13	16		
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CKA} - QA$)		2.0			120	150	ns	
			4.5			24	30		
			6.0			21	26		
t _{PHL}	output propagation time ($\overline{CKA} - QA$)		2.0			120	150	ns	
			4.5			24	30		
			6.0			21	26		
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CKA} - QC$, with QA and CKB connected)		2.0			290	360	ns	
			4.5			58	72		
			6.0			50	62		
t _{PHL}	output propagation time ($\overline{CKA} - QC$, with QA and CKB connected)		2.0			290	360	ns	
			4.5			58	72		
			6.0			50	62		
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CKB} - QB$)	C _L = 50pF (Note 4)	2.0			130	160	ns	
			4.5			26	33		
			6.0			22	28		
t _{PHL}	output propagation time ($\overline{CKB} - QB$)	C _L = 50pF (Note 4)	2.0			130	160	ns	
			4.5			26	33		
			6.0			22	28		
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CKB} - QC$)		2.0			185	230	ns	
			4.5			37	46		
			6.0			32	40		
t _{PHL}	output propagation time ($\overline{CKB} - QC$)		2.0			185	230	ns	
			4.5			37	46		
			6.0			32	40		
t _{PLH}	Low-level to high-level and high-level to low-level output propagation time ($\overline{CKB} - QD$)		2.0			130	160	ns	
			4.5			26	33		
			6.0			22	28		
t _{PHL}	output propagation time ($\overline{CKB} - QD$)		2.0			130	160	ns	
			4.5			26	33		
			6.0			22	28		
t _{PHL}	High-level to low-level output propagation time ($R_0 - QA, QB, QC, QD$)		2.0			165	210	ns	
			4.5			33	41		
			6.0			28	35		
C _I	Input capacitance					10	pF		
C _{PD}	Power dissipation capacitance (Note 3)			46			pF		

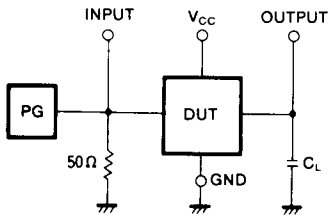
Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per counter)
The power dissipated during operation under no-load conditions is calculated using the following formula:
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

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TIMING REQUIREMENTS ($V_{CC} = 2\sim 6V$, $T_a = -40\sim +85^\circ C$)

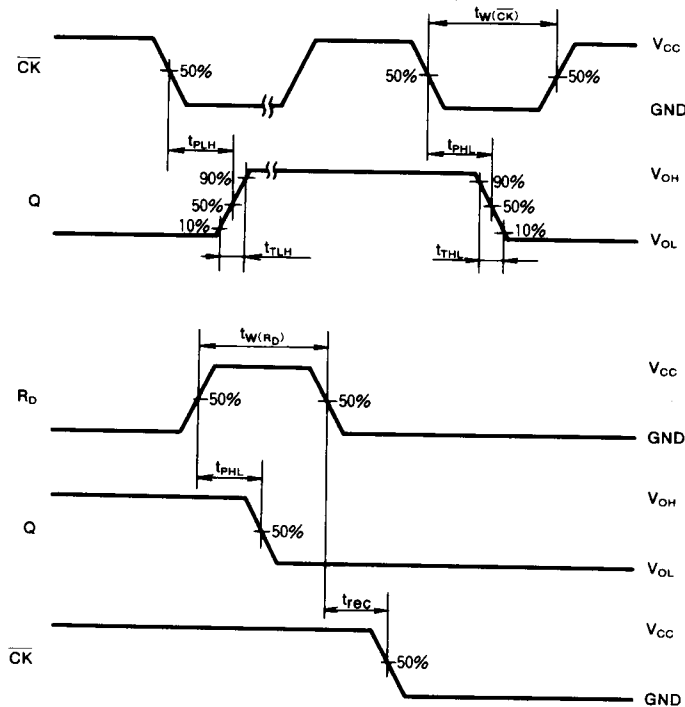
Symbol	Parameter	Test conditions	Limits					Unit	
			$V_{CC}(V)$	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
$t_{w(\overline{CK})}$	Clock pulse width		2.0	80			100	ns	
			4.5	16			20		
			6.0	14			18		
$t_{w(R_D)}$	Direct reset pulse width		2.0	80			100	ns	
			4.5	16			20		
			6.0	14			18		
t_{rec}	R_D recovery time with respect to CK		2.0	50			65	ns	
			4.5	10			13		
			6.0	9			11		

Note 4 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6ns$, $t_f = 6ns$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



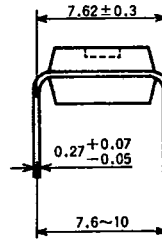
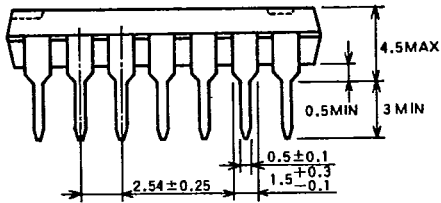
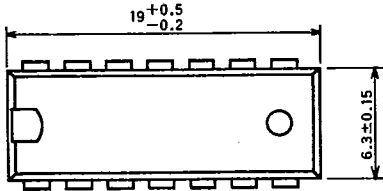
MITSUBISHI HIGH SPEED CMOS PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12849 D T-90-20

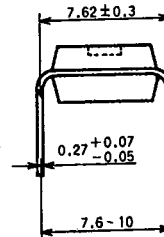
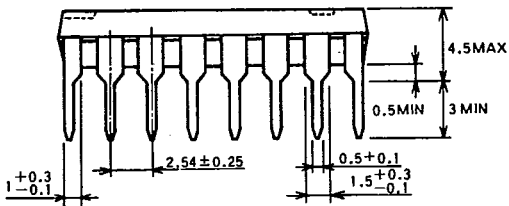
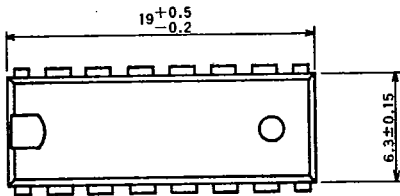
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

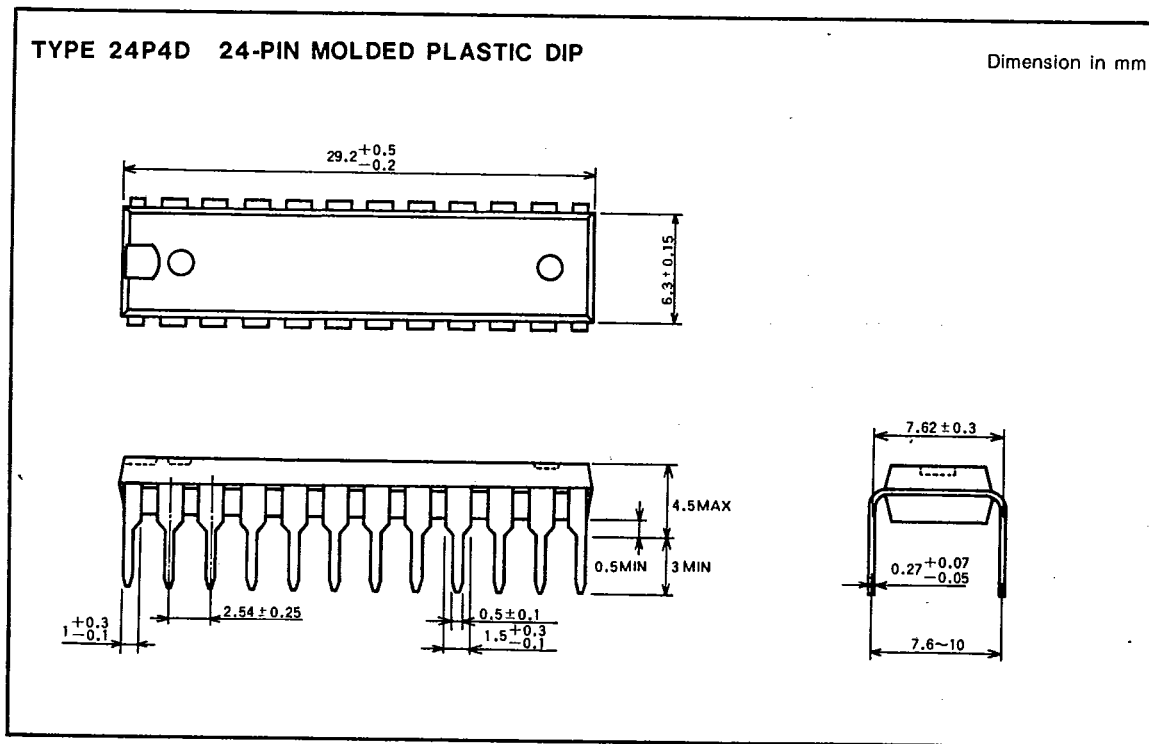
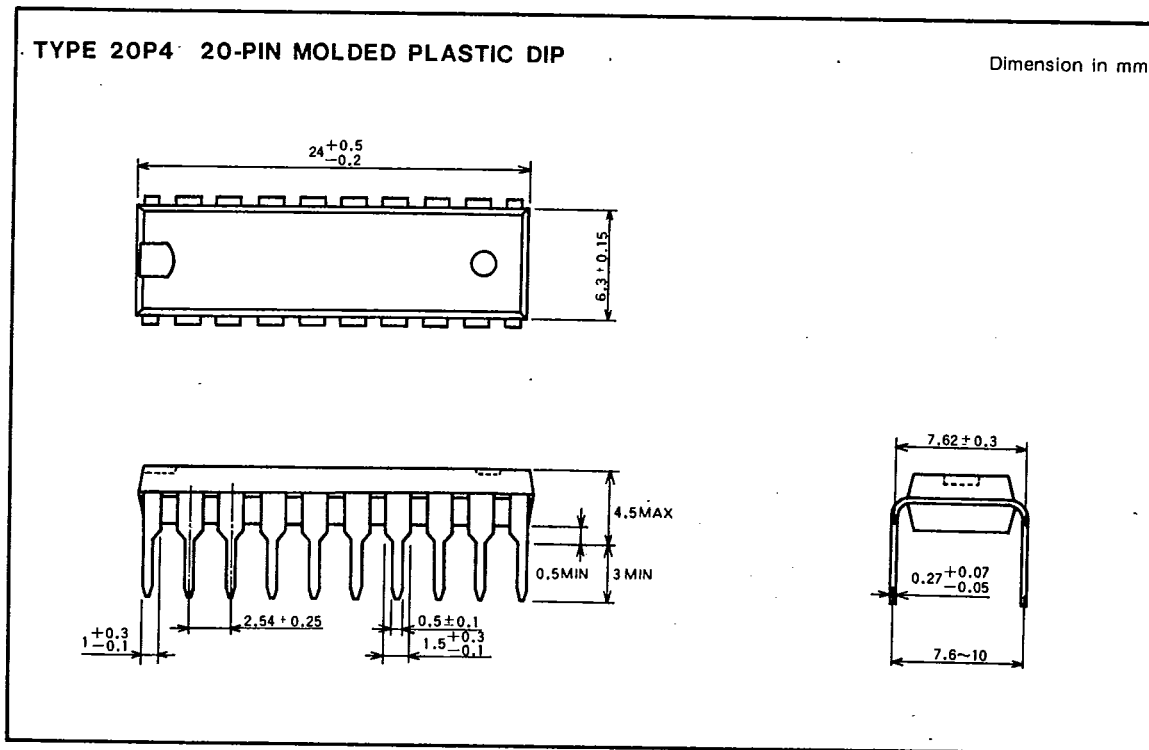
Dimension in mm



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12850 D.T-90-20



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MITSUBISHI ELECTRIC CO. TOKYO, JAPAN

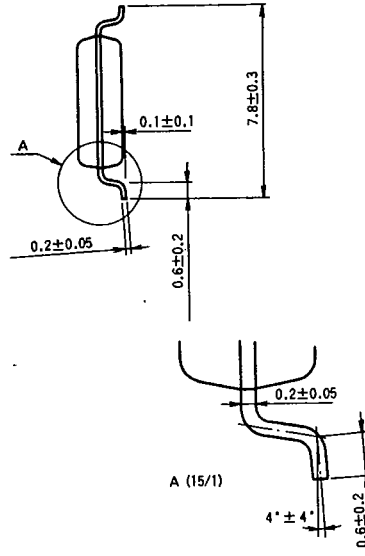
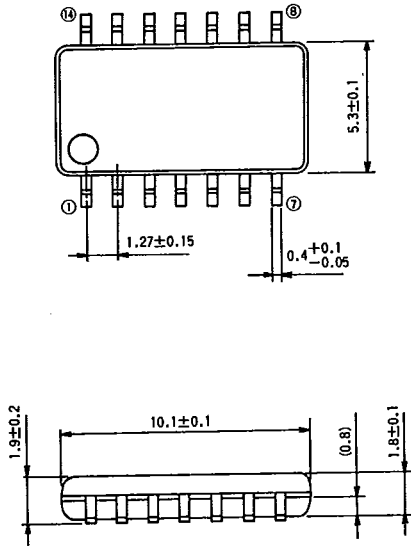
MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12851 D T-90.20

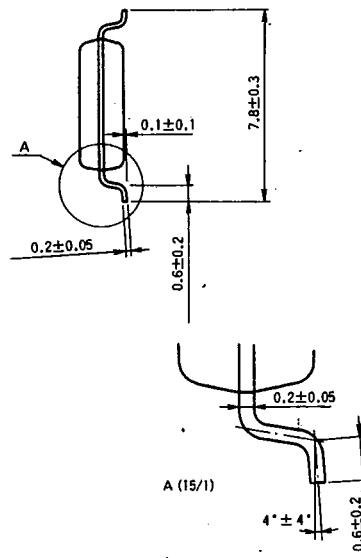
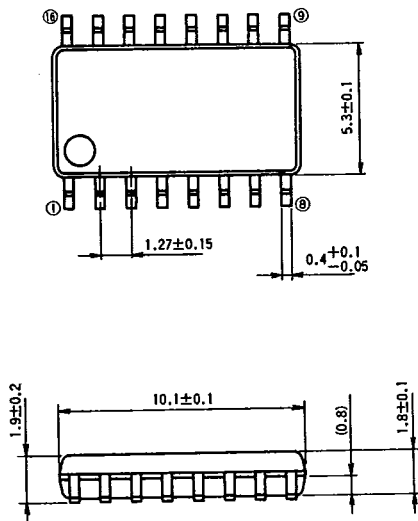
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



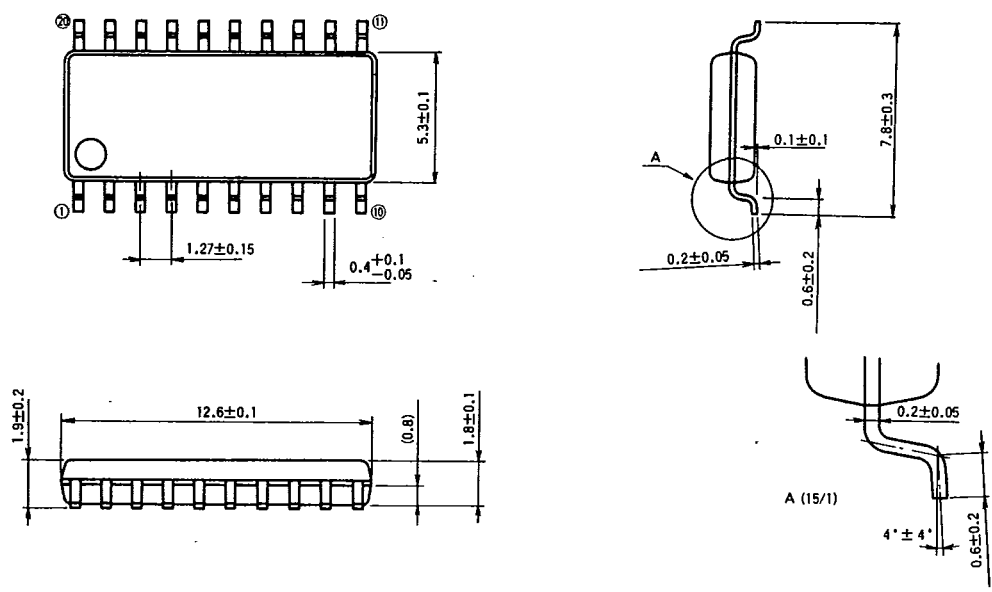
TYPE 16P2N 16PIN MOLDED PLASTIC SOP

Dimension in mm



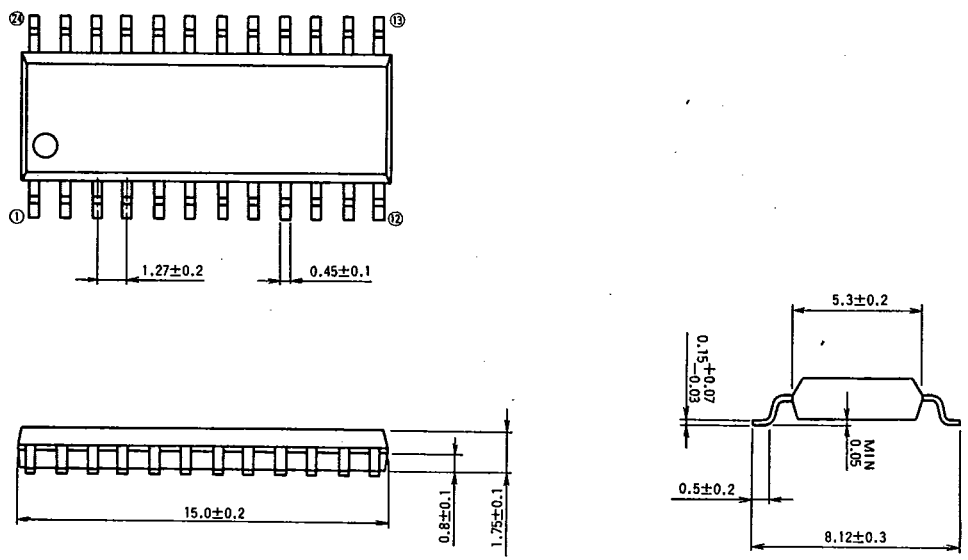
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



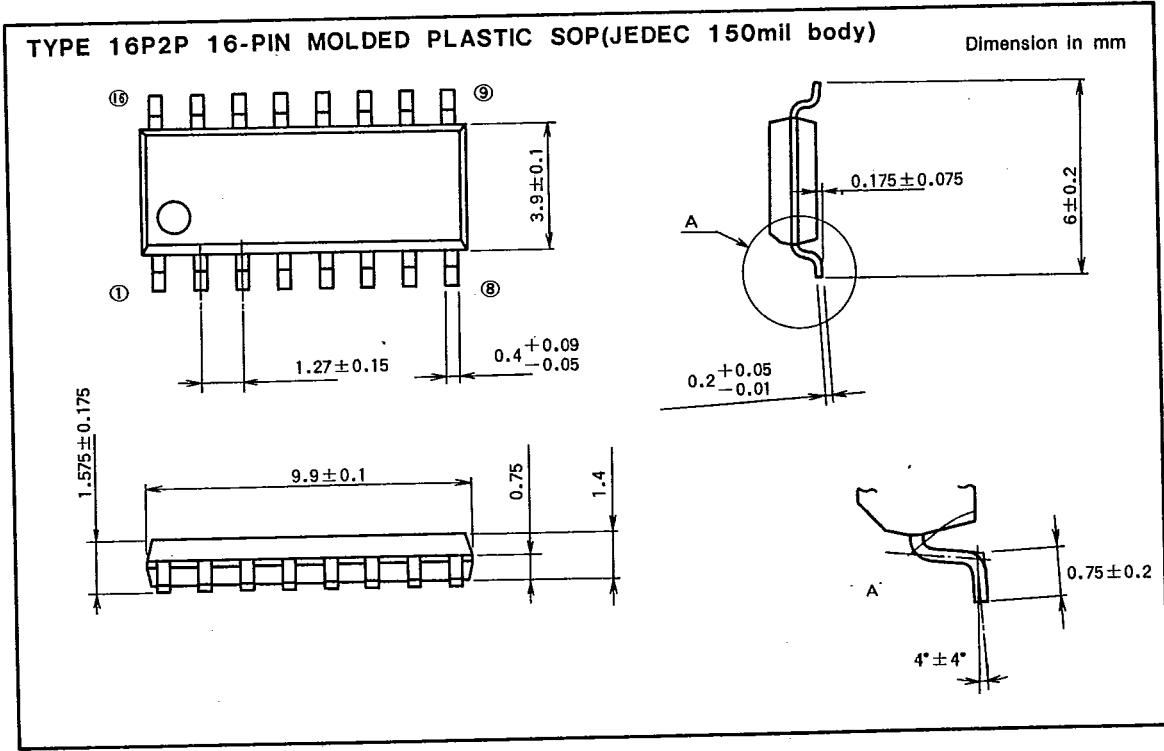
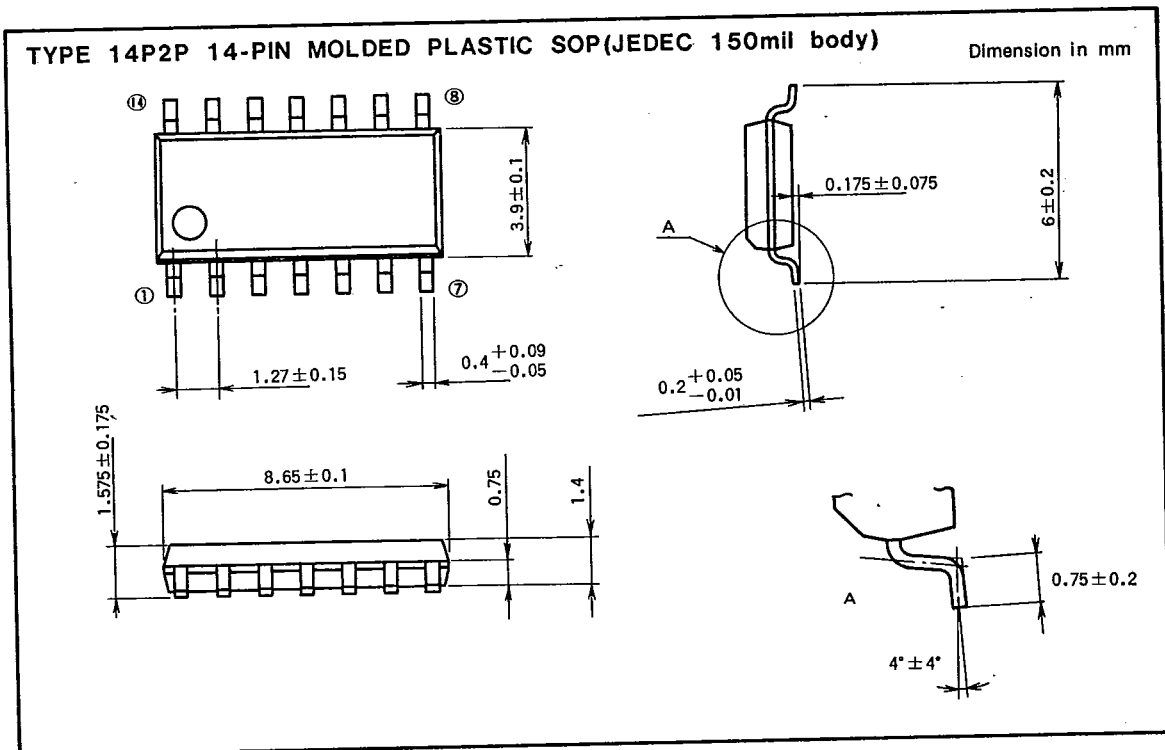
TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



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91D 12853 D T90-20



MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12854 D T-90-20

