

## MM54HC4017/MM74HC4017 Decade Counter/Divider with 10 Decoded Outputs

### General Description

The MM54HC4017/MM74HC4017 is a 5-stage Johnson counter with 10 decoded outputs that utilizes advanced silicon-gate CMOS technology. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output transitions low to high after OUTPUT 9 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low except output 0.

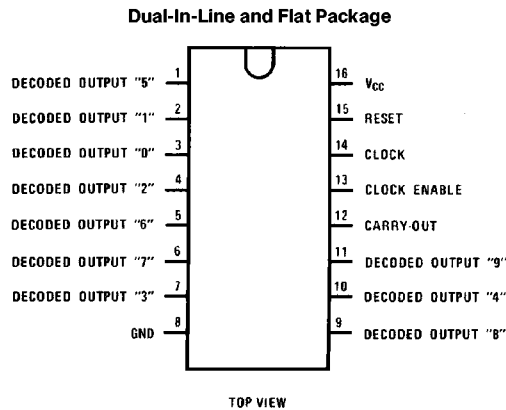
The MM54HC4017/MM74HC4017 is functionally and pinout equivalent to the CD4017BM/CD4017BC. It can drive

up to 10 low power Schottky equivalent loads. All inputs are protected from damage due to static discharge by diodes from  $V_{CC}$  and ground.

### Features

- Wide power supply range: 2–6V
- Typical operating frequency: 30 MHz
- Fanout of 10 LS-TTL loads
- Low quiescent current: 80  $\mu$ A (74HC Series)
- Low input current: 1.0  $\mu$ A

### Connection Diagram



TL/F/5351-1

Order Number MM54HC4017 or MM74HC4017

MM54HC4017/MM74HC4017 Decade Counter/Divider with 10 Decoded Outputs

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC	54HC	Units
						$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	
				Typ				
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

### AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Clock Frequency	Measured with respect to carry line	50	30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Enable to Carry-Out Line		26	44	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Enable Decode-Out Lines		27	44	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Reset or Clock to Decode Out		23	40	ns
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Reset or Clock to Carry Out		23	40	ns
$t_S$	Minimum Clock Inhibit to Clock Set-Up Time		12	20	ns
$t_W$	Minimum Clock or Reset Pulse Width		8	16	ns
$t_{REM}$	Minimum Reset Removal Time		20	10	ns

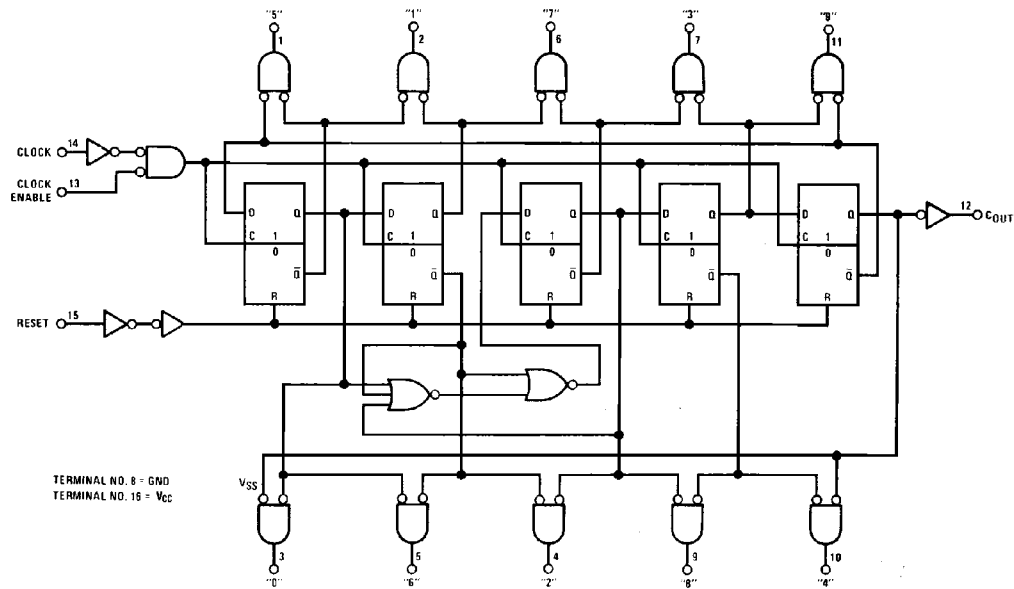
### AC Electrical Characteristics $V_{CC}=2.0-6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^{\circ}C$			74HC $T_A = -40\text{ to }85^{\circ}C$		54HC $T_A = -55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits		Guaranteed Limits		Guaranteed Limits		
$f_{MAX}$	Maximum Clock Frequency	Measured with respect to carry line	2.0V		6	5	4			MHz	
			4.5V		30	24	20		MHz		
			6.0V		35	28	24		MHz		
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Enable to Carry-Out Line		2.0V	89	250	312	375		ns		
			4.5V	25	50	63	75		ns		
			6.0V	20	43	54	65		ns		
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Enable to Decode Out Line		2.0V	90	250	312	375		ns		
			4.5V	25	50	63	75		ns		
			6.0V	20	43	54	65		ns		
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Reset or Clock to Decode Out		2.0V	82	230	288	345		ns		
			4.5V	22	46	58	69		ns		
			6.0V	18	39	49	59		ns		
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Reset or Clock to Carry Out		2.0V	82	230	288	345		ns		
			4.5V	22	46	58	69		ns		
			6.0V	18	39	49	59		ns		
$t_W$	Minimum Reset, Clock, or Clock Enable Pulse Width		2.0V	30	80	100	120		ns		
			4.5V	9	16	20	24		ns		
			6.0V	8	14	18	21		ns		
$t_{REM}$	Minimum Reset Removal Time		2.0V		100	125	150		ns		
			4.5V		20	25	30		ns		
			6.0V		17	21	25		ns		
$t_S, t_H$	Minimum Clock Inhibit to Clock Set-Up or Hold Time		2.0V		50	63	75		ns		
			4.5V		10	13	15		ns		
			6.0V		9	11	13		ns		
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110		ns		
			4.5V	8	15	19	22		ns		
			6.0V	7	13	16	19		ns		
$t_r, t_f$	Minimum Input Rise and Fall Time		2.0V		1000	1000	1000		ns		
			4.5V		500	500	500		ns		
			6.0V		400	400	400		ns		
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per package)							pF		
$C_{IN}$	Maximum Input Capacitance			5	10	10	10		pF		

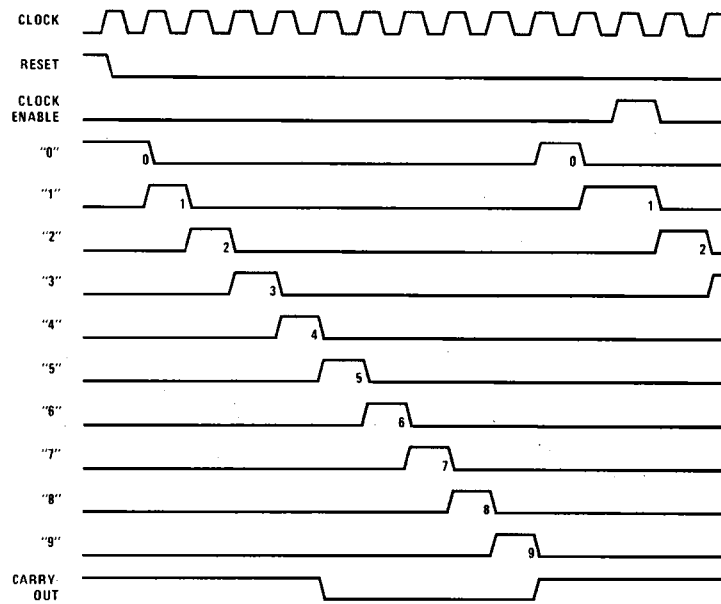
**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

# Logic and Timing Diagrams

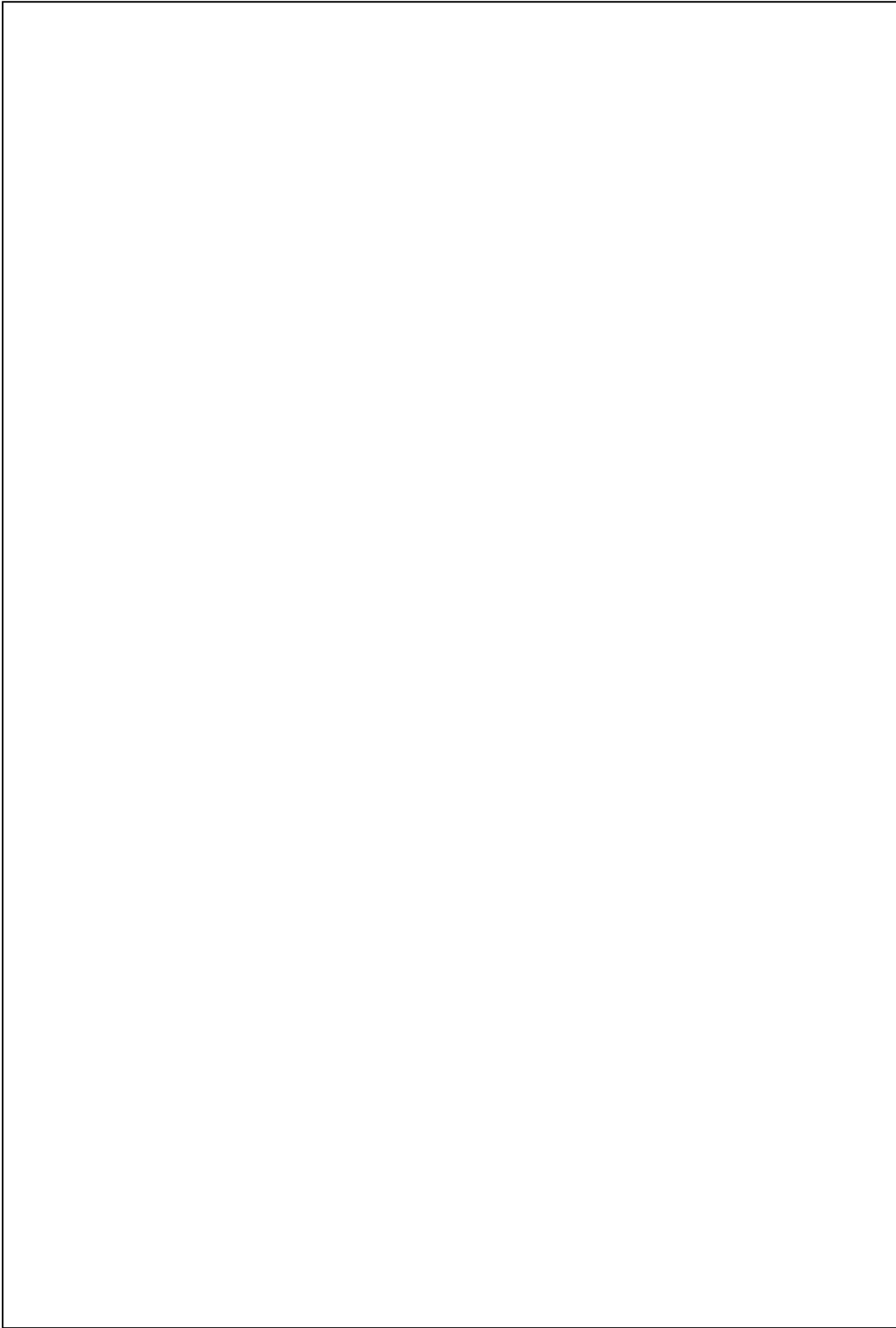
MM54HC4017/MM74HC4017



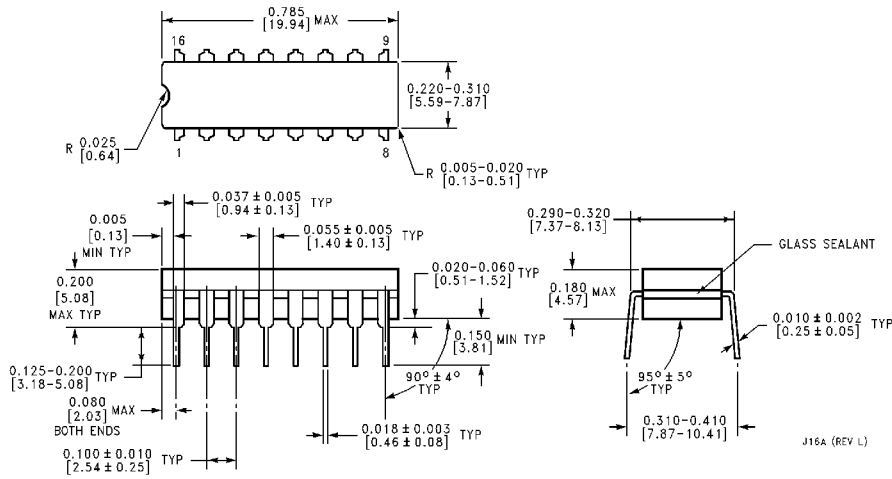
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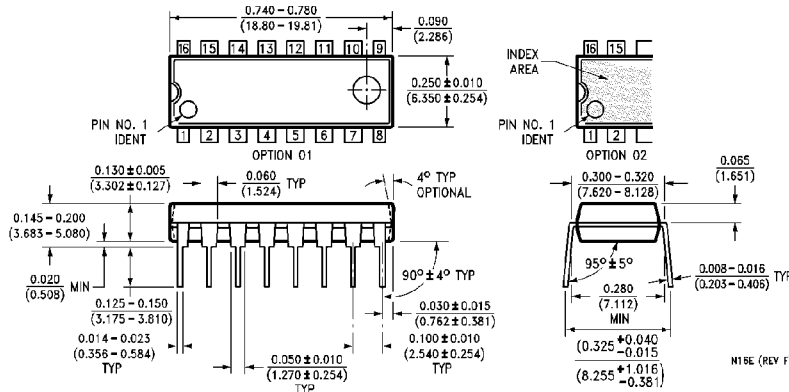
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**Physical Dimensions** inches (millimeters)



**Dual-In-Line and Flat Package**  
**Order Number MM54HC4017J or MM74HC4017J,N**  
**NS Package Number J16A**



**Dual-In-Line and Flat Package**  
**Order Number MM74HC4017N**  
**NS Package Number N16E**

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