

SN74LS393

Dual 4-Stage Binary Counter

The SN74LS393 contains a pair of high-speed 4-stage ripple counters.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

GUARANTEED OPERATING RANGES

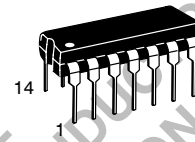
| Symbol | Parameter | Min | Typ | Max | Unit |
|----------|-------------------------------------|------|-----|------|------|
| V_{CC} | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| T_A | Operating Ambient Temperature Range | 0 | 25 | 70 | °C |
| I_{OH} | Output Current - High | | | -0.4 | mA |
| I_{OL} | Output Current - Low | | | 8.0 | mA |



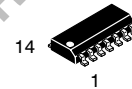
ON Semiconductor™

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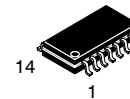
LOW
POWER
SCHOTTKY



PLASTIC
N SUFFIX
CASE 646



SOIC
D SUFFIX
CASE 751A



SOEIAJ
M SUFFIX
CASE 965

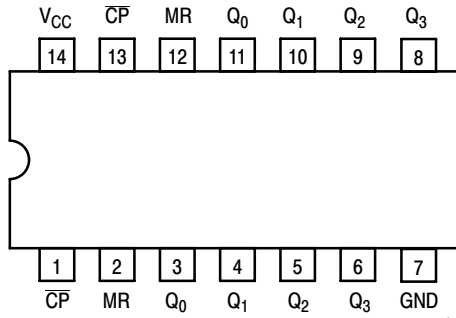
ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|------------|------------------|
| SN74LS393N | 14 Pin DIP | 2000 Units/Box |
| SN74LS393D | SOIC-14 | 55 Units/Rail |
| SN74LS393DR2 | SOIC-14 | 2500/Tape & Reel |
| SN74LS393M | SOEIAJ-14 | See Note 1 |
| SN74LS393MEL | SOEIAJ-14 | See Note 1 |

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

SN74LS393

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

| PIN NAMES | | LOADING (Note a) | |
|-------------------|---|------------------|-----------|
| | | HIGH | LOW |
| \overline{CP} | Clock (Active LOW Going Edge) Input to +16 (LS393) | 0.5 U.L. | 1.0 U.L. |
| \overline{CP}_0 | Clock (Active LOW Going Edge) Input to +2 (LS390) | 0.5 U.L. | 1.0 U.L. |
| \overline{CP}_1 | Clock (Active LOW Going Edge) Input to +5 (LS390) | 0.5 U.L. | 1.5 U.L. |
| MR | Master Reset (Active HIGH) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0 - Q_3$ | Flip-Flop Outputs | 10 U.L. | 5 U.L. |

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

OBSOLETE

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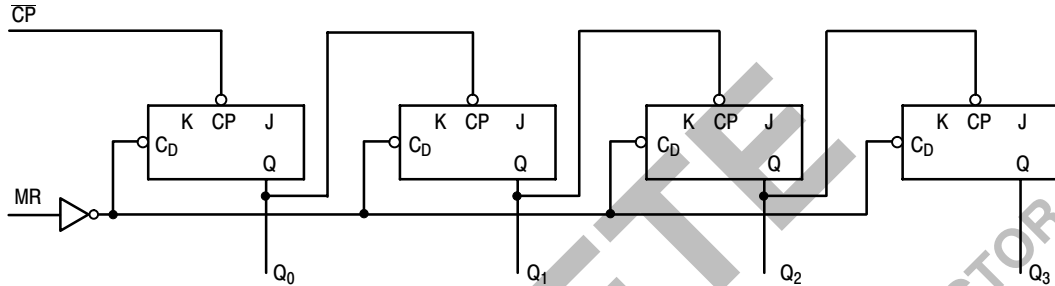
SN74LS393

FUNCTIONAL DESCRIPTION

Each half of the SN74LS393 operates in the Modulo 16 binary sequence, as indicated in the ± 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do

not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

SN74LS393 LOGIC DIAGRAM (one half shown)



TRUTH TABLE

| COUNT | OUTPUTS | | | |
|-------|----------------|----------------|----------------|----------------|
| | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H = HIGH Voltage Level
L = LOW Voltage Level

SN74LS393

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|-----------------|--------------------------------|---------------------|-------|------|------|--|
| | | Min | Typ | Max | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.7 | 3.5 | | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table |
| V _{OL} | Output LOW Voltage | | 0.25 | 0.4 | V | I _{OL} = 4.0 mA |
| | | | 0.35 | 0.5 | V | I _{OL} = 8.0 mA |
| I _{IH} | Input HIGH Current | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V |
| I _{IL} | Input LOW Current | MR | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V |
| | | CP, CP ₀ | | -1.6 | mA | |
| | | CP ₁ | | -2.4 | mA | |
| I _{OS} | Short Circuit Current (Note 2) | -20 | | -100 | mA | V _{CC} = MAX |
| I _{CC} | Power Supply Current | | | 26 | mA | V _{CC} = MAX |

2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------------------------------------|--|--------|----------|----------|------|------------------------|
| | | Min | Typ | Max | | |
| f _{MAX} | Maximum Clock Frequency CP ₀ to Q ₀ | 25 | 35 | | MHz | C _L = 15 pF |
| f _{MAX} | Maximum Clock Frequency CP ₁ to Q ₁ | 20 | | | MHz | |
| t _{PLH} t _{PHL} | Propagation Delay, CP to Q ₀ | | 12 13 | 20 20 | ns | |
| t _{PLH} t _{PHL} | CP to Q ₃ | | 40 40 | 60 60 | ns | |
| t _{PHL} | MR to Any Output | | 24 | 39 | ns | |

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|-------------------|--------|-----|-----|------|-------------------------|
| | | Min | Typ | Max | | |
| t _W | Clock Pulse Width | 20 | | | ns | V _{CC} = 5.0 V |
| t _W | MR Pulse Width | 20 | | | ns | |
| t _{rec} | Recovery Time | 25 | | | ns | |

SN74LS393

AC WAVEFORMS

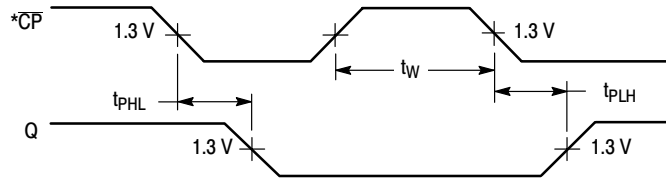


Figure 1.

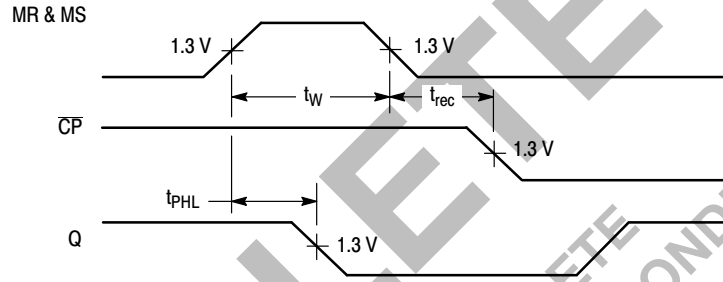


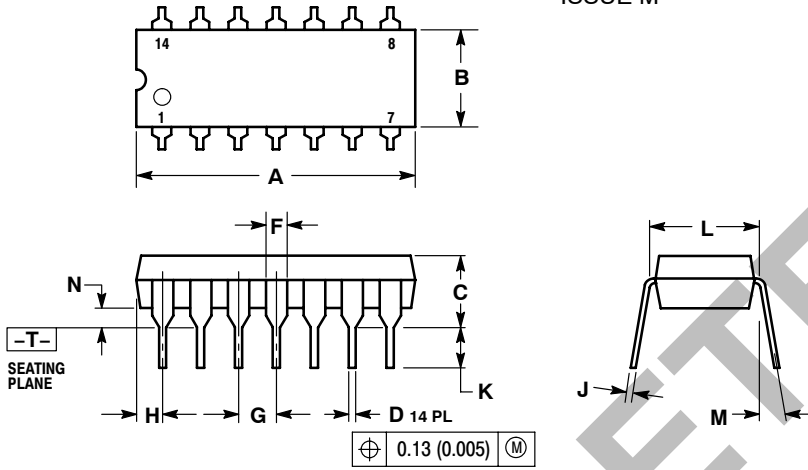
Figure 2.

*The number of Clock Pulses required between t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.

SN74LS393

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE M



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 18.80 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

OBSOLETE

THIS DEVICE IS OBSOLETE

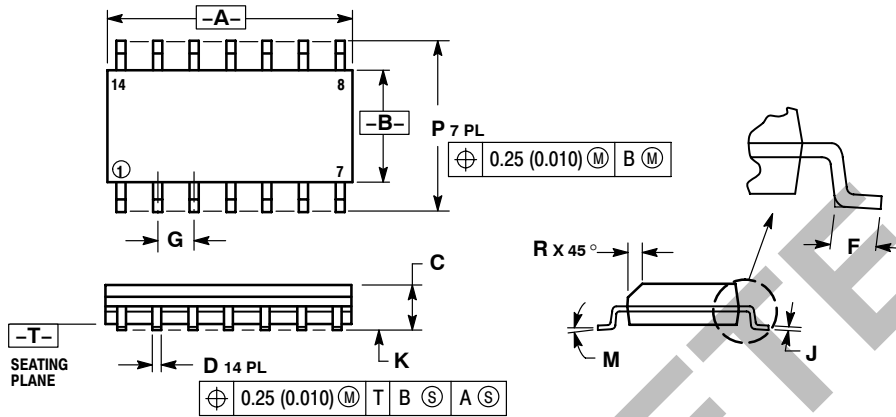
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SN74LS393

PACKAGE DIMENSIONS

D SUFFIX
 PLASTIC SOIC PACKAGE
 CASE 751A-03
 ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

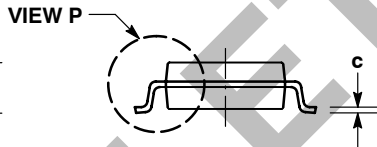
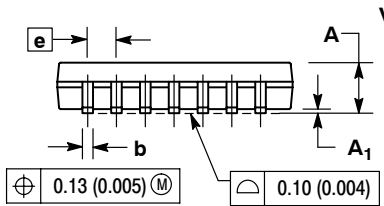
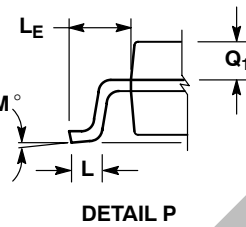
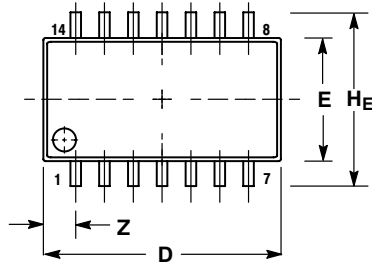
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SN74LS393

PACKAGE DIMENSIONS

M SUFFIX
SOEIAJ PACKAGE
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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