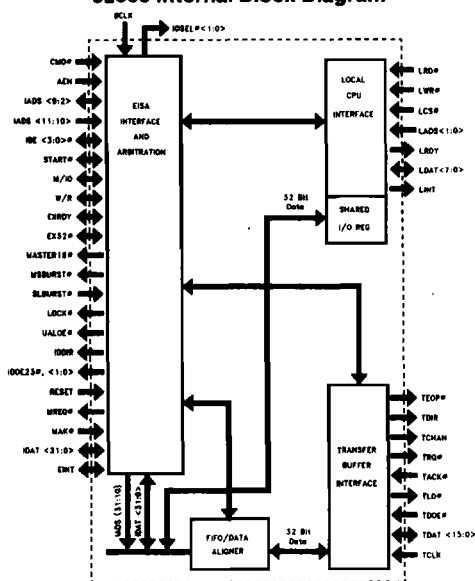# intel®

82355
BUS MASTER INTERFACE CONTROLLER
(BMIC)

- **Designed for use in 32-Bit EISA Bus Master Expansion Board Designs**
  - Integrates Three Interfaces (EISA, Local CPU, and Transfer Buffer)

- **Supports 16- and 32-Bit Burst Transfers**
  - 33 Mbytes/Sec Maximum Data Transfers

- **Supports 32-Bit Non-Burst and Mismatched Data Size Transfers**

- **Supports 32-Bit EISA Addressability (4 Gigabyte)**

- **Two Independent Data Transfer Channels with 24-Byte FIFOs**
  - Expansion Board Timing and EISA Timing Operate Asynchronously

- **Supports Peek/Poke Operation with the Ability to Access Individual Locations in EISA Memory or I/O space**

- **Automatically Handles Misaligned Doubleword Data Transfers with No Performance Penalty**

- **Supports Automatic Handling of Complete EISA Bus Master Protocol**
  - EISA Arbitration/Preemption
  - Cycle Timing and Execution
  - Byte Alignment
  - 1K Boundary Detection

- **Supports Local Data Transfer Protocol Similar to Traditional DMA**

- **Supports a General Purpose Command and Status Interface**
  - Local and EISA System Interrupt Support
  - General Purpose Information Transfers
  - Set-and-Test-Functions in I/O Space (Semaphore Function)
  - Supports the EISA Expansion Board ID Function

- **Supports Decode of Slot Specific and General I/O Addresses**

- **132-Pin JEDEC PQFP Package**
  (See Packaging Specification Order #240800, Package Type NG)

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82355 Internal Block Diagram

290255-1

The complete document for this product is available from Intel's Literature Center at 1-800-548-4725.