KSZ8852HLE

Two-Port 10/100 Ethernet Switch with 8-/16-Bit Host Interface

Features

Management Capabilities:

- The KSZ8852 includes all the Functions of a 10/100BASE-T/TX Switch System which Combines a Switch Engine, Frame Buffer Management, Address Look-Up Table, Queue Management, MIB Counters, Media Access Controllers (MAC) and PHY Transceivers
- Non-Blocking Store-and-Forward Switch Fabric Assures Fast Packet Delivery by Utilizing 1024 Entry Forwarding Table
- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port
- MIB Counters for Fully Compliant Statistics Gathering-34 Counters Per Port
- Loopback Modes for Remote Failure Diagnostics
- Rapid Spanning Tree Protocol Support (RSTP) for Topology Management and Ring/Linear Recovery

Robust PHY Ports

- Two Integrated IEEE 802.3/802.3u Compliant Ethernet Transceivers Supporting 10BASE-T and 100BASE-TX
- On-Chip Termination Resistors and Internal Biasing for Differential Pairs to Reduce Power
- HP Auto MDI/MDI-X™ Crossover Support Eliminating the Need to Differentiate Between Straight or Crossover Cables in Applications

MAC Ports

- Three Internal Media Access Control (MAC) Units
- 2Kbyte Jumbo Packet Support
- Tail Tagging Mode (One Byte Added Before FCS) Support at Port 3 to Inform the Processor which Ingress Port Receives the Packet and it's Priority
- Programmable MAC Addresses for Port 1 and Port 2 and Self-Address Filtering Support
- MAC Filtering Function to Filter or Forward Unknown Unicast Packets

Advanced Switch Capabilities

- Non-Blocking Store-and-Forward Switch Fabric Assures Fast Packet Delivery By Utilizing 1024 Entry Forwarding Table
- IEEE 802.1Q VLAN for Up To 16 Groups with a Full Range of VLAN IDs
- IEEE 802.1p/Q Tag Insertion or Removal on a Per-Port Basis (Egress) and Support Double-Tagging
- VLAN ID Tag/Untag Options on Per Port Basis
- Fully Compliant With IEEE 802.3/802.3u Standards
- IEEE 802.3x Full-Duplex with Force Mode Option and Half-Duplex Backpressure Collision Flow Control
- IEEE 802.1w Rapid Spanning Tree Protocol Support
- IGMP v1/v2/v3 Snooping for Multicast Packet Filtering
- QoS/CoS Packets Prioritization Support: 802.1p, DiffServ-Based and Re-Mapping Of 802.1p Priority Field Per Port Basis on Four Priority Levels
- IPv4/IPv6 QoS Support
- IPv6 Multicast Listener Discovery (MLD) Snooping Support
- Programmable Rate Limiting at the Ingress and Egress Ports
- Broadcast Storm Protection
- 1K Entry Forwarding Table with 32K Frame Buffer
- Four Priority Queues with Dynamic Packet Mapping for IEEE 802.1P, IPv4 TOS (DIFFSERV), IPv6 Traffic Class, Etc.
- Source Address Filtering for Implementing Ring Topologies

Comprehensive Configuration Registers Access

- Complete Register Access Via the Parallel Host Interface
- Facility to Load MAC Address from EEPROM At Power Up and Reset Time
- I/O Pin Strapping Facility to Set Certain Register Bits from I/O Pins at Reset Time
- Control Registers Configurable On-The-Fly

Host Interface

- Selectable 8-bit or 16-bit Wide Interface
- Supports Big- and Little-Endian Processors
- Indirect Data Bus for Data, Address and Byte Enable to Access any I/O Registers and RX/TX FIFO Buffers
- Large Internal Memory with 12KByte for RX FIFO and 6Kbytes for TX FIFO
- Programmable Low, High and Overrun Water

Marks for Flow Control in RX FIFO
- Efficient Architecture Design with Configurable Host Interrupt Schemes to Minimize Host CPU Overhead and Utilization
- Queue Management Unit (QMU) Supervises Data Transfers Across this Interface

Power and Power Management

- Single 3.3V Power Supply with Optional VDD I/O for 1.8V, 2.5V, or 3.3V
- Integrated Low-Voltage (~1.3V) Low-Noise Regulator (LDO) Output for Digital and Analog Core Power
- Supports IEEE P802.3az™ Energy Efficient Ethernet (EEE) To Reduce Power Consumption In Transceivers In LPI State
- Full-Chip Hardware or Software Power Down (All Registers Value are not Saved and Strap-In Value will Re-Strap after Releasing the Power Down)
- Energy Detect Power Down (EDPD), which Disables the PHY Transceiver when Cables are Removed
- Wake On LAN Supported with Configurable Packet Control
- Dynamic Clock Tree Control to Reduce Clocking in Areas not in Use
- Power Consumption Less than 0.5W

Additional Features

- Single 25 MHz +50 ppm Reference Clock Requirement
- Comprehensive Programmable Two LED Indicators Support for Link, Activity, Full/Half Duplex and 10/100 Speed

Packaging

- Commercial Temperature Range: 0°C to +70°C and Extended Industrial Temperature Ranges: –40°C to +105°C and –40°C to +115°C
- 64-pin (10 mm × 10 mm) Lead Free (RoHS) LQFP Package with Heat Exposed Ground Paddle for Low Thermal Resistance
- 0.11 µm Technology for Lower Power Consumption

Applications

- General and Industrial Ethernet Applications
- Wireless LAN Access Point and Gateway
- Set Top / Game Box
- Test and Measurement Equipment
- Automotive

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

Table of Contents

1.0 INTRODUCTION

1.1 General Terms and Conditions

The following is list of the general terms used throughout this document:

BIU - Bus Interface Unit	The host interface function that performs code conversion, buffering, and the like required for communications to and from a network.
BPDU - Bridge Protocol Data Unit	A packet containing ports, addresses, etc. to make sure data being passed through a bridged network arrives at its proper destination.
CMOS - Complementary Metal Oxide Semiconductor	A common semiconductor manufacturing technique in which positive and negative types of transistors are combined to form a current gate that in turn forms an effective means of controlling electrical current through a chip.
CRC - Cyclic Redundancy Check	A common technique for detecting data transmission errors. CRC for Ethernet is 32 bits long.
Cut-Through Switch	A switch typically processes received packets by reading in the full packet (storing), then processing the packet to determine where it needs to go, then forwarding it. A cut-through switch simply reads in the first bit of an incoming packet and forwards the packet. Cut-through switches do not store the packet.
DA - Destination Address	The network address to which packets are sent.
DMA - Direct Memory Access	A design in which memory on a chip is controlled independently of the CPU.
EMI - Electromagnetic Interference	A naturally occurring phenomena when the electromagnetic field of one device disrupts, impedes or degrades the electromagnetic field of another device by coming into proximity with it. In computer technology, computer devices are susceptible to EMI because electromagnetic fields are a byproduct of passing electricity through a wire. Data lines that have not been properly shielded are susceptible to data corruption by EMI.
FCS - Frame Check Sequence	See CRC.
FID - Frame or Filter ID	Specifies the frame identifier. Alternately is the filter identifier.
IGMP - Internet Group Management Protocol	The protocol defined by RFC 1112 for IP multicast transmissions.
IPG - Inter-Packet Gap	A time delay between successive data packets mandated by the network standard for protocol reasons. In Ethernet, the medium has to be "silent" (i.e., no data transfer) for a short period of time before a node can consider the network idle and start to transmit. IPG is used to correct timing differences between a transmitter and receiver. During the IPG, no data is transferred, and information in the gap can be discarded or additions inserted without impact on data integrity.
ISA - Industry Standard Architecture	A bus architecture used in the IBM PC/XT and PC/AT.
ISI - Inter-Symbol Interference	The disruption of transmitted code caused by adjacent pulses affecting or interfering with each other.
Jumbo Packet	A packet larger than the standard Ethernet packet (1500 bytes). Large packet sizes allow for more efficient use of bandwidth, lower overhead, less processing, etc.
MAC - Media Access Controller	A functional block responsible for implementing the Media Access Control layer which is a sub layer of the Data Link Layer.
MDI - Medium Dependent Interface	An Ethernet port connection that allows network hubs or switches to connect to other hubs or switches without a null-modem, or cross-over, cable. MDI provides the standard interface to a particular media (copper or fiber) and is therefore “media dependent”.

MDI-X - Medium Dependent Interface Crossover	An Ethernet port connection that allows networked end stations (i.e., PCs or workstations) to connect to each other using a null-modem, or crossover, cable. For 10/100 full-duplex networks, an end point (such as a computer) and a switch are wired so that each transmitter connects to the far end receiver. When connecting two computers together, a cable that crosses the TX and RX is required to do this. With auto MDI-X, the PHY senses the correct TX and RX roles, eliminating any cable confusion.
MIB - Management Information Base	The MIB comprises the management portion of network devices. This can include things like monitoring traffic levels and faults (statistical), and can also change operating parameters in network nodes (static forwarding addresses).
MII - Media Independent Interface	The MII accesses PHY registers as defined in the IEEE 802.3 specification.
NIC - Network Interface Card	An expansion board inserted into a computer to allow it to be connected to a network. Most NICs are designed for a particular type of network, protocol, and media, although some can serve multiple networks.
NPVID - Non Port VLAN ID	The Port VLAN ID value is used as a VLAN reference.
PLL - Phase-Locked Loop	An electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e., lock) on the frequency of an input, or reference, signal. A PLL ensures that a communication signal is locked on a specific frequency and can also be used to generate, modulate, and demodulate a signal and divide a frequency.
QMU - Queue Management Unit	Manages packet traffic between MAC/PHY interface and the system host. The QMU has built-in packet memories for receive and transmit functions called TXQ (Transmit Queue) and RXQ (Receive Queue).
SA - Source Address	The address from which information has been sent.
TDR - Time Domain Reflectometry	TDR is used to pinpoint flaws and problems in underground and aerial wire, cabling, and fiber optics. They send a signal down the conductor and measure the time it takes for the signal, or part of the signal, to return.
VLAN - Virtual Local Area Network	A configuration of computers that acts as if all computers are connected by the same physical network but which may be located virtually anywhere.

1.2 General Description

The KSZ8852 product line consists of industrial capable Ethernet switches, providing integrated communication for a range of Industrial Ethernet and general Ethernet applications.

The KSZ8852 product enables distributed, daisy-chained topologies preferred for industrial Ethernet networks. Conventional centralized (i.e., star-wired) topologies are also supported for fault tolerant arrangements.

A flexible 8 or 16-bit general bus interface is provided for interfacing to an external host processor.

The wire-speed, store-and-forward switching fabric provides a full complement of QoS and congestion control features optimized for real-time Ethernet

The KSZ8852 product is built upon Microchip's industry-leading Ethernet technology, with features designed to offload host processing and streamline your overall design:

- Wire-speed Ethernet switching fabric with extensive filtering
- Two integrated 10/100BASE-TX PHY transceivers, featuring the industry's lowest power consumption
- Full-featured QoS support
- Flexible management options that support common standard interfaces

A robust assortment of power management features including energy-efficient Ethernet (EEE) have been designed in to satisfy energy-efficient environments.

FIGURE 1-1: KSZ8852 TOP LEVEL ARCHITECTURE

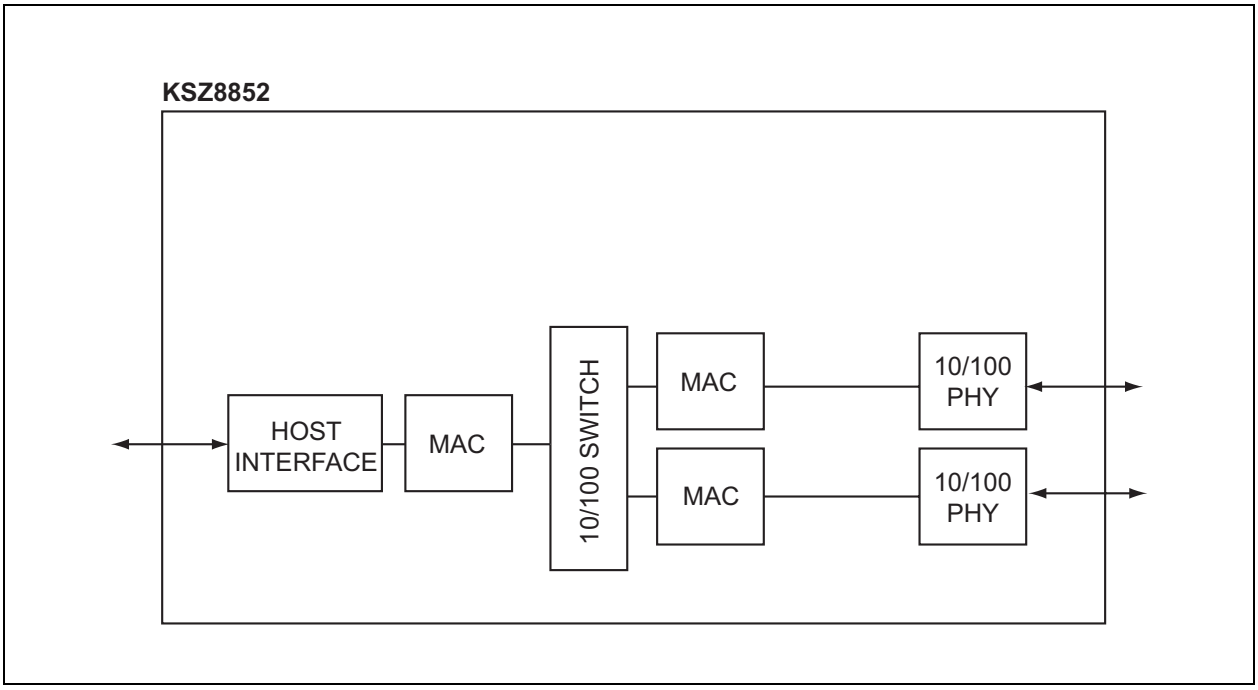
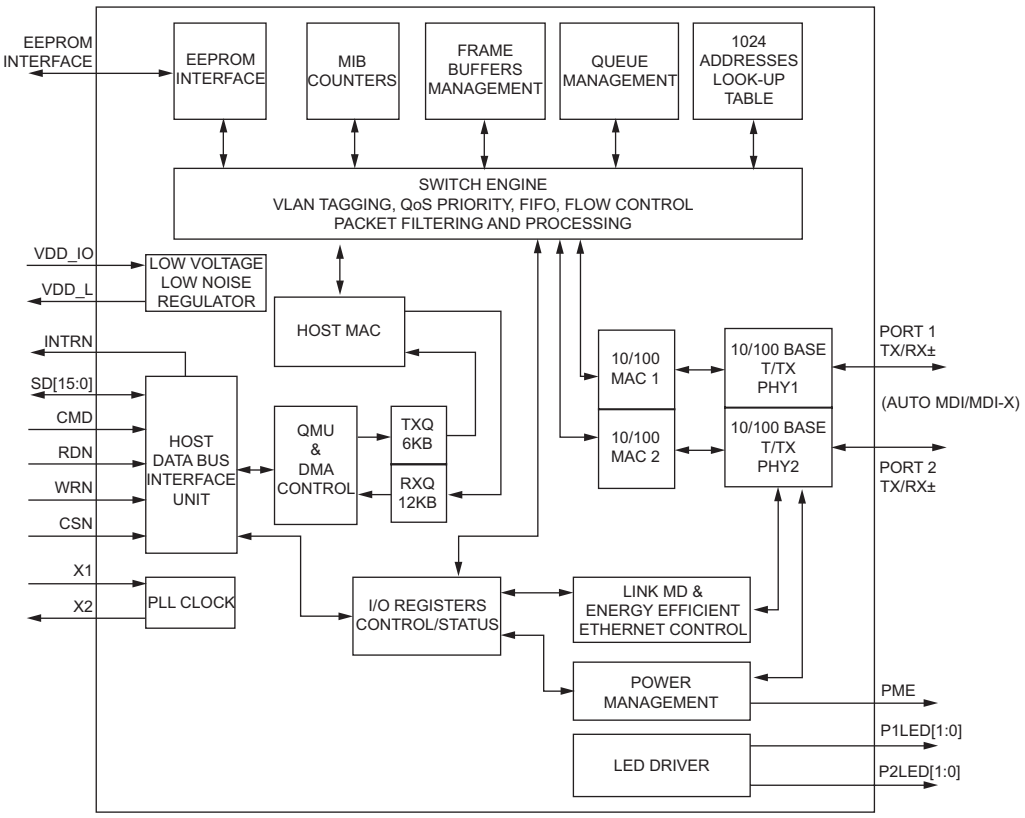


FIGURE 1-2: KSZ8852 FUNCTIONAL DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

FIGURE 2-1: 64-PIN LQFP ASSIGNMENT, (TOP VIEW)

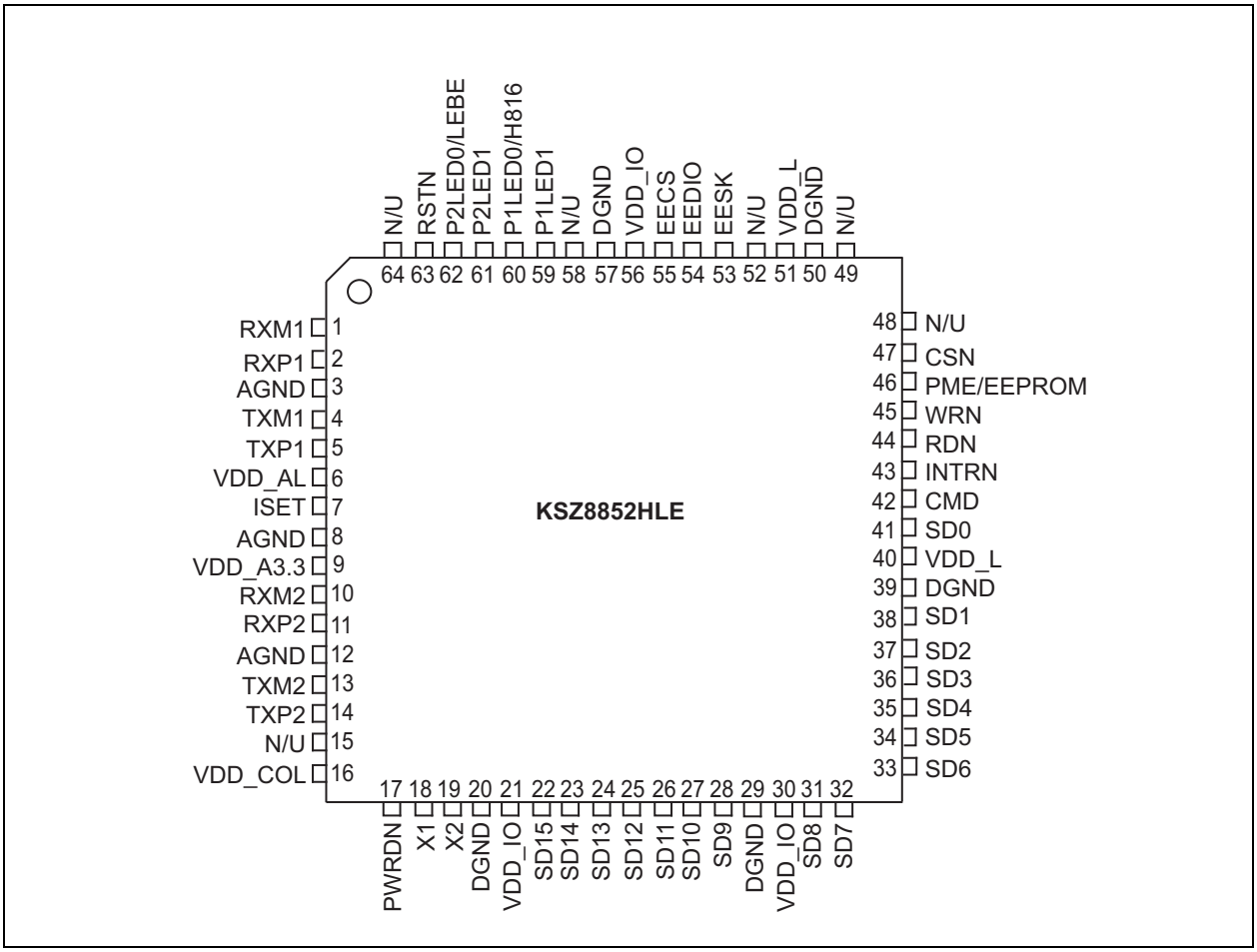


TABLE 2-1: SIGNALS FOR KSZ8852HLE

Pin Number	Pin Name	Type	Description
1	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential).
2	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
3	AGND	GND	Analog ground.
4	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential).
5	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential).
6	VDD_AL	P	This pin is used as an input for the low voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
7	ISET	O	**Current Set** Sets the physical transmit output current. Pull down this pin with a 6.49 kΩ (1%) resistor to ground.
8	AGND	GND	Analog ground.
9	VDD_A3.3	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
10	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (– differential).
11	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	AGND	GND	Analog ground.
13	TXM2	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential).
14	TXP2	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential).
15	N/U	I	This unused input should be connected to GND.
16	VDD-COL	P	This pin is used as a second input for the low voltage analog power. Its source should have appropriate filtering with a ferrite bead and capacitors.
17	PWRDN	IPU	**Full Chip Power-Down** Active-Low (Low = power down; High or floating = normal operation). While this pin is asserted low, all I/O pins will be tri-stated. All registers will be set to their default state. While this pin is asserted, power consumption will be minimal. When the pin is de-asserted power consumption will climb to nominal and the device will be in the same state as having been reset by the reset pin (RSTN, pin 63).
18	X1	I	**25 MHz Crystal or Oscillator Clock Connection** Pins (X1, X2) connect to a crystal or frequency oscillator source. If an oscillator is used, X1 connects to a VDD_IO voltage tolerant oscillator and X2 is a no connect. This clock requirement is ±50 ppm.
19	X2	O	
20	DGND	GND	Digital ground.
21	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power pin for IO logic and the internal Low Voltage regulator.
22	SD15/BE3	I/O (PD)	**Shared Data Bus Bit[15] or BE3** This is data bit (D15) access when CMD = “0”. This is Byte Enable 3 (BE3, 4th byte enable and active-high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.

TABLE 2-1: SIGNALS FOR KSZ8852HLE (CONTINUED)

Pin Number	Pin Name	Type	Description
23	SD14/BE2	I/O (PD)	**Shared Data Bus Bit [14] or BE2** This is data bit (D14) access when CMD = “0”. This is Byte Enable 2 (BE2, 3rd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
24	SD13/BE1	I/O (PD)	**Shared Data Bus Bit [13] or BE1** This is data bit (D13) access when CMD = “0”. This is Byte Enable 1 (BE1, 2nd byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
25	SD12/BE0	I/O (PD)	**Shared Data Bus Bit [12] or BE0** This is data bit (D12) access when CMD = “0”. This is Byte Enable 0 (BE0, 1st byte enable and active high) at double-word boundary access in 16-bit bus mode when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
26	SD11	I/O (PD)	**Shared Data Bus Bit [11]** This is data bit (D11) access when CMD = “0”. Don’t care when CMD = “1”. This pin must be tied to GND in 8-bit bus mode.
27	SD10/A10	I/O (PD)	**Shared Data Bus bit [10]** This is data bit (D10) access when CMD = “0”. In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A10 access when CMD = “1”.
28	SD9/A9	I/O (PD)	**Shared Data Bus Bit[9] or A9** This is data bit (D9) access when CMD = “0”. In 8−bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A9 access when CMD = “1”.
29	DGND	GND	Digital ground.
30	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power pin for IO logic and the internal low voltage regulator.
31	SD8/A8	IPU/O	**Shared Data Bus Bit [8] or A8** This is data bit (D8) access when CMD = “0”. In 8-bit bus mode, this pin must be tied to GND. In 16-bit bus mode, this is address A8 access when CMD = “1”.
32	SD7/A7	IPU/O	**Shared Data Bus Bit [7] or A7** This is data bit (D7) access when CMD = “0”. In 8-bit bus mode, this is address A7 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A7 access when CMD = “1”.
33	SD6/A6	IPU/O	**Shared Data Bus Bit [6] or A6** This is data bit (D6) access when CMD = “0”. In 8-bit bus mode, this is address A6 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A6 access when CMD = “1”.
34	SD5/A5	IPU/O	**Shared Data Bus Bit [5] or A5** This is data bit (D5) access when CMD = “0”. In 8-bit bus mode, this is address A5 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A5 access when CMD = “1”.

TABLE 2-1: SIGNALS FOR KSZ8852HLE (CONTINUED)

Pin Number	Pin Name	Type	Description
35	SD4/A4	IPU/O	**Shared Data Bus Bit [4] or A4** This is data bit (D4) access when CMD = “0”. In 8-bit bus mode, this is address A4 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A4 access when CMD = “1”.
36	SD3/A3	I/O (PD)	**Shared Data Bus Bit [3] or A3** This is data bit (D3) access when CMD = “0”. In 8-bit bus mode, this is address A3 (1st write) or Don’t care (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A3 access when CMD = “1”.
37	SD2/A2	I/O (PD)	**Shared Data Bus Bit [2] or A2** This is data bit (D2) access when CMD = “0”. In 8-bit bus mode, this is address A2 (1st write) or A10 (2nd write) access when CMD = “1”. In 16-bit bus mode, this is address A2 access when CMD = “1”.
38	SD1/A1/A9	I/O (PD)	**Shared Data Bus Bit [1] or A1 or A9** This is data bit (D1) access when CMD = “0”. In 8-bit bus mode, this is address A1 (1st write) or A9 (2nd write) access when CMD = “1”. In 16-bit bus mode, this is “Don’t care” when CMD = “1”.
39	DGND	GND	Digital ground.
40	VDD_L	P	This pin can be used in two ways: as the pin to input a low voltage to the device if the internal low voltage regulator is not used, or as the low voltage output if the internal low voltage regulator is used.
41	SD0/A0/A8	IPU/O	Shared Data Bus Bit [0] or A0 or A8 This is data bit (D0) access when CMD = “0”. In 8-bit bus mode, this is address A0 (1st write) or A8 (2nd write) access when CMD = “1”. In 16-bit bus mode, this is “Don’t care” when CMD = “1”.
42	CMD	IPD	**Command Type** This command input decides the SD[15:0] shared data bus access information. When command input is low, the access of shared data bus is for data access either SD[15:0] −> DATA[15:0] in 16−bit bus mode or SD[7:0] −> DATA[7:0] in 8-bit bus mode. When command input is high, in 16-bit bus mode: The access of shared data bus is for address A[10:2] access at shared data bus SD[10:2] and SD[1:0] is “don’t care". Byte enable BE[3:0] at SD[15:12] and the SD[11] is “don’t care”. in 8-bit bus mode: It is for address A[7:0] during 1st write access at shared data bus SD[7:0] or A[10:8] during 2nd write access at shared data bus SD[2:0] (SD[7:3] is don’t care).
43	INTRN	OPU	**Interrupt Output** This is an active-low signal going to the host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7 kΩ pull-up resistor.
44	RDN	IPU	**Read Strobe** This signal is an active-low signal used as the asynchronous read strobe during read access cycles by the host processor. It is recommended that it be pulled up with a 4.7 kΩ resistor.
45	WRN	IPU	**Write Strobe** This is an asynchronous write strobe signal used during write cycles from the external host processor. It is a low active signal.

TABLE 2-1: SIGNALS FOR KSZ8852HLE (CONTINUED)

Pin Number	Pin Name	Type	Description
46	PME/ EEPROM	IPD/O	**Power Management Event** This output signal indicates that a Wake On LAN event has been detected. The KSZ8852 is requesting the system to wake up from low power mode. Its assertion polarity is programmable with the default polarity to be active- low. **Config Mode: (EEPROM)** At the end of the power up/reset period, this pin is sampled and the pull-up/ pull-down value is latched. The value latched will indicate if a Serial EEPROM is present or not. See Table 2-2 for details.
47	CSN	IPU	**Chip Select** This signal is the Chip Select signal that is used by the external host processor for accesses to the device. It is an active-low signal.
48	N/U	O(PU)	This unused output should be unconnected.
49	N/U	O(PU)	This unused output should be unconnected.
50	DGND	GND	Digital ground.
51	VDD_L	P	This pin can be used in two ways; as the pin to input a low voltage to the device if the internal low voltage regulator is not used, or as the low voltage output if the internal low voltage regulator is used.
52	N/U	N/U	This unused output should be unconnected.
53	EESK	O(PD)	EEPROM Serial Clock Output A serial output clock is used to load configuration data into the KSZ8852 from the external EEPROM when it is present.
54	EEDIO	I/O (PD)	EEPROM Data Input/Output Serial data input/output is from/to external EEPROM when it is present.
55	EECS	O (PD)	EEPROM Chip Select Output This signal is used to select an external EEPROM device when it is present.
56	VDD_IO	P	3.3V, 2.5V, or 1.8V digital V_{DD} input power pin for IO logic and the internal Low Voltage regulator.
57	DGND	GND	Digital ground.
58	N/U	O(PU)	This unused output should be unconnected.

TABLE 2-1: SIGNALS FOR KSZ8852HLE (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>59</td><td>P1LED1</td><td>IPU/O</td><td>Programmable LED Outputs to Indicate Port 1 and Port 2 Activity/ Status
The LED is ON (active) when output is LOW; the LED is OFF (inactive) when output is HIGH.
The Port 1 LED pins outputs are determined by the table below if Reg. 0x06C – 0x06D, bits [14:12] are set to ‘000’. Otherwise, the Port 1 LED pins are controlled via the processor by setting Reg. 0x06C – 0x06D, bits [14:12] to a non-zero value.
The Port 2 LED pins outputs are determined by the table below if Reg. 0x084 – 0x085, bits [14:12] are set to ‘000’. Otherwise, the Port 2 LED pins are controlled via the processor by setting Reg. 0x084 – 0x085, bits [14:12] to a non-zero value.
Automatic Port 1 and Port 2 indicators are defined as follows:</td></tr>
<tr><td rowspan="4">60</td><td rowspan="4">P1LED0/ H816</td><td rowspan="4">IPU/O</td><td>Two bits [9:8] in SGCR7 Control Register
<table><tr><td>—</td><td>00 (Default)</td><td>01</td><td>10</td><td>11</td></tr><tr><td>P1LED1/P2LED1</td><td>Speed</td><td>ACT</td><td>Duplex</td><td>Duplex</td></tr><tr><td>P1LED0/P2LED0</td><td>LINK/ACT</td><td>LINK</td><td>LINK/ACT</td><td>LINK</td></tr></table></td></tr>
<tr><td>61</td><td>P2LED1</td><td>O</td><td rowspan="2">LINK = LED ON; ACT = LED Blink; LINK/ACT = LED On/Blink: Spped = LED ON (100BT); LED OFF = (10BT); Duplex = LED ON (Full duplex) and LED OFF = Half duplex)
Config Mode: (P1LED1)
At the end of the power up/reset period, this pin is sampled and the pull-up/ pull-down value is latched. It must be at a logic high level at this time. See the Strapping Options section for details.
Config Mode: (P1LED0/H816)
At the end of the power up/reset period, this pin is sampled and the pull-up/ pull-down value is latched. The value latched will determine if 8-bit or 16-bit mode will be used for the host interface. See Table 2-2 for details.
Config Mode: (P2LED0/LEBE)
At the end of the power up/reset period, this pin is sampled and the pull-up/ pull-down value is latched. The value latched will determine if “Little Endian” or “Big Endian” mode will be used for the host interface. See Table 2-2 for details.</td></tr>
<tr><td>62</td><td>P2LED0/ LEBE</td><td>IPU/O</td></tr>
<tr><td>63</td><td>RSTN</td><td>IPU</td><td>Reset
Hardware reset pin (Active-Low). This reset input is required to be low for a minimum of 10 ms after supply voltages VDD_IO and 3.3V are stable.</td></tr>
<tr><td>64</td><td>N/U</td><td>I</td><td>This unused input should be connected to GND.</td></tr>
<tr><td>65 (Bottom Pad)</td><td>GND</td><td>GND</td><td>Ground.</td></tr>
</table>

Note 2-1 P = power supply; GND = ground;
I = input; O = output; I/O = bi-directional;
IPU/O = Input with internal pull-up (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPD/O = Input with internal pull-down (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPU = Input with internal pull-up. (58 kΩ ±30%)
IPD = Input with internal pull-down. (58 kΩ ±30%)
OPU = Output with internal pull-up. (58 kΩ ±30%)
OPD = Output with internal pull-down. (58 kΩ ±30%)

I/O (PD) = Bi-directional input/output with internal pull-down. (58 kΩ ±30%)
I/O (PU) = Bi-directional Input/Output with internal pull-up. (58 kΩ ±30%)

TABLE 2-2: STRAPPING OPTIONS

Pin Number	Pin Name	Type Note 2-1	Description
46	PME/EEPROM	IPD/O	**EEPROM Select** Pull-up = EEPROM present NC or pull-down (default) = EEPROM not present This pin value is latched into register CCR, bit [9] at the end of the Power-Up/Reset time.
59	P1LED1	IPU/O	**Reserved** NC or pull-up (default) = Normal Operation Pull-down = Reserved
60	P1LED0/H816	IPU/O	8 or 16-Bit Host Interface Mode Select NC or pull-up (default) = 16-bit bus mode Pull-down = 8-bit bus mode This pin value is also latched into register CCR, bit [7:6] at the end of the Power-Up/Reset time.
62	P2LED0/LEBE	IPU/O	**Endian Mode Select for 8/16-bit Host Interface** NC or pull-up (default) = Little Endian Pull-down = Big Endian This pin value is latched into register CCR, bit [10] at the end of the power-up/reset time.

Note 2-1 IPD/O = Input with internal pull-down. (58 kΩ ±30%) during power-up/reset; output pin otherwise.
IPD/O = Input with internal pull-down. (58 kΩ ±30%) during power-up/reset; output pin otherwise.

All strapping pins are latched during power-up or reset as well as re-strap-in when hardware/software power-down and hardware reset.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8852 is a highly integrated networking device that incorporates a Layer-2 switch, two 10BT/100BT physical layer transceivers (PHYs) and associated MAC units, and a bus interface unit (BIU) with one general 8/16-bit host interface.

The KSZ8852 operates in a managed mode. In managed mode, a host processor can access and control all PHY, Switch, and MAC related registers within the device via the host interface.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption. Both power management and Energy Efficient Ethernet (EEE) are designed to save more power while device is in idle state. Wake on LAN is implemented to allow the KSZ8852 to monitor the network for packets intended to wake up the system which is upstream from the KSZ8852.

The KSZ8852 is fully compliant to IEEE802.3u standards.

3.1 Direction Terminology

Readers should note that two different terminologies are used in this data sheet to describe the direction of data flow. In the standard terminology that is used for all switches, directions are described from the point of view of the switch core: “transmit” indicates data flow out of the KSZ8852 on any of the three ports, while “receive” indicates data flow into the KSZ8852. This terminology is used for the MIB counters.

When referencing the QMU block, which is located on port 3 between the internal MAC and the external 8/16-bit host interface, directions are revered. They are described from the point of view of the external host processor. “Transmit” indicates data flow from the host into port 3 of the KSZ8852, while “receive” indicates data flow out of the KSZ8852 on port 3. Since both terminologies are used for port 3, it is important to note whether or not a particular section refers to the QMU.

3.2 Physical (PHY) Block

There is a full chip power-down mode if PWRDN (pin 36) is tied to low. When this pin is pulled-down, the entire chip powers down. Transitioning this pin from pull-down to pull-up results in a power up and chip reset. The reset will set all registers to default values. The host CPU will need to re-program all register values again after release of the PWRDN.

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. An external 6.49 kΩ (1%) resistor for the 1:1 transformer ratio sets the output current.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.2.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then, the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.4 PLL CLOCK SYNTHESIZER (RECOVERY)

The internal PLL clock synthesizer generates 125 MHz, 62.5 MHz, and 31.25 MHz clocks for the KSZ8852 system timing. These internal clocks are generated from an external 25 MHz crystal or oscillator.

3.2.5 100BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnets. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function.

The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP1 or RXM1 input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8852 decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.3 MDI/MDI−X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8852 supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns these transmit and receive pairs for the KSZ8852 device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers. The IEEE 802.3u standard MDI and MDI-X definitions are as below:

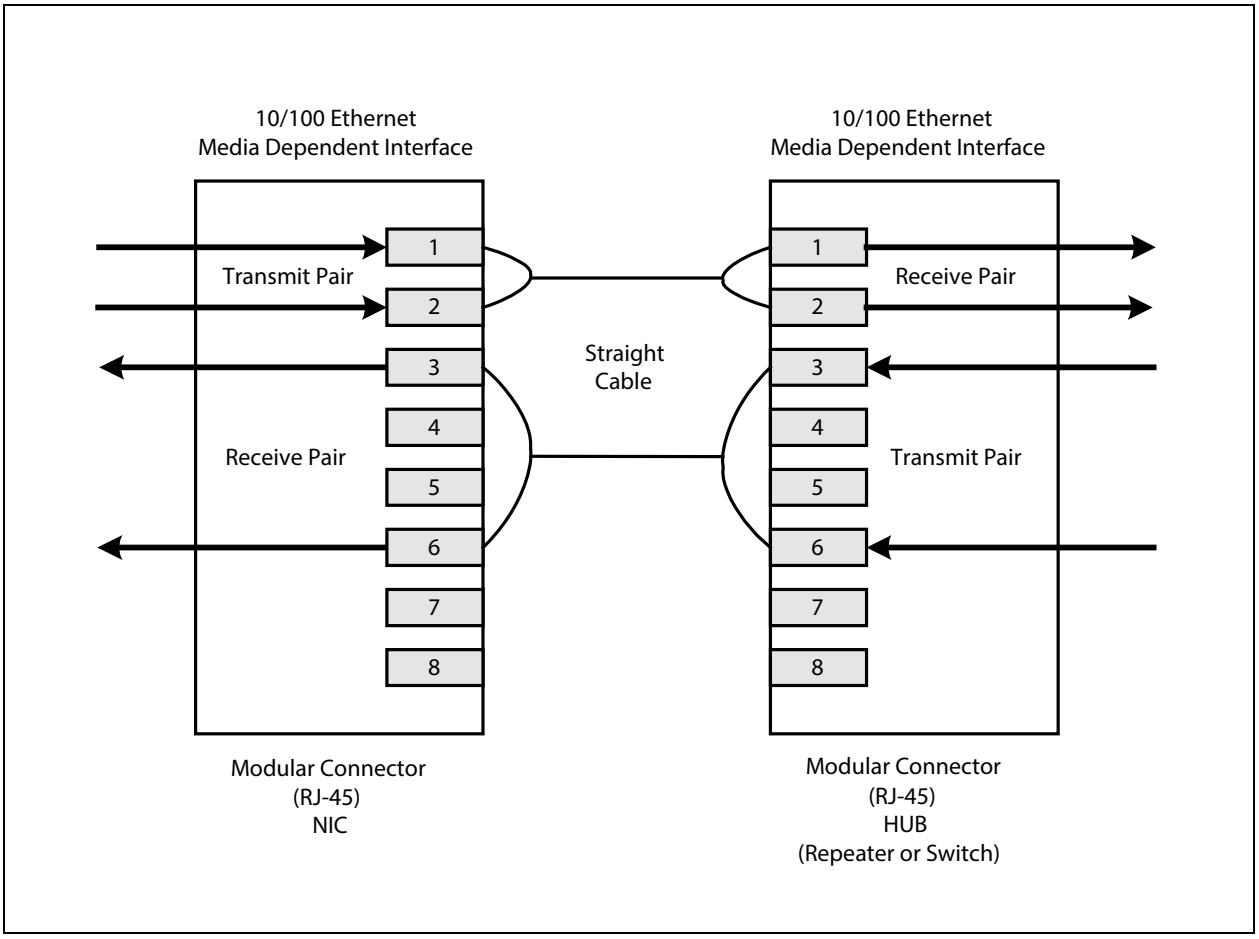
TABLE 3-1: MDI/MDI-X PIN DEFINITION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.3.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device or an MDI-X device to an MDI device. Figure 3-1 shows a typical straight cable connection between a network interface card (NIC) and a switch, or hub (MDI-X).

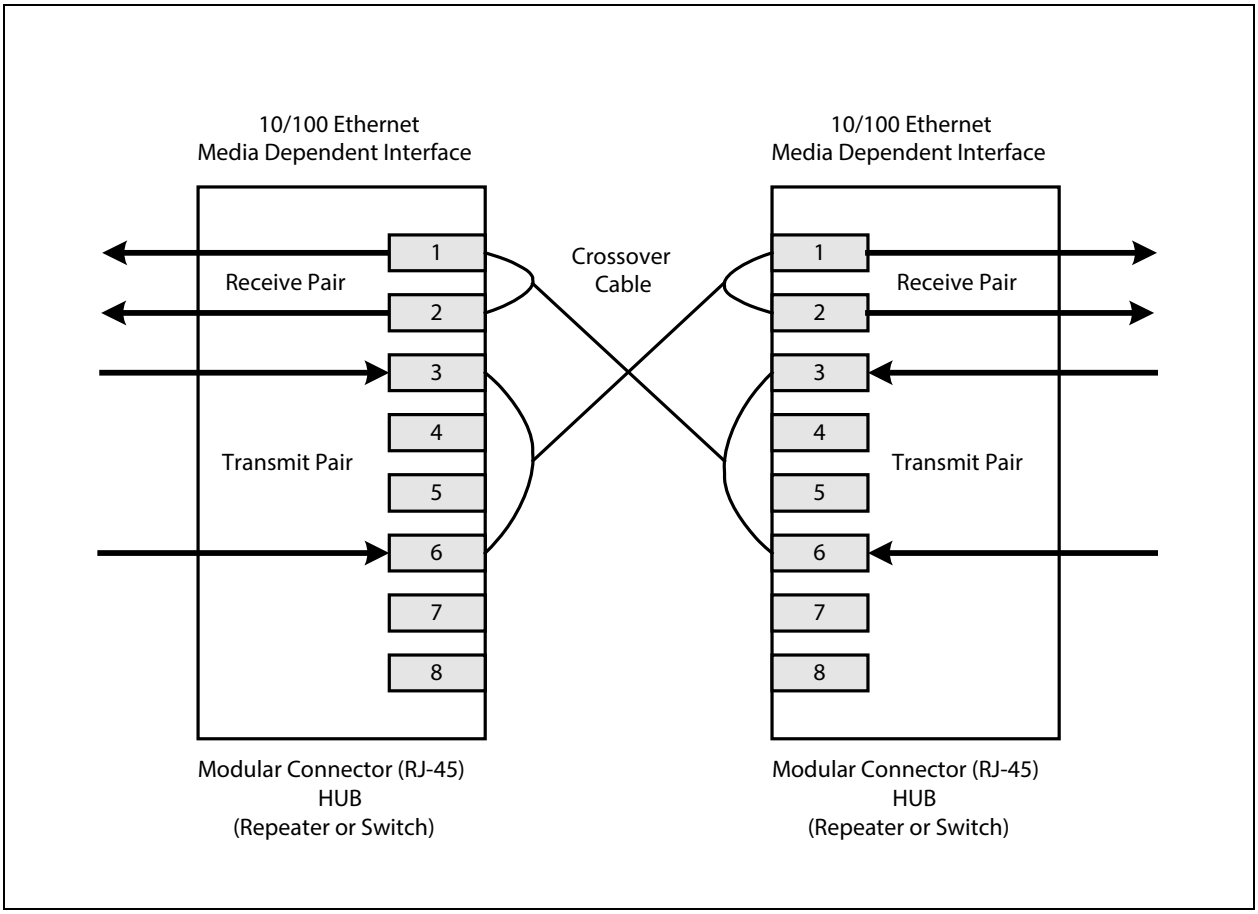
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.3.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two chips or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



3.4 Auto Negotiation

The KSZ8852 conforms to the auto-negotiation protocol as described by IEEE 802.3. It allows each port to operate at either 10BASE-T or 100BASE-TX. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto-negotiation, the link partners advertise capabilities across the link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is also used to negotiate support for Energy Efficient Ethernet (EEE).

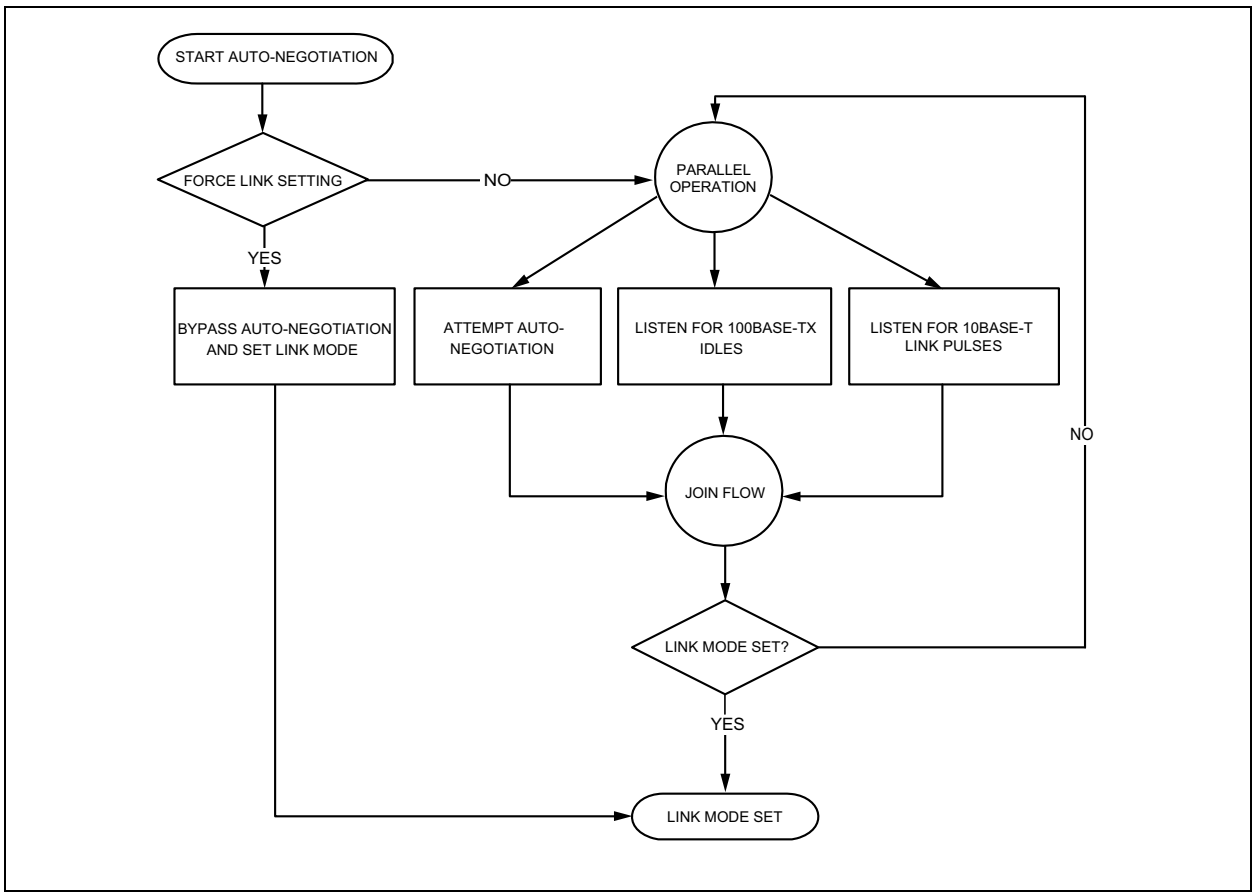
The following list shows the speed and duplex operation mode from highest to lowest.

- Highest: 100BASE-TX, full-duplex
- High: 100BASE-TX, half-duplex
- Low: 10BASE-T, full-duplex
- Lowest: 10BASE-T, half-duplex

If Auto-negotiation is not supported or the link partner to the KSZ8852 is forced to bypass auto-negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup is shown in the Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.5 LINK MD® Cable Diagnostics

The KSZ8852 LINK MD® uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LINK MD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format in register P1SCSLMD[8:0] or P2SCSLMD[8:0].

3.5.1 ACCESS

LINK MD is initiated by accessing register P1SCSLMD (0x07C) or P2SCSLMD (0x094), the PHY special control/status, and LINK MD register.

3.5.2 USAGE

Before initiating LINK MD the value 0x8008 must be written to the ANA_CNTRL_3 Register (0x74C – 0x74D). This needs to be done once (after power-on reset), but does not need to be repeated for each initiation of
LINK MD. Auto-MDIX must also be disabled before using LINK MD. To disable Auto-MDIX, write a ‘1’ to P1CR4[10] or P2CR4[10] to enable manual control over the pair used to transmit the LINK MD pulse. The self-clearing cable diagnostic test enable bit, P1SCSLMD[12] or P2SCSLMD[12], is set to ‘1’ to start the test on this pair.

When bit P1SCSLMD[12] or P2SCSLMD[12] returns to ‘0’, the test is completed. The test result is returned in bits P1SCSLMD[14:13] or P2SCSLMD[14:13] and the distance is returned in bits P1SCSLMD[8:0] or P2SCSLMD[8:0]. The cable diagnostic test results are as follows:

- 00 = Valid test, normal condition
- 01 = Valid test, open circuit in cable

- 10 = Valid test, short-circuit in cable
- 11 = Invalid test, LINK MD® failed

If P1SCLMD[14:13]=11, this indicates an invalid test, and occurs when the KSZ8852 is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8852 to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by utilizing the following formula:

- P1SCSLMD[8:0] x 0.4m for port 1 cable distance
- P2SCSLMD[8:0] x 0.4m for Port 2 cable distance

This constant (0.4m) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.6 On-Chip Termination Resistors

The KSZ8852 reduces board cost and simplifies board layout by using on-chip termination resistors for RX/TX differential pairs, eliminating the need for external termination resistors. The on-chip termination and internal biasing will provide significant power savings when compared with using external biasing and termination resistors.

3.7 Lookback Support

The KSZ8852 provides two loopback modes. One is Near-End (Remote) Loopback to support remote diagnosing of failures on line side, and the other is Far-End loopback to support local diagnosing of failures through all blocks of the device. In loopback mode, the speed of the PHY port will be set to 100BASE-TX full-duplex mode.

3.7.1 FAR-END LOOPBACK

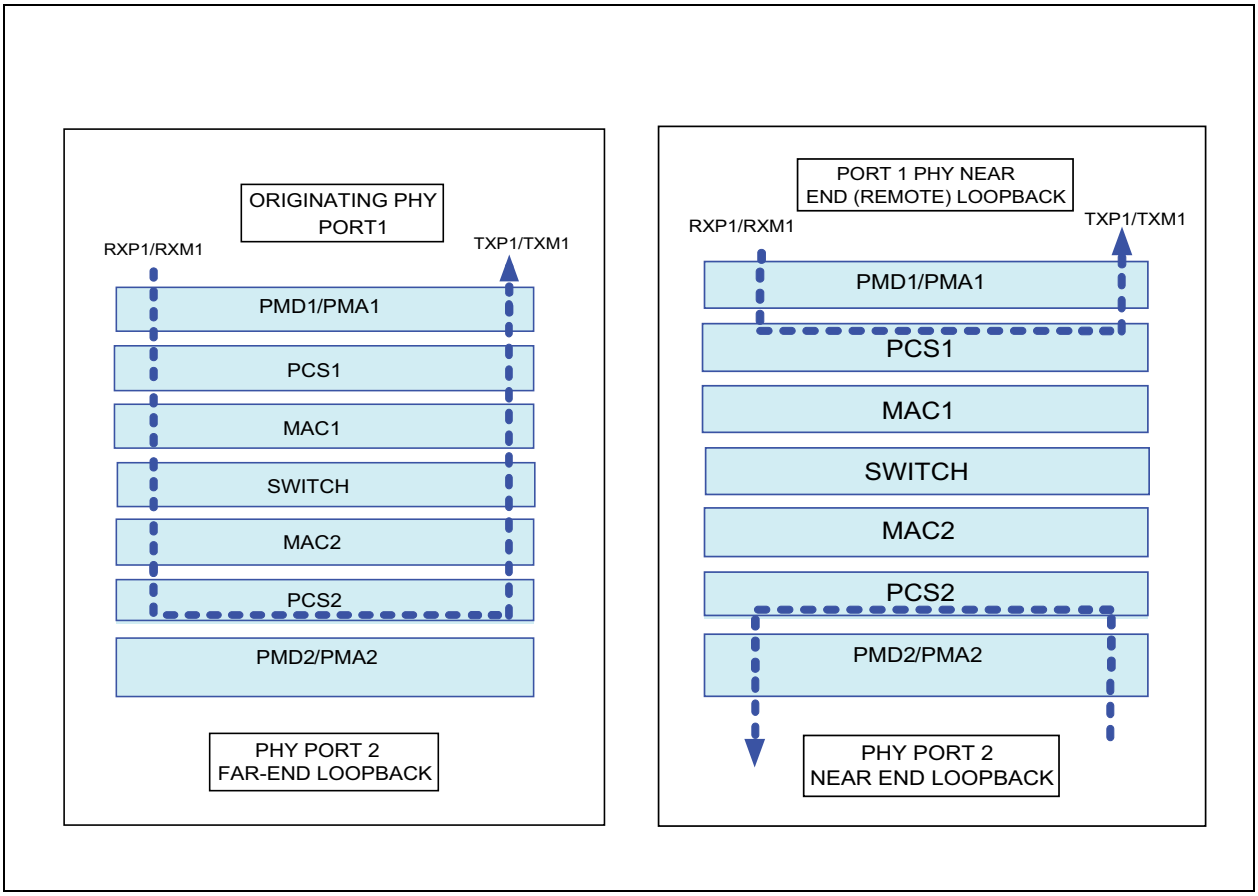
Far-end loopback is conducted between the KSZ8852's two PHY ports. The loopback path starts at the "Originating" PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PCS (Physical Coding Sublayer), and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit[8] of registers P1CR4 and P2CR4 is used to enable far-end loopback for Ports 1 and 2, respectively. As an alternative, Bit[14] of registers P1MBCR and P2MBCR can be used to enable far-end loopback. The Port 2 far-end loopback path is illustrated in Figure 3-4.

3.7.2 NEAR−END (REMOTE) LOOPBACK

Near-end (Remote) loopback is conducted at either PHY Port 1 or PHY Port 2 of the KSZ8852. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PCS, and ends at the same PHY port's transmit outputs (TXPx/TXMx). Bit[1] of registers P1PHYCTRL and P2PHYCTRL is used to enable near-end loopback for Ports 1 and 2, respectively. As an alternative, Bit[9] of registers P1SCSLMD and P2SCSLMD can be used to enable near-end loopback. The near-end loopback paths for Port 1 and Port 2 are illustrated in Figure 3-4.

FIGURE 3-4: NEAR-END AND FAR-END LOOPBACK



3.8 MAC (Media Access Controller) Block

3.8.1 MAC OPERATION

The KSZ8852 strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter unicast packets. The MAC filtering function is useful in applications such as VoIP where restricting certain packets reduces congestion and thus improves performance.

3.8.2 ADDRESS LOOKUP

The internal dynamic MAC address lookup table stores MAC addresses and their associated information. It contains a 1K entry unicast address learning table plus switching information.

The KSZ8852 is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending upon the operating environment and probabilities, may not guarantee the absolute number of addresses they can learn.

3.8.3 LEARNING

The internal lookup engine updates the dynamic MAC address table with a new entry if the following conditions are met:

- The received packet's Source Address (SA) does not exist in the lookup table.
- The received packet has no receiving errors, and the packet size is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the oldest entry of the table is deleted to make room for the new entry.

3.8.4 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the dynamic table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet has no receiving errors, and the packet size is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

3.8.5 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 300 seconds, ±75 seconds. This feature can be enabled or disabled through global register SGCR1[10].

3.8.6 FORWARDING

The KSZ8852 forwards packets using the algorithm that is depicted in the following flowcharts. Figure 3-5 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 3-6. The packet is sent to PTF2.

The KSZ8852 will not forward the following packets:

- Error packets: These include framing errors, frame check sequence (FCS) errors, alignment errors, and illegal size packet errors.
- IEEE802.3x PAUSE frames: KSZ8852 intercepts these packets and performs full duplex flow control accordingly.
- “Local” packets: Based on destination address (DA) lookup. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as “local.”

FIGURE 3-5: DESTINATION ADDRESS LOOKUP FLOW CHART IN STAGE ONE

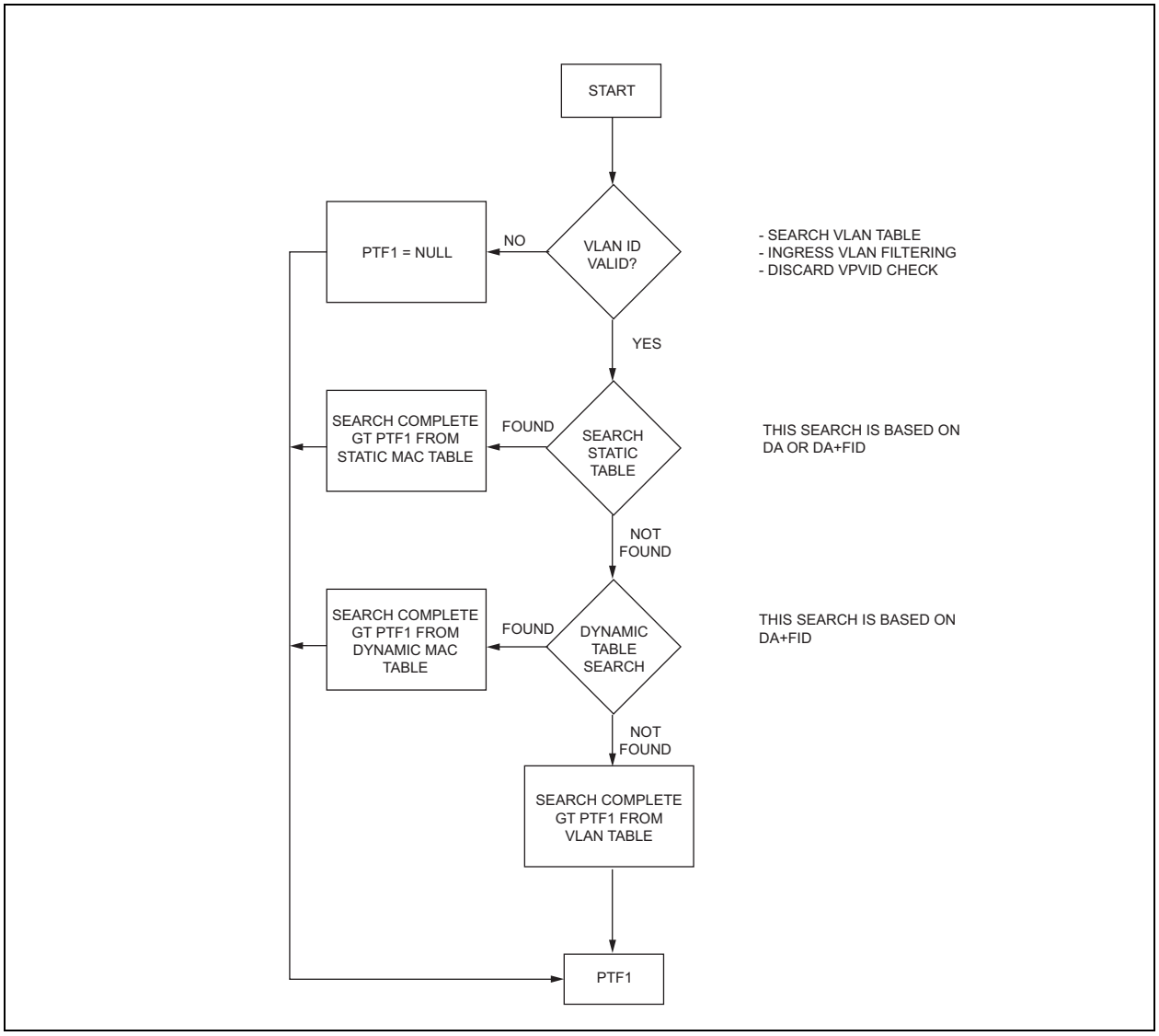
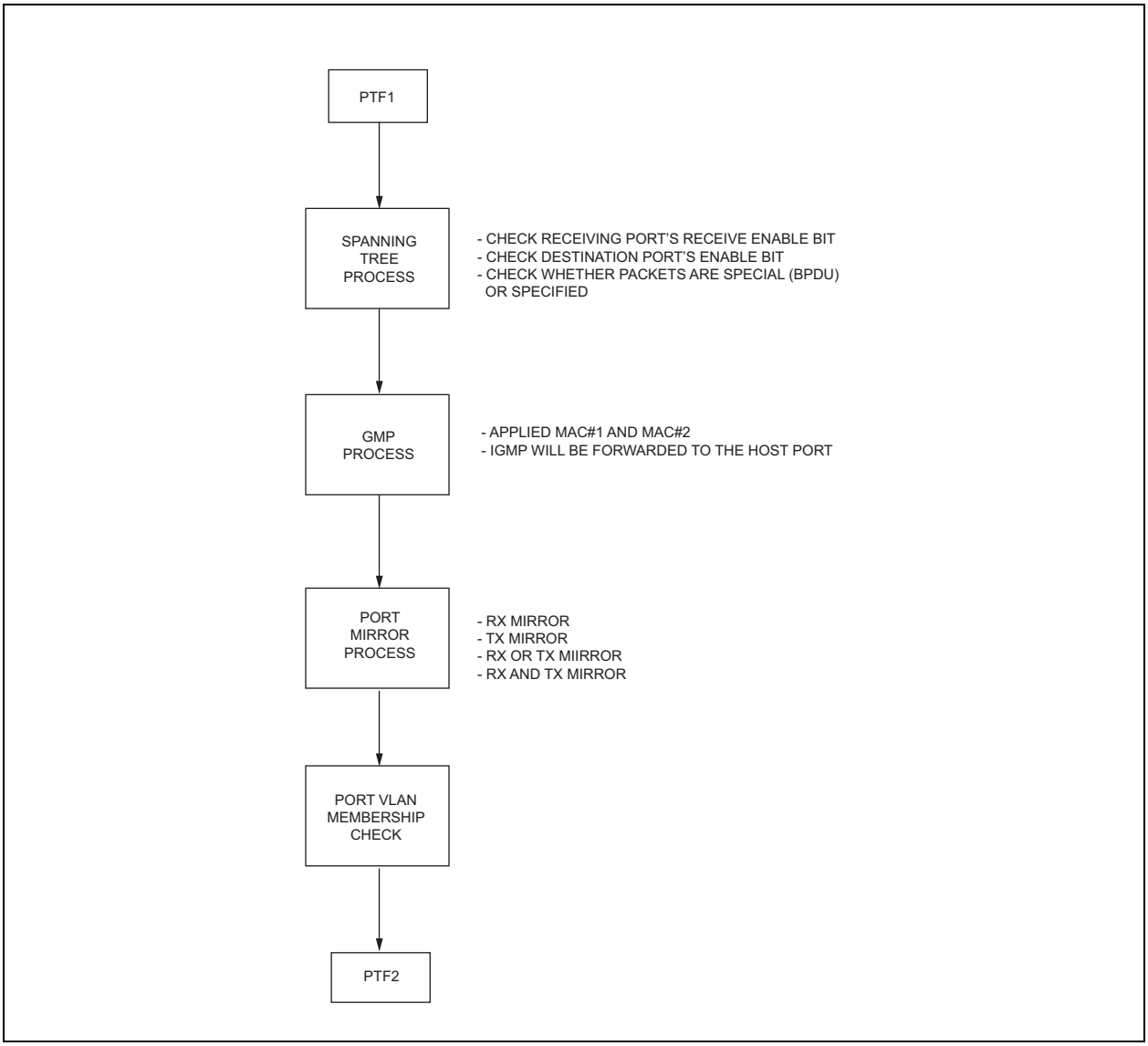


FIGURE 3-6: DESTINATION ADDRESS RESOLUTION FLOW CHART IN STAGE TWO



3.8.7 INTER PACKET GAP (IPG)

If a frame is successfully transmitted, then the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.8.8 BACK-OFF ALGORITHM

The KSZ8852 implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode. After 16 collisions, the packet is dropped.

3.8.9 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, the packet is dropped.

3.8.10 LEGAL PACKET SIZE

The KSZ8852 discards packets less than 64 bytes and can be programmed to accept packet sizes up to 1536 bytes in SGCR2[1]. The KSZ8852 can also be programmed for special applications to accept packet sizes up to 2000 bytes in SGCR1[4].

3.8.11 FLOW CONTROL

The KSZ8852 supports standard 802.3x flow control frames on both transmit and receive sides. In the receive direction, if a PAUSE control frame is received on any port, the KSZ8852 will not transmit the next normal frame on that port until the timer, specified in the PAUSE control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second PAUSE frame. During this flow controlled period, only flow control packets from the KSZ8852 are transmitted.

In the transmit direction, the KSZ8852 has intelligent and efficient ways to determine when to invoke flow control and send PAUSE frames. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8852 issues a PAUSE frame containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8852 then sends out another flow control frame with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

On Port 3, a flow control handshake exists internally between the QMU and the port 3 MAC. In the QMU, there are three programmable threshold levels for flow control in the RXQ FIFO: 1) low water mark register FCLWR (0x1B0), 2) high water mark register FCHWR (0x1B2) and 3) overrun water mark register FCOWR (0x1B4). The QMU will send a PAUSE frame internally to the MAC when the RXQ buffer fills with egress packets above the high water mark level (default 3.072 Kbytes available). It sends a stop PAUSE frame when the RXQ buffer drops below the low water mark level (default 5.12 Kbytes available). The QMU will drop new packets from the switch when the RXQ buffer fills beyond the overrun water mark level (default 256 bytes available).

3.8.12 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (non-IEEE 802.3 standard) is also provided. The activation and deactivation conditions are the same as in full-duplex mode. If backpressure is required, the KSZ8852 sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8852 discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, carrier sense type backpressure is reactivated again until chip resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collision and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex mode, the user must enable the following bits:

- Aggressive back off (bit[8] in SGCR1)
- No excessive collision drop (bit[3] in SGCR2)
- Backpressure flow control enable (bit[11] in P1CR2/P2CR2)

These bits are not set in default, since this is not the IEEE standard.

3.8.13 BROADCAST STORM PROTECTION

The KSZ8852 has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8852 has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be enabled or disabled on a per port basis in P1CR1[7] and P2CR1[7]. The rate is based on a 67 ms interval for 100BT and a 670 ms interval for 10 BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in SGCR3[2:0][15:8]. The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec × 67 ms/interval X 1% = 99 frames/interval (approx.) = 0x63

148,800 frames/sec is based on 64-byte block of packets in 100BASE−T with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.8.14 PORT INDIVIDUAL MAC ADDRESS AND SOURCE PORT FILTERING

The KSZ8852 can provide individual MAC addresses for port 1 and port 2. They can be set at registers 0x0B0h - 0x0B5h and 0x0B6 - 0x0BB. Received packets can be filtered (dropped) if their source address matches the MAC address of port 1 or port 2. This feature can be enabled by setting bits [11:10] in the P1CR1 or P2CR1 registers. One example of usage is that a packet will be dropped after it completes a full round trip within a ring network.

3.8.15 ADDRESS FILTERING FUNCTION

The KSZ8852 supports 11 different address filtering schemes as shown in Table 3-2. The Ethernet destination address (DA) field inside the packet is the first 6-byte field which uses to compare with either the host MAC address registers (0x110 - 0x115) or the MAC address hash table registers (0x1A0 – 0x1A7) for address filtering operation. The first bit (bit[40]) of the destination address (DA) in the Ethernet packet decides whether this is a physical address if bit[40] is “0” or a multicast address if bit[40] is “1”.

TABLE 3-2: MAC ADDRESS FILTERING SCHEME

Item	Address Filtering Mode	Receive Control Register (0x174 – 0x175): RXCR1				Description
		RX ALL (Bit [4])	RX Inverse (Bit [1])	RX Physical Address (Bit [11])	RX Multicast Address (Bit [8])	
1	Perfect	0	0	1	1	All Rx frames are passed only if the DA exactly matches the MAC Address in MARL, MARM and MARH registers.
2	Inverse Perfect	0	1	1	1	All Rx frames are passed if the DA is not matching the MAC Address in MARL, MARM, and MARH registers.
3	Hash Only	0	0	0	0	All Rx frames with either multicast or physical destination address are filtering against the MAC address hash table.
4	Inverse Hash Only	0	1	0	0	All Rx frames with either multicast or physical destination address are filtering not against the MAC address hash table. All Rx frames which are filtering out at item 3 (Hash only) only are passed in this mode.
5	Hash Perfect (Default)	0	0	1	0	All Rx frames are passed with physical address (DA) matching the MAC Address and to enable receive multicast frames that pass the hash table when Multicast address is matching the MAC address hash table.
6	Inverse Hash Perfect	0	1	1	0	All Rx frames which are filtering out at item 5 (hash perfect) only are passed in this mode.
7	Promiscuous	1	1	0	0	All Rx frames are passed without any conditions.
8	Hash Only with Multicast Address Passed	1	0	0	0	All Rx frames are passed with physical address (DA) matching the MAC Address hash table and with Multicast address without any conditions.
9	Perfect with Multicast Address Passed	1	0	1	1	All Rx frames are passed with physical address (DA) matching the MAC Address and with Multicast address without any conditions.
10	Hash Only with Physical Address Passed	1	0	1	0	All Rx frames are passed with Multicast address matching the MAC Address hash table and with physical address without any conditions.
11	Perfect with Physical Address Passed	1	0	0	1	All Rx frames are passed with Multicast address matching the MAC Address and with physical address without any conditions.

Bit [0] (RX Enable), Bit [5] (RX Unicast Enable) and Bit [6] (RX Multicast Enable) must be set to 1 in RXCR1 register.
The KSZ8852M will discard frame with SA same as the MAC Address if bit[0] is set in RXCR2 register.

3.9 Switch Block

3.9.1 SWITCHING ENGINE

The KSZ8852 features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. The switching engine has a 32 KByte internal frame buffer. This resource is shared between all the ports. There are a total of 256 buffers available. Each buffer is sized at 128 Bytes.

"Transmit = egress" applies to all three ports in the context of the switch core. This includes the MIB counters. It also applies to the TX priority queues (sometimes called TXQs) which are not to be confused with the TX queue (TXQ) in the QMU. This would generally include Registers 0x000 – 0x16B.

3.9.2 SPANNING TREE SUPPORT

To support spanning tree, the host port is the designated port for the processor. The other ports (Port 1 and Port 2) can be configured in one of the five spanning tree states via "transmit enable", "receive enable" and "learning disable" register settings in registers P1CR2 and P2CR2 for Ports 1 and 2, respectively. Table 3-3 shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-3: SPANNING TREE STATES

State	Port Setting	Software Action
Disable State: The port should not forward or receive any packets. Learning is disabled.	Transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the Static MAC Address Table with "overriding bit" set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State: Only packets to the processor are forwarded.	Transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should not send any packets to the port(s) in this state. The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State: Only packets to and from the processor are forwarded. Learning is disabled.	Transmit enable = "0", receive enable = "0", learning disable = "1"	The processor should program the Static MAC Address TableStatic MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.
Learning State: Only packets to and from the processor are forwarded. Learning is enabled.	Transmit enable = "0", receive enable = "0", learning disable = "0"	The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State Packets are forwarded and received normally. Learning is enabled.	Transmit enable = "1", receive enable = "1", learning disable = "0"	The processor programs the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The "overriding" bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

3.9.3 RAPID SPANNING TREE SUPPORT

There are three operational states assigned to each port for RSTP (Discarding, Learning, and Forwarding):

- Discarding ports do not participate in the active topology and do not learn MAC addresses.
- Discarding state: the state includes three states of the disable, blocking and listening of STP.
- Port setting: Transmit enable = “0”, receive enable = “0”, learning disable = “1”.

3.9.3.1 Discarding State

Software action: The host processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. When the port’s learning capability (learning disable = ‘1’) is disabled, setting bits [10:9] in the SGCR8 register will rapidly flush the port related entries in the dynamic MAC table and static MAC table.

The processor is connected to Port 3 via the host interface. Address learning is disabled on the port in this state.

3.9.3.2 Learning State

Ports in “Learning States” learn MAC addresses, but do not forward user traffic.

Learning State: Only packets to and from the processor are forwarded. Learning is enabled.

Port setting for Learning State: transmit enable = “0”, receive enable = “0”, learning disable = “0”.

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state (see **Section 3.9.3.4 “Tail Tagging Mode”** section for details.) Address learning is enabled on the port in this state.

Ports in forwarding states fully participate in both data forwarding and MAC learning.

3.9.3.3 Forwarding State

Forwarding state: Packets are forwarded and received normally. Learning is enabled.

Port setting: transmit enable = “1”, receive enable = “1”, learning disable = “0”.

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see **Section 3.9.3.4 “Tail Tagging Mode”** section for details. Address learning is enabled on the port in this state.

RSTP uses only one type of BPDU called RSTP BPDUs. They are similar to STP Configuration BPDUs with the exception of a type field set to “version 2” for RSTP and “version 0” for STP, and a flag field carrying additional information.

3.9.3.4 Tail Tagging Mode

Tail tag mode is only seen and used by the Port 3 host interface, which should be connected to a processor. It is an effective way to retrieve the ingress port information for spanning tree protocol, IGMP snooping, and other applications. Bits [1:0] in the one byte tail tagging are used to indicate the source/destination port in Port 3. Bits [3:2] are used for priority setting of the ingress frame in Port 3. Other bits are not used. The tail tag feature is enabled by setting bit [8] in the SGCR8 register.

FIGURE 3-7: TAIL TAG FRAME FORMAT

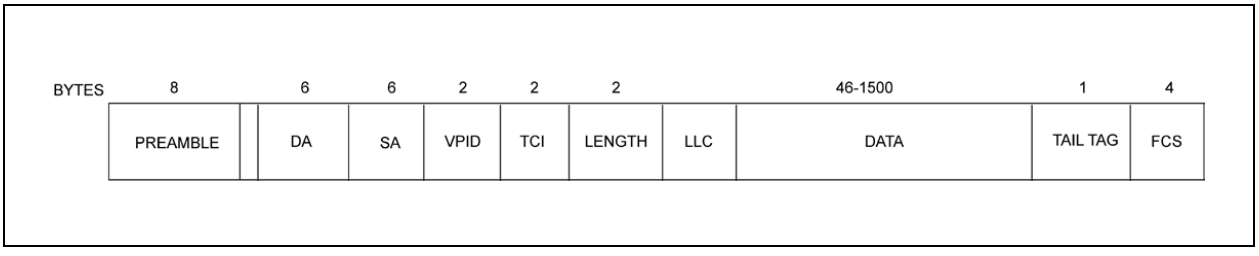


TABLE 3-4: TAIL TAG RULES

Ingress to Port 3 (Host −> KSZ8852)	
Bit [1:0]	**Destination Port**
00	Normal (Address Look up)
01	Port 1
10	Port 2
11	Port 1and Port 1
Bit [3:2]	**Frame Priority**
00	Priority 0
01	Priority 1
10	Priority 2
11	Priority 3
Egress from Port 3 (KSZ8852 −> Host)	
Bit [0]	Source Port
0	Port 1
1	Port 2

3.10 IGMP Support

For internet group management protocol (IGMP) support in Layer 2, the KSZ8852 provides two components:

3.10.1 “IGMP” SNOOPING

The KSZ8852 traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.10.2 “MULTICAST ADDRESS INSERTION” IN THE STATIC MAC TABLE

Once the multicast address is programmed in the Static MAC Address Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

To enable IGMP support, set bit[14] to ‘1’ in the SGCR2 register. Also, Tail Tagging Mode needs to be enabled, so that the processor knows which port the IGMP packet was received on. This is achieved by setting bit[8] to ‘1’ in the SGCR8 register.

3.11 IPv6 MLD Snooping

The KSZ8852 traps IPv6 multicast listener discovery (MLD) packets and forwards them only to the processor (host port). MLD snooping is controlled by SGCR2, bit[13] (MLD snooping enable) and SGCR2 bit[12] (MLD option).

Setting SGCR2 bit[13] causes the KSZ8852 to trap packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = “1”
- IPv6 next header = “1”or “58” (or = “0” with hop-by-hop next header = “1” or “58”)
- If SGCR2[12] = “1”, IPv6 next header = “43”, “44”, “50”, “51”, or “60” (or = “0” with hop−by−hop next header = “43”, “44”, “50”, “51”, or “60”)

3.12 Port Mirroring Support

KSZ8852 supports “Port Mirroring” comprehensively as illustrated in the following sub-sections:

3.12.1 “RECEIVE ONLY” MIRROR-ON-A-PORT

All the packets received on the port are mirrored on the sniffer port. For example, Port 1 is programmed to be “receive sniff” and the host port is programmed to be the “sniffer port”. A packet received on Port 1 is destined to Port 2 after the internal lookup. The KSZ8852 forwards the packet to both Port 2 and the host port. The KSZ8852 can optionally even forward “bad” received packets to the “sniffer port”.

3.12.2 “TRANSMIT ONLY” MIRROR-ON-A-PORT

All the packets transmitted on the port are mirrored on the sniffer port. For example, Port 1 is programmed to be “transmit sniff” and the host port is programmed to be the “sniffer port”. A packet received on Port 2 is destined to Port 1 after the internal lookup. The KSZ8852 forwards the packet to both Port 1 and the host port.

3.12.3 “RECEIVE AND TRANSMIT” MIRROR-ON-TWO-PORTS

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the “AND” feature, set register SGCR2, bit 8 to “1”. For example, Port 1 is programmed to be “receive sniff”, Port 2 is programmed to be “transmit sniff”, and the host port is programmed to be the “sniffer port”. A packet received on Port 1 is destined to Port 2 after the internal lookup. The KSZ8852 forwards the packet to both Port 2 and the host port.

Multiple ports can be selected as “receive sniff” or “transmit sniff”. In addition, any port can be selected as the “sniffer port”. All these per port features can be selected through registers P1CR2, P2CR2, and P3CR2 for Ports 1, 2, and the host port, respectively.

3.13 IEEE 802.1Q VLAN Support

The KSZ8852 supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8852 provides a 16-entry VLAN table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning (see Table 3-5 and Table 3-6).

Advanced VLAN features are also supported in the KSZ8852, such as “VLAN ingress filtering” and “discard non PVID” defined in bits [14:13] of P1CR2, P2CR2 and P3CR2 registers. These features can be controlled on per port basis.

TABLE 3-5: FID + DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table	Use FID Flag	FID Match	DA+FID Found in Dynamic MAC Table	Action
No	Don’t Care	Don’t Care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don’t Care	Don’t Care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don’t Care	Don’t Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don’t Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-6: FID + SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

3.14 QoS Priority Support

The KSZ8852 provides quality-of-service (QoS) for applications such as VoIP and video conferencing. The KSZ8852 offer 1, 2, and 4 priority queues option per port. This is controlled by bit[0] and bit[8] in P1CR1, P2CR1 and P3CR1 registers as shown below:

- Bit[0], Bit[8] = '00' Egress port is a single output queue as default.
- Bit[0], Bit[8] = '01' Egress port can be split into two priority transmit queues. (Q0 and Q1)
- Bit[0], Bit[8] = '10' Egress port can be split into four priority transmit queues. (Q0, Q1, Q2, and Q3)

The four priority transmit queues is a new feature in the KSZ8852. Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option for every port via bits[15,7] in the P1ITXQRCR1, P1TXQRCR2, P2TXQRCR1, P2TXQRCR2, P3TXQRCR1, and P3TXQRCR2 Registers to select either always to deliver high priority packets first or use weighted fair queuing for the four priority queues scale by 8:4:2:1.

3.14.1 PORT-BASED PRIORITY

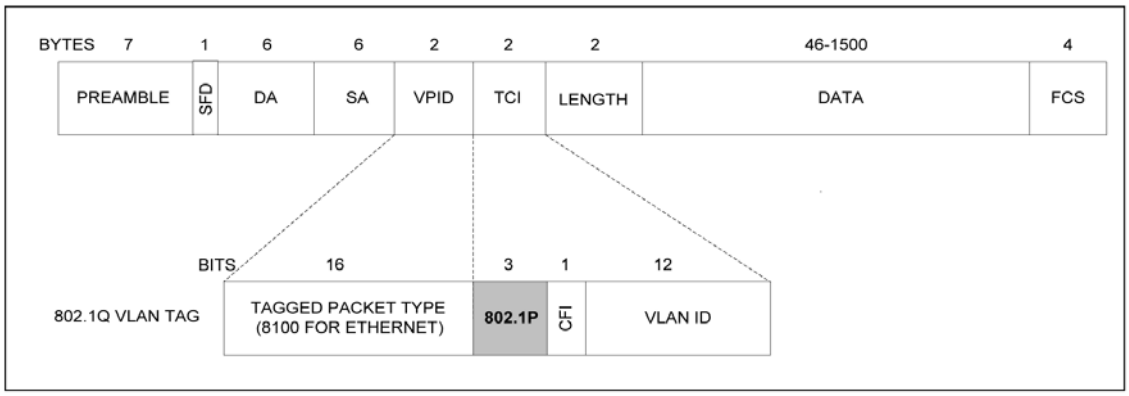
With port-based priority, each ingress port is individually classified as a specific priority level. All packets received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits[4:3] of registers P1CR1, P2CR1, and P3CR1 is used to enable port-based priority for Ports 1, 2, and the host port, respectively.

3.14.2 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8852 examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and used to look up the "priority mapping" value, as specified by the register SGCR6. The "priority mapping" value is programmable.

Figure 3-8 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-8: 802.1P PRIORITY FIELD FORMAT



802.1p based priority is enabled by bit[5]of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively.

The KSZ8852 provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN protocol ID (VPID) and the 2 bytes tag control information field (TCI), is also referred to as the 802.1Q VLAN tag.

Tag insertion is enabled by bit [2] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in register sets P1VIDCR, P2VIDCR, and P3VIDCR for Ports 1, 2, and the host port, respectively. The KSZ8852 does not add tags to already tagged packets.

Tag removal is enabled by bit [1] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8852 will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

3.14.3 PRIORITY FIELD RE-MAPPING

This is a QoS feature that allows the KSZ8852 to set the “user priority ceiling” at any ingress port. If the ingress packet’s priority field has a higher priority value than the default tag’s priority field of the ingress port, the packet’s priority field is replaced with the default tag’s priority field. The “user priority ceiling” is enabled by bit[3] of registers P1CR2, P2CR2, and P3CR2 for Ports 1, 2, and the host port, respectively.

3.14.4 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the TOS registers shown in the Type-of-Service (TOS) Priority Control Registers section. The TOS priority control registers implement a fully-decoded, 128-bit differentiated services code point (DSCP) register to determine packet priority from the 6-bit TOS field in the IP header. When the most significant 6 bits of the TOS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.15 Rate-Limiting Support

The KSZ8852 supports hardware rate limiting from 64 Kbps to 99 Mbps, independently on the “receive side” and on the “transmit side” as per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up ingress rate control registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up egress rate control registers. The size of each frame has options to include minimum inter-frame gap (IFG) or preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8852 provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8852 counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the “leaky bucket” algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

3.16 MAC Address Filtering Function

When a packet is received, the destination MAC address is looked up in both the static and dynamic MAC address tables. If the address is not found in either of these tables, then the destination MAC address is “unknown”. By default, an unknown unicast packet is forwarded to all ports except the port at which it was received. An optional feature makes it possible to specify the port or ports to which to forward unknown unicast packets. It is also possible to specify no ports, meaning that unknown unicast packets will be discarded. This feature is enabled by setting bit [7] in SGCR7.

The unicast MAC address filtering function is useful in preventing the broadcast of unicast packets that could degrade the quality of this port in applications such as voice-over-internet protocol (VoIP).

3.17 Queue Management Unit (QMU)

The Queue Management Unit (QMU) manages packet traffic on port 3 between the internal MAC and the external host processor interface. It has built-in packet memory for receive and transmit functions called transmit queue (TXQ) and receive queue (RXQ). The RXQ capacity is 12 Kbytes, and the TXQ capacity is 6 Kbytes. These FIFOs support back-to-back, non-blocking frame transfer performance. There are control registers for system control, frame status registers for current packet transmit/receive status, and interrupts to inform the host of the real time TX/RX status.

Please refer to the **Section 3.1 “Direction Terminology”** for a discussion of the different terminology used to describe the QMU.

3.17.1 TRANSMIT QUEUE (TXQ) FRAME FORMAT

The frame format for the transmit queue is shown in Table 3-7. The first word contains the control information for the frame to transmit. The second word is used to specify the total number of bytes of the frame. The packet data follows. The packet data area holds the frame itself. It may or may not include the CRC checksum depending upon whether hardware CRC checksum generation is enabled in bit [1] in TXCR register.

Multiple frames can be pipelined in both the transmit queue and receive queue as long as there is enough queue memory, thus avoiding overrun. For each transmitted frame, the transmit status information for the frame is located in the TXSR (0x172) register.

TABLE 3-7: FRAME FORMAT FOR TRANSMIT QUEUE

Packet Memory Address Offset (Bytes)	2nd Byte [15:8]	1st Byte [7:0]
0	**Control Word** (High byte and low byte need to swap in Big-Endian mode)	
2	**Byte Count** (High byte and low byte need to swap in Big-Endian mode)	
4 - Up	**Transmit Packet Data** (Maximum size is 2000)	

Since multiple packets can be pipelined into the TX packet memory for transmit, the transmit status reflects the status of the packet that is currently being transferred on the MAC interface, which may or may not be the last queued packet in the TX queue.

The transmit control word is the first 16-bit word in the TX packet memory, followed by a 16-bit byte count. It must be word aligned. Each control word corresponds to one TX packet. Table 3-8 gives the transmit control word bit fields.

TABLE 3-8: TRANSMIT CONTROL WORD BIT FIELDS

Bit	Description
15	TXIC Transmit Interrupt on Completion: When this bit is set, the KSZ8852 sets the transmit interrupt after the present frame has been transmitted.
14 - 10	Reserved
9 - 8	Reserved
7 - 6	Reserved
5 - 0	TXFID Transmit Frame ID: This field specifies the frame ID that is used to identify the frame and its associated status information in the transmit status register.

The transmit byte count specifies the total number of bytes to be transmitted from the TXQ. Its format is given Table 3-9.

TABLE 3-9: TRANSMIT BYTE COUNT FORMAT

Bit	Description
15 - 11	Reserved
10 - 0	TXBC Transmit Byte Count: Transmit Byte Count. Hardware uses the byte count information to conserve the TX buffer memory for better utilization of the packet memory. **Note:** The hardware behavior is unknown if an incorrect byte count information is written to this field. Writing a “0” value to this field is not permitted.

The data area contains six bytes of destination address (DA) followed by six bytes of source address (SA), followed by a variable-length number of bytes. On transmit, all bytes are provided by the CPU, including the source address. The KSZ8852 does not insert its own SA. The IEEE 802.3 frame length word (frame type in Ethernet) is not interpreted by the KSZ8852. It is treated transparently as data both for transmit operations.

3.17.2 FRAME TRANSMITTING PATH OPERATION IN TXQ

This section describes the typical register settings for transmitting packets from a host processor to the KSZ8852 using the generic bus interface. The user can use the default value for most of the transmit registers. Table 3-10 describes all the registers which need to be set and used for transmitting single frames.

TABLE 3-10: REGISTER SETTING FOR TRANSMIT FUNCTION BLOCK

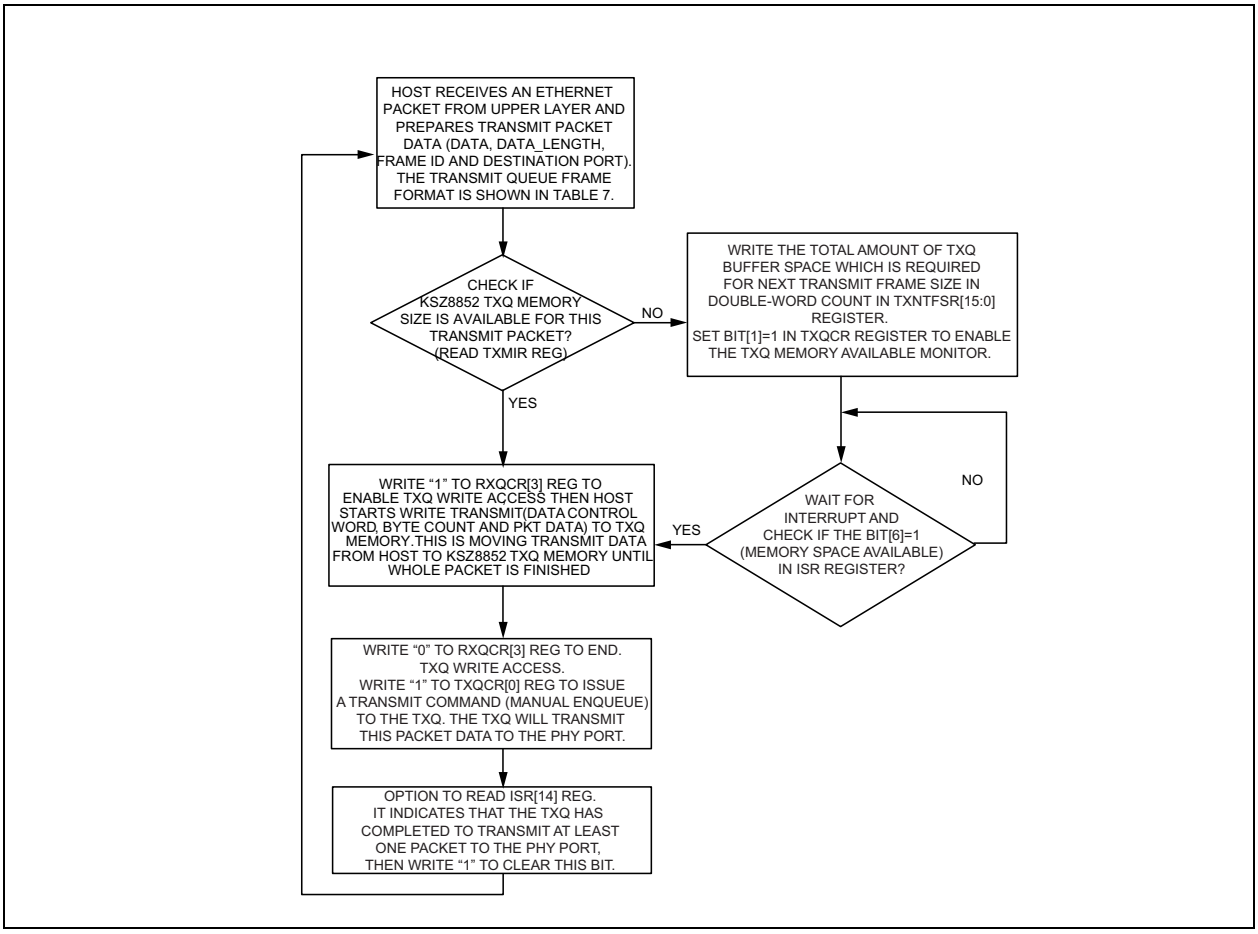
Register Name [bit](offset)	Description
TXCR[3:0](0x170) TXCR[8:5](0x170)	Set transmit control function as below: Set bit[3] to enable transmitting flow control. Set bit [2] to enable transmitting padding. Set bit[1] to enable transmitting CRC. Set bit [0] to enable transmitting block operation. Set transmit checksum generation for ICMP, UDP, TCP and IP packet.
TXMIR[12:0](0x178)	The amount of free transmit memory available is represented in units of byte. The TXQ memory (6 KByte) is used for both frame payload and control word.
TXQCR[0](0x180)	For single frame to transmit, set this bit[0] = “1” (manual enqueue). The KSZ8852 will enable current TX frame prepared in the TX buffer is queued for transmit; this is only transmit one frame at a time. **Note:** This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting up another new TX frame.
TXQCR[1](0x180)	When this bit is written as “1”, the KSZ8852 will generate interrupt (bit[6] in the ISR register) to CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at TXNTFSR (0x19E) register. **Note:** This bit is self−clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before set to “1” again.
RXQCR[3](0x182)	Set bit[3] to start DMA access from host CPU either read (receive frame data) or write (transmit data frame).
TXFDPR[14](0x184)	Set bit[14] to enable TXQ transmit frame data pointer register increments automatically on accesses to the data register.
IER[14][6](0x190)	Set bit[14] to enable transmit interrupt in interrupt enable register. Set bit[6] to enable transmit space available interrupt in interrupt enable register.
ISR[15:0](0x192)	Write all ones (0xFFFF) to clear all interrupt status bits after interrupt occurred in interrupt enable register.
TXNTFSR[15:0](0x19E)	The host CPU is used to program the total amount of TXQ buffer space which is required for next total transmit frames size in double-word count.

3.17.3 DRIVER ROUTINE FOR TRANSMITTING PACKETS FROM HOST PROCESSOR TO KSZ8852

The transmit routine is called by the upper layer to transmit a contiguous block of data through the Ethernet controller. It is the user’s choice to decide how the transmit routine is implemented. If the Ethernet controller encounters an error while transmitting the frame, it’s the user’s choice to decide whether the driver should attempt to retransmit the same frame or discard the data. Figure 3-9 shows the step-by-step process for transmitting a single packet from host processor to the KSZ8852.

Each DMA write operation from the host CPU to the “write TXQ frame buffer” begins with writing a control word and a byte count of the frame header. At the end of the write, the host CPU must write each piece of frame data to align with a double word boundary at the end. For example, the host CPU has to write up to 68 bytes if the transmit frame is 65 bytes.

FIGURE 3-9: HOST TX SINGLE FRAME IN MANUAL ENQUEUE FLOW DIAGRAM



3.17.4 RECEIVE QUEUE (RXQ) FRAME FORMAT

The frame format for the receive queue is shown in Table 3-11. The first word contains the status information for the frame received. The second word is the total number of bytes of the RX frame. Following that is the packet data area. The packet data area holds the frame itself. It includes the CRC checksum.

TABLE 3-11: FRAME FORMAT FOR RECEIVE QUEUE

Packet Memory Address Offset (Bytes)	Bit 15 2nd Byte	Bit 15 1st Byte
0	**Status Word** (High byte and low byte need to swap in Big-Endian mode. Also see description in RXFHSR register)(**TABLE 4-146: "Receive Frame Header Status Register (0x17C – 0x17D): RXFHSR"**).	
2	**Byte Count** (High byte and low byte need to swap in Big-Endian mode. Also see description in RXFHBCR register)(**TABLE 4-147: "Receive Frame Header Byte Count Register (0x17E – 0x17F): RXFHBCR"**)	
4 - Up	**Receive Packet Data** (Maximum size is 2000)	

TABLE 3-12: REGISTER SETTINGS FOR RECEIVE FUNCTION BLOCK

Register Name [bit](offset)	Description
RXCR1 (0x174) RXCR2 (0x176)	Set receive control function as below: Set RXCR1[10] to enable receiving flow control. Set RXCR1[0] to enable receiving block operation. Set receive checksum check for ICMP, UDP, TCP, and IP packet. Set receive address filtering scheme as shown in Table 3-2.
RXFHSR[15:0] (0x17C)	This register (read only) indicates the current received frame header status information.
RXFHBCR[11:0] (0x17E)	This register (read only) indicates the current received frame header byte count information.
RXQCR[12:3] (0x182)	Set RXQ control function as below: Set bit[3] to start DMA access from host CPU either read (receive frame data) or write (transmit data frame). Set bit[4] to automatically enable RXQ frame buffer de-queue. Set bit[5] to enable RX frame count threshold and read bit[10] for status. Set bit[6] to enable RX data byte count threshold and read bit[11] for status. Set bit[7] to enable RX frame duration timer threshold and read bit[12] for status. Set bit[9] to enable RX IP header two-byte offset.
RXFDPR[14] (0x186)	Set bit[14] to enable RXQ address register increments automatically on accesses to the data register.
RXDTTR[15:0] (0x18C)	Used to program the received frame duration timer value. When Rx frame duration in RXQ exceeds this threshold in 1 µs interval count and bit[7] of RXQCR register is set to “1”, the KSZ8852 will generate RX interrupt in ISR[13] and indicate the status in RXQCR[12].
RXDBCTR[15:0] (0x18E)	Used to program the received data byte count value. When the number of received bytes in RXQ exceeds this threshold in byte count and bit [6] of RXQCR register is set to “1”, the KSZ8852 will generate RX interrupt in ISR[13] and indicate the status in RXQCR[11].
IER[13] (0x190)	Set bit[13] to enable receive interrupt in interrupt enable register.
ISR[15:0] (0x192)	Write all ones (0xFFFF) to clear all interrupt status bits after interrupt occurred in interrupt status register.
RXFC[15:8] (0x1B8)	Rx Frame Count. This indicates the total number of frames received in the RXQ frame buffer when the receive interrupt (Reg. ISR, bit [13]) occurred.
RXFCTR[7:0] (0x19C)	Used to program the received frame count threshold value. When the number of received frames in RXQ exceeds this threshold value and bit[5] of RXQCR register is set to “1”, the KSZ8852 will generate an RX interrupt in ISR[13] and indicate the status in RXQCR[10].

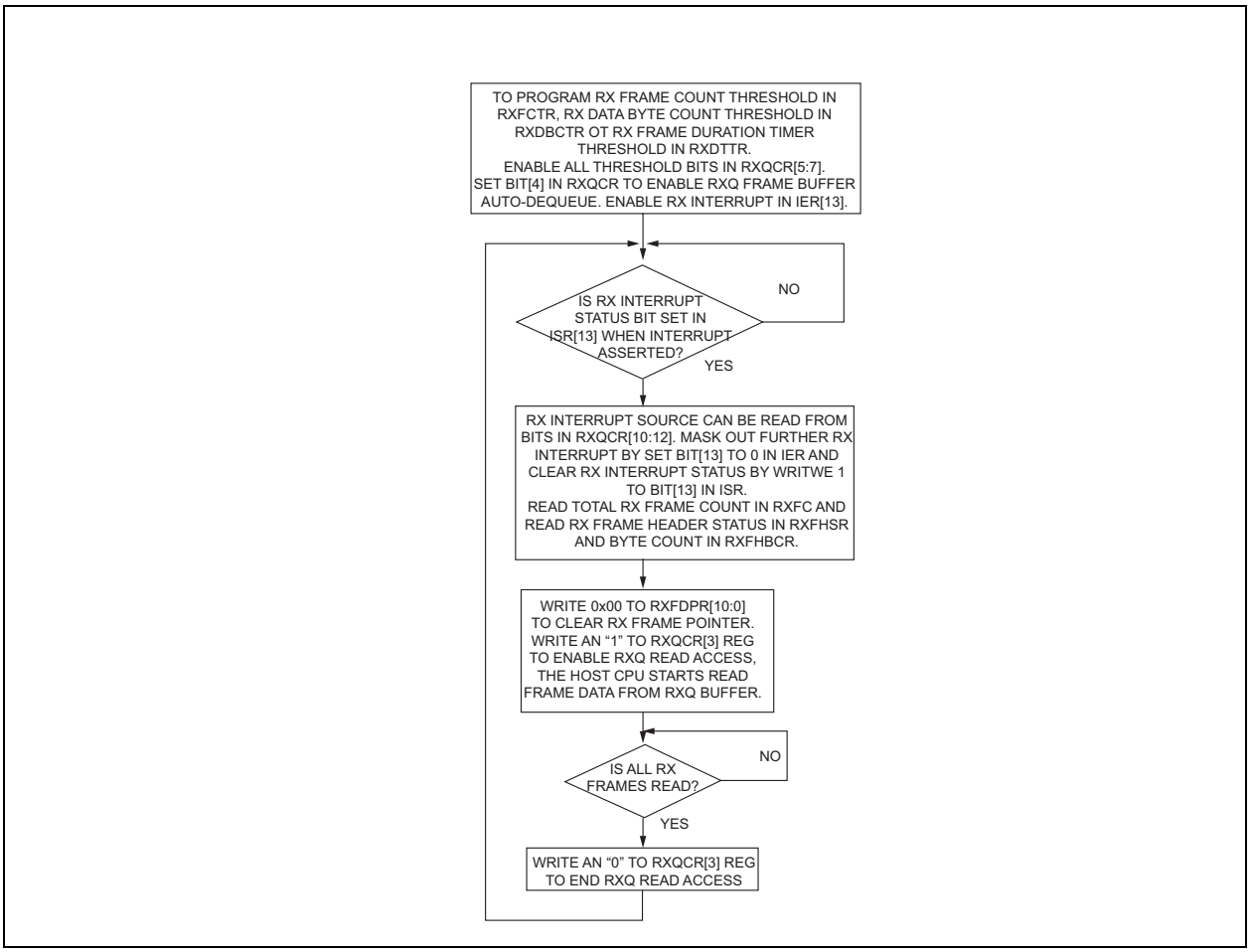
3.17.5 DRIVER ROUTINE FOR RECEIVING PACKETS FROM THE KSZ8852 TO THE HOST PROCESSOR

The software driver receives data packet frames from the KSZ8852 device either as a result of polling or an interrupt based service. When an interrupt is received, the operating system invokes the interrupt service routine that is in the interrupt vector table.

If your system has operating system support, to minimize interrupt lockout time, the interrupt service routine should handle at interrupt level only those tasks that require minimum execution time, such as error checking or device status change. The routine should queue all the time-consuming work to transfer the packet from the KSZ8852 RXQ into system memory at task level. Figure 3-10 shows the step-by-step for receive packets from KSZ8852 to host processor.

For each DMA read operation from the host CPU to read the RXQ frame buffer, the first read data (byte in 8-bit bus mode, word in 16-bit bus mode) is dummy data and must be discarded by the host CPU. Afterward, the host CPU must read each data frame to align it with a double word boundary at the end. For example, the host CPU has to read up to 68 bytes if the number of received frames is 65 bytes.

FIGURE 3-10: HOST RX SINGLE OR MULTIPLE FRAMES IN AUTO-DEQUEUE FLOW DIAGRAM



In order to read received frames from RXQ without error, the software driver must follow these steps:

1. When a receive interrupt occurs and the software driver writes a "1" to clear the RX interrupt in the ISR register; the KSZ8852 will update the Rx frame counter (RXFC) register for this interrupt.
2. When the software driver reads back the Rx frame count (RXFC) register, the KSZ8852 will update both the receive frame header status and byte count registers (RXFHSR/RXFHBCR).
3. When the software driver reads back both the receive frame header status and byte count registers (RXFHSR/RXFHBCR), the KSZ8852 will update the next receive frame header status and byte count registers (RXFHSR/RXFHBCR).

3.18 Device Clocks

A 25 MHz crystal or oscillator clock is required to operate the device. This clock is used as input to a PLL clock synthesizer which generates 125 MHz, 62.5 MHz, and 31.25 MHz clocks for the KSZ8852 system timing. Table 3-13 summarizes the clocking.

TABLE 3-13: KSZ8852 DEVICE CLOCKS

Clock	Usage	Source	Strapping Option
25 MHz	Used for general system internal clocking. Used to generate an internal 125 MHz clock.	A 25 MHz crystal connected between pins X1 and X2. (or) A 25 MHz oscillator that is connected to only the X1 pin. The X2 pin is left unconnected.	None
SEEPROM Clock	Used to clock data to or from the Serial EEPROM.	2.5 MHz, divided down from the 25 MHz input clock. Can also be software generated via Register 0x122 - 0x123 (EEPCR). After reset time, this is the only way to generate the clock to the Serial EEPROM for access.	—

Note that the clock tree power-down control register (0x038 - 0x039) CTPDC is used to power-down the clocks in various areas of the device. There are no other internal register bits which control the clock generation or usage in the device.

3.19 Power

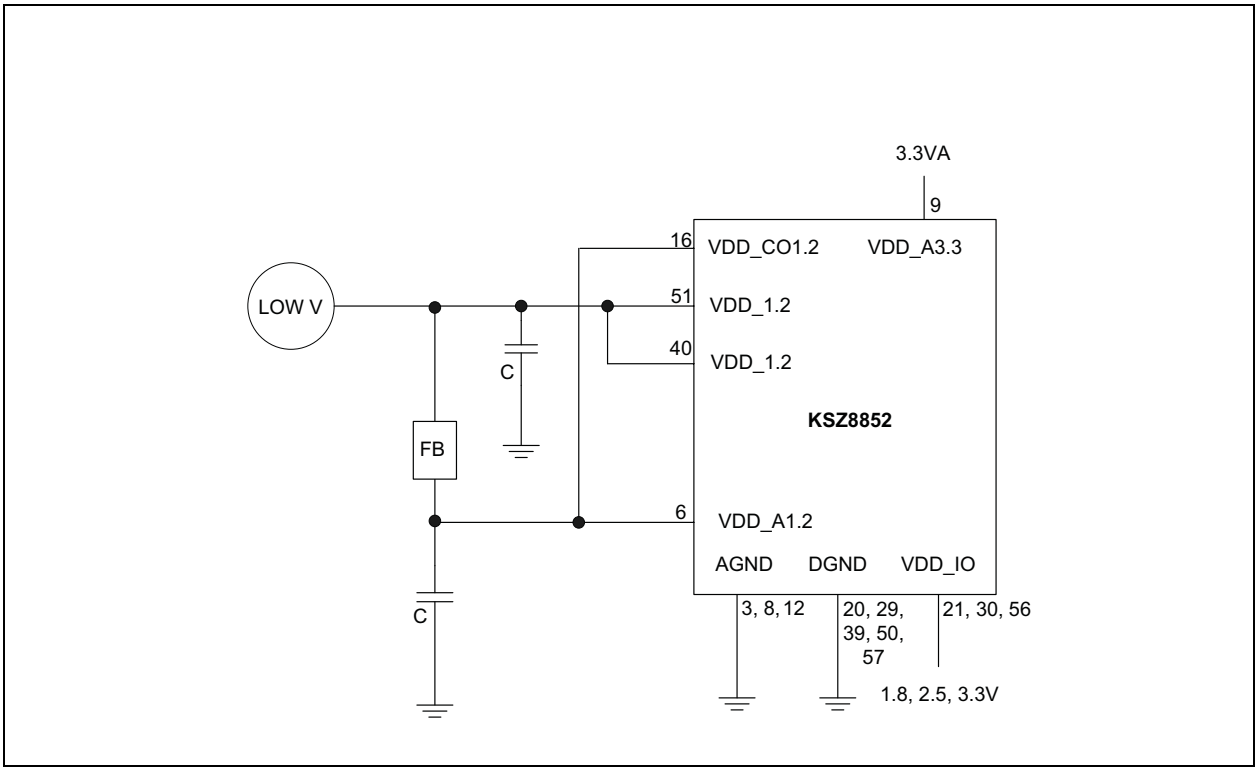
The KSZ8852 device requires a single 3.3V supply to operate. An internal low voltage LDO provides the necessary low voltage (nominal ~1.3V) to power the analog and digital logic cores. The various I/O's can be operated at 1.8V, 2.5V, and 3.3V. Table 3-14 illustrates the various voltage options and requirements of the device.

TABLE 3-14: VOLTAGE OPTIONS AND REQUIREMENTS

Power Signal Name	Device Pin	Requirement
$V_{DD\_A3.3}$	9	3.3V input power to the analog blocks in the device.
V_{DD_IO}	21, 30, 56	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device. This voltage is also used as the input to the internal low-voltage regulator.
V_{DD_AL}	6	Filtered low-voltage analog input voltage. This is where filtered low voltage is fed back into the device to power the analog block.
V_{DD_COL}	16	Filtered low-voltage AD input voltage. This pin feeds low voltage to digital circuits within the analog block.
V_{DD_L}	40, 51	Output of internal low voltage LDO regulator. This voltage is available on these pins to allow connection to external capacitors and ferrite beads for filtering and power integrity. These pins must be externally connected to pins 6 and 16. If the internal LDO regulator is turned off, these pins become power inputs.
AGND	3, 8, 12	Analog Ground.
DGND	20, 29, 39, 50, 57	Digital Ground.

The preferred method of configuring the low-voltage related power pins when using an external low-voltage regulator is illustrated in Figure 3-11. The number of capacitors, values of capacitors, and exact placement of components will depend on the specific design.

FIGURE 3-11: RECOMMENDED LOW-VOLTAGE POWER CONNECTION USING AN EXTERNAL LOW-VOLTAGE REGULATOR



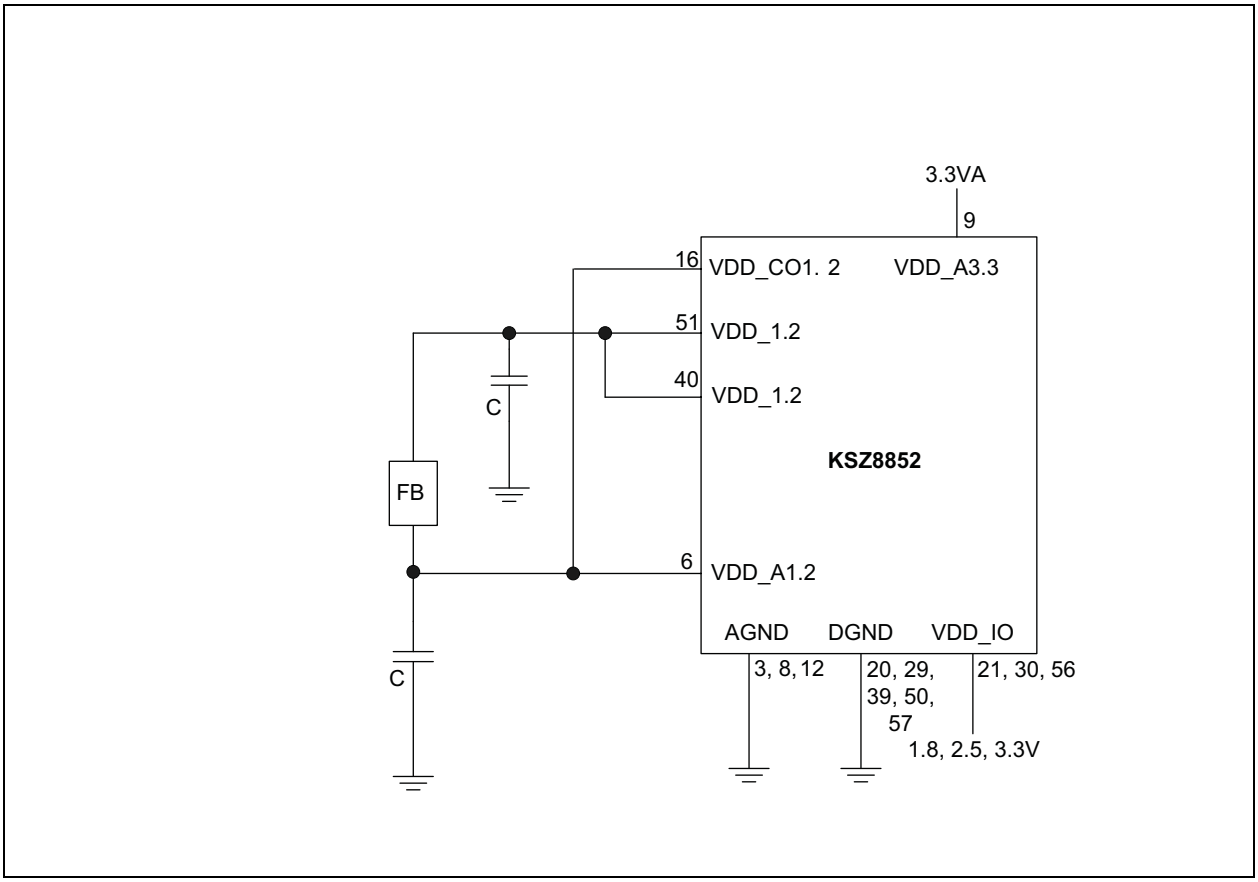
3.20 Internal Low Voltage LDO Regulator

The KSZ8852 reduces board cost and simplifies board layout by integrating a low-noise internal low-voltage LDO regulator to supply the nominal ~1.3V core power voltage for a single 3.3V power supply solution. If it is desired to take advantage of an external low-voltage supply that is available, the internal low-voltage regulator can be disabled to save power. The LDO_Off bit, Bit [7] in Register 0x748 is used to enable or disable the internal low-voltage regulator. The default state of the LDO_Off bit is “0” which enables the internal low-voltage regulator. Turning off the internal low-voltage regulator will require software to write a “1” to that control bit. During the time from power up to setting this bit, both the external voltage supply and the internal regulator will be supplying power. Note that it is not necessary to turn off the internal low-voltage regulator. No damage will occur if it is left on. However, leaving it on will result in less than optimized power consumption.

The internal regulator takes its power from VDD_IO, and functions best when VDD_IO is 3.3V or 2.5V. If VDD_IO is 1.8V, the output voltage will be decreased somewhat. For optimal performance, an external power supply, in place of the internal regulator, is recommended when VDD_IO is 1.8V.

The preferred method of configuring the low-voltage related power pins for using the internal low-voltage regulator is illustrated in Figure 3-12. The output of the internal regulator is available on pins 40 and 51 and is filtered using external capacitors and a ferrite bead to supply power to pins 6 and 16. The number of capacitors, values of capacitors, and exact placement of components will depend upon the specific design.

FIGURE 3-12: RECOMMENDED LOW VOLTAGE POWER CONNECTION USING THE INTERNAL LOW-VOLTAGE REGULATOR



3.21 Power Management

The KSZ8852 supports enhanced power management features in low power state with energy detection to ensure low-power dissipation during device idle periods. There are three operation modes under the power management function which is controlled by two bits in the power management control and wake-up event status register (PMCTRL, 0x032 – 0x033) as shown below:

- PMCTRL[1:0] = “00” Normal Operation Mode
- PMCTRL[1:0] = “01” Energy Detect Mode
- PMCTRL[1:0] = “10” Global Soft Power-Down Mode

Table 3-15 indicates all internal function blocks status under three different power management operation modes.

TABLE 3-15: POWER MANAGEMENT AND INTERNAL BLOCKS

KSZ8852 Function Blocks	Power Management Operation Modes		
	Normal Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled
Tx/Rx PHYs	Enabled	Energy detect at Rx	Disabled
MACs	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled

3.21.1 NORMAL OPERATION MODE

Normal operation mode is the power management mode entered into after device power-up or after hardware reset pin 63. It is established via bits [1:0] = “00” in the PMCTRL register. When the KSZ8852 is in normal operation mode, all PLL clocks are running, PHYs and MACs are on, and the CPU is ready to read or write the KSZ8852 through host interface.

During the normal operation mode, the host CPU can change the power management mode bits [1:0] in the PMCTRL register to transition to another desired power management mode.

3.21.2 ENERGY DETECT MODE

Energy Detect mode provides a mechanism to save more power than in normal operation mode when the KSZ8852 is not connected to an active link partner. For example, if the cable is not present or it is connected to a powered down partner, the KSZ8852 can automatically enter the low power state in energy detect mode. Once activity resumes after attaching a cable or by a link partner attempting to establish a link, the KSZ8852 will automatically power up into the normal power state in energy detect normal power state.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the KSZ8852 reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. Energy detect mode is enabled by setting bits [1:0] = “01” in the PMCTRL register. When the KSZ8852 is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than a pre-configured value determined by bits[7:0] (Go-Sleep Time) in the GST register, the device will go into the low power state. When the KSZ8852 is in low power state, it will keep monitoring the cable energy. Once energy is detected from the cable and is present for a time longer than 100 ns, the KSZ8852 will enter the normal power state.

The KSZ8852 will assert the PME output pin if the corresponding enable bit[0] is set in the PMEE register (0x034) or generate an interrupt to signal that an energy detect event has occurred if the corresponding enable bit[2] is set in the IER register (0x190). Once the local power management unit detects the PME output is asserted or that the interrupt is active, it will power up the host processor and issue a wake-up command which is a read cycle to read the globe reset register, GRR (0x126) to wake up the KSZ8852 from the low power state to the normal power state. When the KSZ8852 device is in the normal power state, it is able to transmit or receive packet from the cable.

3.21.3 GLOBAL SOFT POWER-DOWN MODE

Soft power-down mode is entered by setting bits [1:0] = “10” in PMCTRL register. When the device is in this mode, all PLL clocks are disabled, the PHYs and the MACs are off, all internal registers value will change to their default value (except the BIU, QMU registers), and the host CPU interface is only used to wake-up this device from the current soft power-down mode to normal operation mode by setting bits [1:0] = “00” in the PMCTRL register.

Note that the registers within the QMU block will not be changed to their default values when a soft power-down is issued.

All strap-in pins are sampled to latch any new values when soft power-down is disabled.

3.21.4 ENERGY-EFFICIENT ETHERNET (EEE)

Energy Efficient Ethernet (EEE) is implemented in the KSZ8852 as described in the IEEE 802.3AZ specification for MII operations on Port 1 and Port 2. EEE is not performed at Port 3 since that is a Parallel Host interface. The MII connections between the MAC and PHY blocks are internal to the chip and are not visible to the user. The standards are defined around a MAC that supports special signaling associated with EEE. EEE saves power by keeping the voltage on the Ethernet cable at approximately 0V for as often as possible during periods of no traffic activity. This is called low-power idle state (LPI). However, the link will respond automatically when traffic resumes and do so in such a way as to not cause blocking or dropping of any packets. The wake up time for 100BT is specified to be less than 30 µs. The transmit and receive directions are independently controlled. Note the EEE is not specified or implemented for 10BT. In 10BT, the transmitter is already OFF during idle periods.

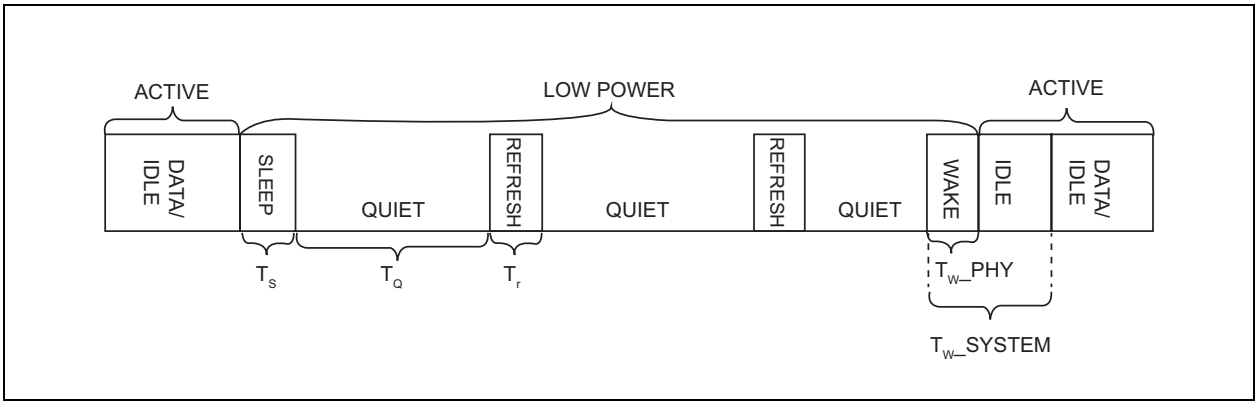
The EEE feature is enabled by default. EEE is auto-negotiated independently for each direction on a link, and is enabled only if both nodes on a link support it. To disable EEE, clear the next page enable bit(s) for the desired port(s) in the PCSEEEC register (0x0F3) and restart auto-negotiation.

Based on the EEE specification, the energy savings from EEE occurs at the PHY level. However, the KSZ8852 reduces the power consumption not only in the PHY block but also in the MAC and switch blocks by shutting down any unused clocks as much as possible when the device is at LPI state. A comprehensive LPI request on/off policy is also built-in at the switch level to determine when to issue LPI requests and when to stop the LPI request. Some software control options are provided in the device to terminate the LPI request in the early phase when certain events occur to reduce the latency impact during LPI recovery. A configurable LPI recovery time register is provided at each port to specify the

recovery time (25 µs at default) required for the KSZ8852 and its link partner before they are ready to transmit and receive a packet after going back to the normal state. For details, refer the KSZ8852 EEE registers (0x0E0 – 0x0F7) description.

Figure 3-13 illustrates the time during which LPI mode is active is during what is called quiet time.

FIGURE 3-13: TRAFFIC ACTIVITY AND EEE



3.22 Wake-On-LAN

Wake-on-LAN is considered a power management feature in that it can be used to communicate to a specific network device and tell it to “wake up” from sleep mode and be prepared to transfer data. The KSZ8852 can be programmed to notify the host of the wake-up detected condition. It does so by assertion of the interrupt signal pin (INTRN) or the power management event signal pin (PME). A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state (working). There are four events that will trigger the wake-up interrupt to occur. They are:

- Detection of an energy signal over a pre-configured value (Indicated by bit[2] in the ISR register being set)
- Detection of a linkup in the network link state (Indicated by bit[3] in the ISR register being set)
- Receipt of a Magic Packet (Indicated by bit[4] in the ISR register being set)
- Receipt of a network wake-up frame (Indicated by bit[5] in the ISR register being set)

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

3.22.1 DETECTION OF ENERGY

The energy is detected from the cable and is continuously presented for a time longer than pre-configured value, especially when this energy change may impact the level at which the system should re-enter to the normal power state.

3.22.2 DETECTION OF LINKUP

Link status wake events are useful to indicate a linkup in the network’s connectivity status.

3.22.3 WAKE-UP PACKET

Wake-up packets are certain types of packets with specific CRC values that a system recognizes as a ‘Wake-Up’ frame. The KSZ8852 supports up to four user defined wake-up frames shown below:

- Wake-up frame 0 is defined in wake-up frame registers (0x130 – 0x13B) and is enabled by bit [0] in the Wake-Up frame register (0x12A).
- Wake-up frame 1 is defined in wake-up frame registers (0x140 – 0x14B) and is enabled by bit [1] in the Wake-Up frame register (0x12A).
- Wake-up frame 2 is defined in wake-up frame registers (0x150 – 0x15B) and is enabled by bit [2] in the Wake-Up frame register (0x12A).
- Wake-up frame 3 is defined in wake-up frame registers (0x160 – 0x16B) and is enabled by bit [3] in the Wake-Up frame register (0x12A).

3.22.4 MAGIC PACKET

Magic Packet (MP) technology is used to remotely wake up a sleeping or powered off PC on a LAN. This is accomplished by sending a specific packet of information, called a MP frame, to a node on the network. When a PC capable of receiving the specific frame goes to sleep, it enables the MP RX mode in the LAN controller, and when the LAN controller receives a MP frame, the LAN controller will alert the system to wake up.

MP is a standard feature integrated into the KSZ8852. The controller implements multiple advanced power-down modes including MP to conserve power and operate more efficiently. Once the KSZ8852 has been put into MP enable mode (WFCR[7] = “1”), it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a MP frame.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the LAN controller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC − FF FF FF FF FF FF − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 −11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − 11 22 33 44 55 66 − MISC − CRC.

There are no further restrictions on an MP frame. For example, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the frame’s destination.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the KSZ8852 controller detects the data sequence, however, it then alerts the PC’s power management circuitry (assert the PME pin) to wake up the system.

3.22.5 INTERRUPT GENERATION ON POWER MANAGEMENT RELATED EVENTS

There are two ways an interrupt can be generated to the host whenever a power management related event takes place. The resulting interrupts are via the PME signal pin or via the INTRN signal pin. The usage is described in the following sub-sections:

3.22.6 TO GENERATE AN INTERRUPT ON THE PME SIGNAL PIN

The PMEE register (0x034 - 0x035) contains the bits needed to control generating an interrupt on the PME signal pin whenever specific power management related events occur. The power management events controlled by this register includes detection of a Wake-Up frame, detection of a MP, detection that the link has changed state, and detection of energy on the Ethernet lines.

3.22.7 TO GENERATE AN INTERRUPT ON THE INTRN SIGNAL PIN

The IER register (0x190 - 0x191) contains the bits needed to control generating an interrupt on the INTRN signal pin whenever specific power management related events occur. The power management events controlled by this register includes detection of a wake-up from a link state change and wake-up from detection of energy on the Ethernet lines.

3.23 Interfaces

The KSZ8852 device incorporates a number of interfaces to enable it to be designed into a standard network environment as well as a vendor unique environment. The available interfaces and details of each usage are provided in Table 3-16.

TABLE 3-16: AVAILABLE INTERFACES

Interface	Type	Usage	Registers Accessed
Host Bus	Configuration and Data Flow	Provides a path for network data to be transferred to and from the host processor. Provides in-band communication between a host processor and the KSZ8852 device for configuration, control, and monitoring.	ALL
Serial EEPROM	Configuration and Register Access	Device can access the Serial EEPROM to load the MAC Address at power-up. In addition, the remainder of EEPROM space can be written or read and used as needed by the host	110h − 115h
PHY	Data Flow	Interface to the two internal PHY devices.	N/A

3.23.1 BUS INTERFACE UNIT (BIU)/HOST INTERFACE

The BIU manages the host interface which is a generic indirect data bus interface, and is designed to communicate with embedded processors. Typically, no glue logic is required when interfacing to standard asynchronous buses and processors.

3.23.2 SUPPORTED TRANSFERS

The BIU can support asynchronous transfers in SRAM-like slave mode. To support the data transfers, the BIU provides a group of signals as shown in Table 3-17. These signals are SD[15:0], CMD, CSN, RDN, WRN, and INTRN. Note that it is intended that the CSN signal be driven by logic within the host processor or by some external logic which decode the base address so the KSZ8852 device does not have to do address range decoding.

3.23.3 PHYSICAL DATA BUS SIZE

The BIU supports an 8-bit or 16-bit host standard data bus. Depending on the size of the physical data bus, the KSZ8852 can support 8-bit or 16-bit data transfers.

For a 16-bit data bus mode, the KSZ8852 allows an 8-bit and 16-bit data transfer.

For an 8-bit data bus mode, the KSZ8852 only allows an 8-bit data transfer.

The KSZ8852 supports internal data byte-swapping. This means that the system/host data bus HD[7:0] connects to SD[7:0] for an 8-bit data bus interface. For a 16-bit data bus, the system/host data bus HD[15:8] and HD[7:0] connects to SD[15:8] and SD[7:0] respectively.

TABLE 3-17: BUS INTERFACE UNIT SIGNAL GROUPING

Signal	Type	Function
SD[15:0]	I/O	**Shared Data Bus** 16-bit Mode & CMD = “0” SD[15:0] = D[15:0] data 16-bit Mode & CMD = “1”: SD[10:2] = A[10:2] Address SD[15:12] = BE[3:0] Byte enable SD[1:0] and SD[11] are not used 8-bit Mode & CMD = “0” SD[7:0] = D[7:0] data 8-bit Mode & CMD = “1” SD[7:0] = A[7:0] = 1st address access SD[2:0] = A[10:8] = 2nd address access SD[7:3] = Not used during 2nd address access
CMD	Input	**Command Type** This command input determines the SD[15:0] shared data bus access cycle information. 0: Data access 1: Command access for address and byte enable
CSN	Input	**Chip Select** Chip Select is an active low signal used to enable the shared data bus access.
INTRN	Output	**Interrupt** This low active signal is asserted low when an interrupt is being requested.
RDN	Input	**Asynchronous Read** This low active signal is asserted low during a read cycle. A 4.7 kΩ pull-up resistor is recommended on this signal.
WRN	Input	**Asynchronous Write** This low active signal is asserted low during a write cycle.

3.23.4 LITTLE AND BIG ENDIAN SUPPORT

The KSZ8852 supports either Little-Endian or Big-Endian processors. The external strap pin 62 (P2LED0) is used to select between two modes. The KSZ8852 host interface operates in Little Endian mode if this pin is pulled up during reset, or in Big Endian mode if this pin is pulled down during reset. If there is no external load on pin 62 during reset, it will be pulled up by its internal pull-up resistor, placing the interface into Little Endian mode.

Bit [11] (Endian mode selection) in RXFDPR register can be used to program either Little Endian mode (bit[11] = “0”) or Big Endian mode (bit [11] = “1”). Changes to this register bit will override the pin 62 strap-in selection. Software in the host processor must take care to avoid unintentionally changing bit [11] when writing to register RXFDPR.

3.23.5 ASYNCHRONOUS INTERFACE

For asynchronous transfers, the asynchronous interface uses RDN (read) or WRN (write) signal strobe for data latching. The host utilizes the rising edge of RDN to latch read data and the KSZ8852 will use the falling edge of WRN to latch write data.

All asynchronous transfers are either single-data or burst-data transfers. Byte or word data bus access (transfers) is supported. The BIU, however, provides flexible asynchronous interfacing to communicate with various applications and architectures. No additional address latch is required. The BIU qualifies both chip select (CSN) pin and write enable (WRN) pin to write the Address A[10:2] and BE[3:0] value (in 16-bit mode) or Address A[10:0] value (in 8-bit mode with two write accesses) into KSZ8852 when CMD (Command type) pin is high. The BIU qualifies the CSN pin as well as the read enable (RDN) or write enable (WRN) pin to read or write the SD[15:0] (16-bit mode) or SD[7:0] (8-bit mode) data value from or to KSZ8852 when command type (CMD) pin is low.

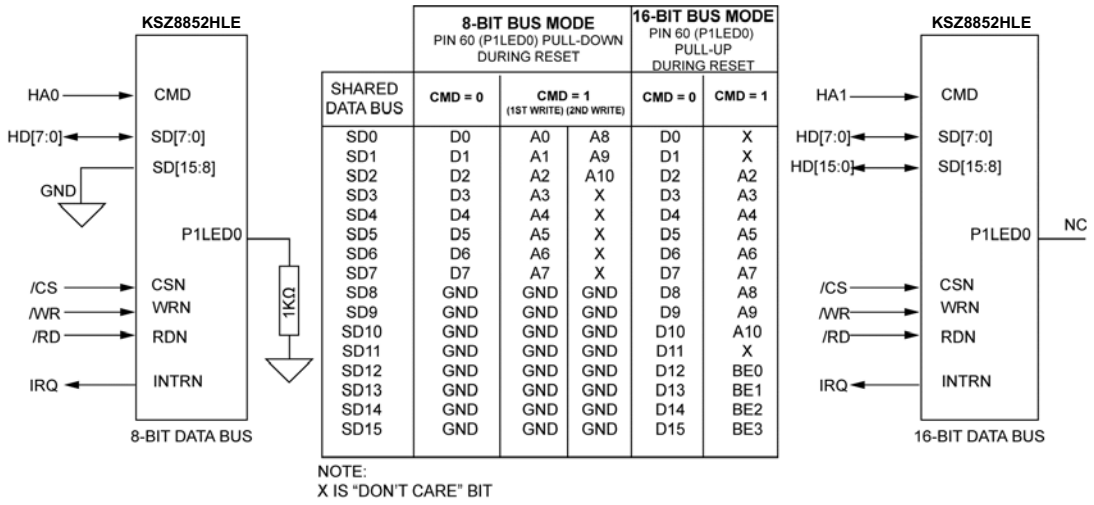
In order for software to read back the previous CMD register write value when CMD is “1”, the BIU qualifies both the CSN pin and the RDN pin to read the Address A[10:2] and BE[3:0] value (in 16−bit mode) back from the KSZ8852 when CMD pin is high. Reading back the addresses in 8-bit mode is not a valid operation.

3.23.6 BIU SUMMARY

Figure 3-14 shows the connection for different data bus sizes.

All of control and status registers in the KSZ8852 are accessed indirectly depending upon the CMD pin. The command sequence to access the specified control or status register is to write the register's address (when CMD = "1") then read or write this register data (when CMD = "0"). If both RDN and WRN signals in the system are only used for KSZ8852, the CSN pin can be forced to active low to simplify the system design. The CMD pin can be connected to host address line HA[0] for 8-bit bus mode or HA[1] for 16-bit bus mode.

FIGURE 3-14: KSZ8852 8-BIT AND 16-BIT DATA BUS CONNECTIONS



SHARED DATA BUS	8-BIT BUS MODE (PIN 60 (P1LED0) PULL-DOWN DURING RESET) CMD = 0	8-BIT BUS MODE CMD = 1 (1ST WRITE)	8-BIT BUS MODE CMD = 1 (2ND WRITE)	16-BIT BUS MODE (PIN 60 (P1LED0) PULL-UP DURING RESET) CMD = 0	16-BIT BUS MODE CMD = 1
SD0	D0	A0	A8	D0	X
SD1	D1	A1	A9	D1	X
SD2	D2	A2	A10	D2	A2
SD3	D3	A3	X	D3	A3
SD4	D4	A4	X	D4	A4
SD5	D5	A5	X	D5	A5
SD6	D6	A6	X	D6	A6
SD7	D7	A7	X	D7	A7
SD8	GND	GND	GND	D8	A8
SD9	GND	GND	GND	D9	A9
SD10	GND	GND	GND	D10	A10
SD11	GND	GND	GND	D11	X
SD12	GND	GND	GND	D12	BE0
SD13	GND	GND	GND	D13	BE1
SD14	GND	GND	GND	D14	BE2
SD15	GND	GND	GND	D15	BE3

NOTE:
X IS "DON'T CARE" BIT

Example:

Assume that the register space is located at an external I/O base address of 0x0300, a 16-bit data path is used, and it is desired to read two bytes of data from address 0xD0:

- External address decoding should decode the 0x0300 base address and create a signal for the CSN pin.
- The host address line 1 (HA[1]) is connected to the CMD input pin. For a host write to the device, the HA[1] being asserted will make CMD = "1" which will indicate that the data on the DS[15:0] bus are address and byte enable bits.
- As shown in Figure 3-14, the address bits A[10:2] are on SD[10:2].
- Write a value of 0x30D0 (register offset of 0xD0 with BE[1:0] (set on the SD[16:0] bus) to address 0x0302. (This sets up the address for the upcoming read operation by writing the desired destination address to be read.)
- Read the value from address 0x0300 with HA[1] = 0 (CMD =" "0"). The CSN pin is driven again by the decode of the base address of 0x0300.

3.23.7 SERIAL EEPROM INTERFACE

A serial EEPROM interface has been incorporated into the device to enable loading the MAC address into the device at power-up time with a value from an external serial EEPROM. This feature is turned on using a strapping option on pin 46. At power-up time, the voltage on pin 46 is sampled. If the voltage is found to be high, the first seven words of the serial EEPROM will be read. Registers 0x110 – 0x115 will be loaded with words 01h – 03h.

A pull-up resistor is connected to pin 46 to create a high state at power-up time (see Table 2-2). After the de-assertion of RSTN, the KSZ8852 reads in the seven words of data. Note that a 3-wire 1Kbit serial EEPROM utilizing 7−bit addresses must be used. Other size options will not function correctly. A 93C46 or equivalent type device meets these requirements. The EEPROM must be organized in 16−bit mode.

If the EEDIO pin (Pin 54) is pulled high, then the KSZ8852 performs an automatic read of words 0h – 6h in the external EEPROM after the de-assertion of reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR (0x122) registers. See Figure 7-3 in the Section 7.0, Timing Specifications for the details of the serial EEPROM access timing.

A sample of the KSZ8852 EEPROM format is shown in Table 3-18.

TABLE 3-18: KSZ8852 SERIAL EEPROM FORMAT

Word	15:8	7:0
0h	Reserved	
1h	Host MAC Address Byte 2	Host MAC Address Byte 1
2h	Host MAC Address Byte 4	Host MAC Address Byte 2
3h	Host MAC Address Byte 6	Host MAC Address Byte 5
4h - 6h	Reserved	
7h - 3Fh	Not used for the KSZ8852 (Available for user defined purposes)	

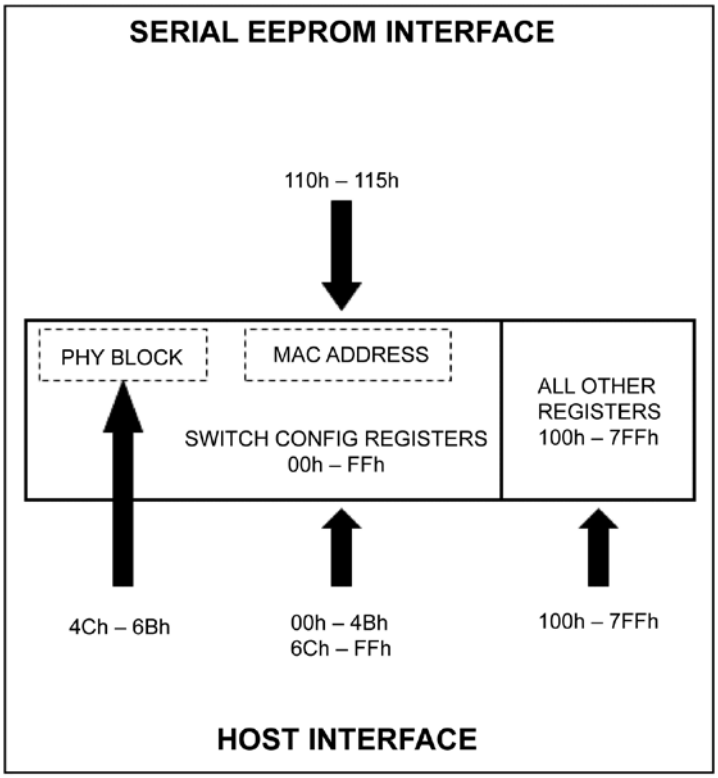
NOTES:

4.0 REGISTER DESCRIPTIONS

4.1 Device Registers

The KSZ8852 device has a rich set of registers available to manage the functionality of the device. Access to these registers is via the host interface (BIU). The device can be programmed to automatically load register locations 0x110 - 0x115 with a MAC address stored in Word locations 01h - 03h in an external serial EEPROM. Figure 4-1 provides a global picture of accessibility via the various interfaces and addressing ranges from the perspective of each interface.

FIGURE 4-1: INTERFACE AND REGISTER MAPPING



The registers within the linear 0x000 - 0x7FF address space are all accessible via the host interface bus by a microprocessor or CPU. The mapping of the various functions within that linear address space is summarized in Table 4-1.

TABLE 4-1: MAPPING OF FUNCTIONAL AREAS WITHIN THE ADDRESS SPACE

Register Locations	Device Area	Description
0x000 - 0x0FF	Switch Control and Configuration	Registers which control the overall functionality of the Switch, MAC, and PHYs
0x026 - 0x031	Indirect Access Registers	Registers used to indirectly address and access four distinct areas within the device. - MIB (Management Information Base) Counters - Static MAC Address Table - Dynamic MAC Address Table - VLAN Table

TABLE 4-1: MAPPING OF FUNCTIONAL AREAS WITHIN THE ADDRESS SPACE

Register Locations	Device Area	Description
0x044 - 0x06B	PHY1 and PHY2 Registers	The same PHY registers as specified in IEEE 802.3 specification.
0x100 - 0x16F	Interrupts, Global Reset, BIU	Registers and bits associated with interrupts, global reset, and the BIU
0x170 - 0x7FF	QMU and Global Registers	Registers and bits associated with the QMU

4.2 Register Map of CPU Accessible I/O Registers

The registers in the address range 00h through 7FFh can be read or written by a local CPU attached to the host interface. If enabled, registers 0x110 - 0x115 can be loaded at power on time by contents in the serial EEPROM. These registers are used for configuring the MAC address of the device.

4.2.1 I/O REGISTERS

The following I/O register space mapping table applies to 8-bit or 16-bit locations. Depending upon the mode selected, each I/O access can be performed using 8-bit or 16-bit wide transfers.

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x000 - 0x001	0x000 0x001	CIDER	0x8433	Chip ID and Enable Register [15:0]
0x002 - 0x003	0x002 0x003	SGCR1	0x3450	Switch Global Control Register 1 [15:0]
0x004 - 0x005	0x004 0x005	SGCR2	0x00F0	Switch Global Control Register 2 [15:0]
0x006 - 0x007	0x006 0x007	SGCR3	0x6320	Switch Global Control Register 3 [15:0]
0x008 - 0x00B	0x008 0x00B	Reserved (4-Bytes)	Don’t Care	None
0x00C - 0x00D	0x00C 0x00D	SGCR6	0xFA50	Switch Global Control Register 6 [15:0]
0x00E - 0x00F	0x00E 0x00F	SGCR7	0x0827	Switch Global Control Register 7 [15:0]
0x010 - 0x011	0x010 0x011	MACAR1	0x0010	MAC Address Register 1 [15:0]
0x012 - 0x013	0x012 0x013	MACAR2	0xA1FF	MAC Address Register 2 [15:0]
0x014 - 0x015	0x014 0x015	MACAR3	0xFFFF	MAC Address Register 3 [15:0]
0x016 - 0x017	0x016 0x017	TOSR1	0x0000	TOS Priority Control Register 1 [15:0]
0x018 - 0x019	0x018 0x019	TOSR2	0x0000	TOS Priority Control Register 2 [15:0]
0x01A - 0x01B	0x01A 0x01B	TOSR3	0x0000	TOS Priority Control Register 3 [15:0]
0x01C - 0x01D	0x01C 0x01D	TOSR4	0x0000	TOS Priority Control Register 4 [15:0]
0x01E - 0x01F	0x01E 0x01F	TOSR5	0x0000	TOS Priority Control Register 5 [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x020 - 0x021	0x020 0x021	TOSR6	0x0000	TOS Priority Control Register 6 [15:0]
0x022 - 0x023	0x022 0x023	TOSR7	0x0000	TOS Priority Control Register 7[15:0]
0x024 - 0x025	0x024 0x025	TOSR8	0x0000	TOS Priority Control Register 8 [15:0]
0x026 - 0x027	0x026 0x027	IADR1	0x0000	Indirect Access Data Register 1 [15:0]
0x028 - 0x029	0x028 0x029	IADR2	0x0000	Indirect Access Data Register 2 [15:0]
0x02A - 0x02B	0x02A 0x02B	IADR3	0x0000	Indirect Access Data Register 3 [15:0]
0x02C - 0x02D	0x02C 0x02D	IADR4	0x0000	Indirect Access Data Register 4 [15:0]
0x02E - 0x02F	0x02E 0x02F	IADR5	0x0000	Indirect Access Data Register 5 [15:0]
0x030 - 0x031	0x030 0x031	IACR	0x0000	Indirect Access Control Register [15:0]
0x032 - 0x033	0x032 0x033	PMCTRL	0x0000	Power Management Control and Wake-up Event Status Register [15:0]
0x034 - 0x035	0x034 0x035	PMEE	0x0000	Power Management Event Enable Register [15:0]
0x036 - 0x037	0x036 0x037	GST	0x008E	Go Sleep Time Register [15:0]
0x038 - 0x039	0x038 0x039	CTPDC	0x0000	Clock Tree Power Down Control Register [15:0]
0x03A - 0x04B	0x03A 0x04B	Reserved (18-Bytes)	Don’t care	None
0x04C - 0x04D	0x04C 0x04D	P1MBCR	0x3120	PHY 1 and MII Basic Control Register [15:0]
0x04E - 0x04F	0x04E 0x04F	P1MBSR	0x7808	PHY 1 and MII Basic Status Register [15:0]
0x050 - 0x051	0x050 0x051	PHY1ILR	0x1430	PHY 1 PHYID Low Register [15:0]
0x052 - 0x053	0x052 0x053	PHY1ILR	0x0022	PHY 1 PHYID High Register [15:0]
0x054 - 0x055	0x054 0x055	P1ANAR	0x05E1	PHY 1 Auto-Negotiation Advertisement Register [15:0]
0x056 - 0x057	0x056 0x057	P1ANLPR	0x0001	PHY 1 Auto-Negotiation Link Partner Ability Register [15:0]
0x058 - 0x059	0x058 0x059	P2MBCR	0x3120	PHY 2 and MII Basic Control Register [15:0]
0x05A - 0x05B	0x05A 0x05B	P2MBSR	0x7808	PHY 2 and MII Basic Status Register [15:0]
0x05C - 0x05D	0x05C 0x05D	PHY2ILR	0x1430	PHY 2 PHYID Low Register [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x05E - 0x05F	0x05D 0x05F	PHY2IHR	0x0022	PHY 2 PHYID High Register [15:0]
0x060 - 0x061	0x060 0x061	P2ANAR	0x05E1	PHY 2 Auto-Negotiation Advertisement Register [15:0]
0x062 - 0x063	0x062 0x063	P2ANLPR	0x0001	PHY 2 Auto-Negotiation Link Partner Ability Register [15:0]
0x064 - 0x065	0x064 0x065	Reserved (2-Bytes)	Don’t care	None
0x066 - 0x067	0x066 0x067	P1PHYCTRL	0x0004	PHY 2 Special Control and Status Register [15:0]
0x068 - 0x069	0x068 0x069	Reserved (2-Bytes)	Don’t care	None
0x06A - 0x06B	0x06A 0x06B	P2PHYCTRL	0x0004	PHY 1 Special Control and Status Register [15:0]
0x06C - 0x06D	0x06C 0x06D	P1CR1	0x0000	Port 1 Control Register 1 [15:0]
0x06E - 0x06F	0x06E 0x06F	P1CR2	0x0607	Port 1 Control Register 2 [15:0]
0x070 - 0x071	0x070 0x071	P1VIDCR	0x0001	Port 1 VID Control Register [15:0]
0x072 - 0x073	0x072 0x073	P1CR3	0x0000	Port 1 Control Register 3 [15:0]
0x074 - 0x075	0x074 0x075	P1IRCR0	0x0000	Port 1 Ingress Rate Control Register 0 [15:0]
0x076 - 0x077	0x076 0x077	P1IRCR1	0x0000	Port 1 Ingress Rate Control Register 1 [15:0]
0x078 - 0x079	0x078 0x079	P1ERCR0	0x0000	Port 1 Egress Rate Control Register 0 [15:0]
0x07A - 0x07B	0x07A 0x07B	P1ERCR1	0x0000	Port 1 Egress Rate Control Register 1 [15:0]
0x07C - 0x07D	0x07C 0x07D	P1SCSLMD	0x0400	Port 1 PHY Special Control/Status, LinkMD® Register [15:0]
0x07E - 0x07F	0x07E 0x07F	P1CR4	0x00FF	Port 1 Control Register 4 [15:0]
0x080 - 0x081	0x080 0x081	P1SR	0x8000	Port 1 Status Register [15:0]
0x082 - 0x083	0x082 0x083	Reserved (2-Bytes)	Don’t Care	None
0x084 - 0x085	0x084 0x085	P2CR1	0x0000	Port 2 Control Register 1 [15:0]
0x086 - 0x087	0x086 0x087	P2CR2	0x0607	Port 2 Control Register 2 [15:0]
0x088 - 0x089	0x088 0x089	P2VIDCR	0x0001	Port 2 VID Control Register [15:0]
0x08A - 0x08B	0x08A 0x08B	P2CR3	0x0000	Port 2 Control Register 3 [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x08C - 0x08D	0x08C 0x08D	P2IRCR0	0x0000	Port 2 Ingress Rate Control Register 0 [15:0]
0x08E - 0x08F	0x08E 0x08F	P2IRCR1	0x0000	Port 2 Ingress Rate Control Register 1 [15:0]
0x090 - 0x091	0x090 0x091	P2ERCR0	0x0000	Port 2 Egress Rate Control Register 0 [15:0]
0x092 - 0x093	0x092 0x093	P2ERCR1	0x0000	Port 2 Egress Rate Control Register 1 [15:0]
0x094 - 0x095	0x094 0x095	P2SCSLMD	0x0400	Port 2 PHY Special Control/Status, LinkMD Register [15:0]
0x096 - 0x097	0x096 0x097	P2CR4	0x00FF	Port 2 Control Register 4 [15:0]
0x098 - 0x099	0x098 0x099	P2SR	0x8000	Port 2 Status Register [15:0]
0x09A - 0x09B	0x09A 0x09B	Reserved (2-Bytes)	Don’t care	None
0x09C - 0x09D	0x09C 0x09D	P3CR1	0x0000	Port 3 Control Register 1 [15:0]
0x09E - 0x09F	0x09E 0x09F	P3CR2	0x0607	Port 3 Control Register 2 [15:0]
0x0A0 - 0x0A1	0x0A0 0x0A1	P3VIDCR	0x0001	Port 3 VID Control Register [15:0]
0x0A2 - 0x0A3	0x0A2 0x0A3	P3CR3	0x0000	Port 3 Control Register 3 [15:0]
0x0A4 - 0x0A5	0x0A4 0x0A5	P3IRCR0	0x0000	Port 3 Ingress Rate Control Register 0 [15:0]
0x0A6 - 0x0A7	0x0A6 0x0A7	P3IRCR1	0x0000	Port 3 Ingress Rate Control Register 1 [15:0]
0x0A8 - 0x0A9	0x0A8 0x0A9	P3ERCR0	0x0000	Port 3 Egress Rate Control Register 0 [15:0]
0x0AA - 0x0AB	0x0AA 0x0AB	P3ERCR1	0x0000	Port 3 Egress Rate Control Register 1 [15:0]
0x0AC - 0x0AD	0x0AC 0x0AD	SGCR8	0x8000	Switch Global Control Register 8 [15:0]
0x0AE - 0x0AF	0x0AE 0x0AF	SGCR9	0x0000	Switch Global Control Register 9 [15:0]
0x0B0 - 0x0B1	0x0B0 0x0B1	SAFMACA1L	0x0000	Source Address Filtering MAC Address 1 Register Low [15:0]
0x0B2 - 0x0B3	0x0B2 0x0B3	SAFMACA1M	0x0000	Source Address Filtering MAC Address 1 Register Middle [15:0]
0x0B4 - 0x0B5	0x0B4 0x0B5	SAFMACA1H	0x0000	Source Address Filtering MAC Address 1 Register High [15:0]
0x0B6 - 0x0B7	0x0B6 0x0B7	SAFMACA2L	0x0000	Source Address Filtering MAC Address 2 Register Low [15:0]
0x0B8 - 0x0B9	0x0B8 0x0B9	SAFMACA2M	0x0000	Source Address Filtering MAC Address 2 Register Middle [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x0BA - 0x0BB	0x0BA 0x0BB	SAFMACA2H	0x0000	Source Address Filtering MAC Address 2 Register High [15:0]
0x0BC - 0x0C7	0x0BC 0x0C7	Reserved (12−Bytes)	Don’t care	None
0x0C8 - 0x0C9	0x0C8 0x0C9	P1TXQRCR1	0x8488	Port 1 TXQ Rate Control Register 1 [15:0]
0x0CA - 0x0CB	0x0CA 0x0CB	P1TXQRCR2	0x8182	Port 1 TXQ Rate Control Register 2 [15:0]
0x0CC - 0x0CD	0x0CC 0x0CD	P2TXQRCR1	0x8488	Port 2 TXQ Rate Control Register 1 [15:0]
0x0CE - 0x0CF	0x0CE 0x0CF	P2TXQRCR2	0x8182	Port 2 TXQ Rate Control Register 2 [15:0]
0x0D0 - 0x0D1	0x0D0 0x0D1	P3TXQRCR1	0x8488	Port 3 TXQ Rate Control Register 1 [15:0]
0x0D2 - 0x0D3	0x0D2 0x0D3	P3TXQRCR2	0x8182	Port 3 TXQ Rate Control Register 2 [15:0]
0x0D4 - 0x0DB	0x0D4 0x0DB	Reserved (8−Bytes)	Don’t Care	None
0x0DC - 0x0DD	0x0DC 0x0DD	P1ANPT	0x2001	Port 1 Auto-Negotiation Next Page Transmit Register [15:0]
0x0DE - 0x0DF	0x0DE 0x0DF	P1ALPRNP	0x0000	Port 1 Auto-Negotiation Link Partner Received Next Page Register [15:0]
0x0E0 - 0x0E1	0x0E0 0x0E1	P1EEEA	0x0002	Port 1 EEE and Link Partner Advertisement Register [15:0]
0x0E2 - 0x0E3	0x0E2 0x0E3	P1EEEWEC	0x0000	Port 1 EEE Wake Error Count Register [15:0]
0x0E4 - 0x0E5	0x0E4 0x0E5	P1EEECS	0x8064	Port 1 EEE Control/Status and Auto-Negotiation Expansion Register [15:0]
0x0E6 - 0x0E7	0x0E6 0x0E7	P1LPIRTC BL2LPIC1	0x27 0x08	Port 1 LPI Recovery Time Counter Register [7:0] Buffer Load to LPI Control 1 Register [7:0]
0x0E8 - 0x0E9	0x0E8 0x0E9	P2ANPT	0x2001	Port 2 Auto-Negotiation Next Page Transmit Register [15:0]
0x0EA - 0x0EB	0x0EA 0x0EB	P2ALPRNP	0x0000	Port 2 Auto-Negotiation Link Partner Received Next Page Register [15:0]

TABLE 4-2: INTERNAL I/O REGISTER SPACE MAPPING FOR SWITCH CONTROL AND CONFIGURATION (0X000 - 0X0FF) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x0EC - 0x0ED	0x0EC 0x0ED	P2EEEA	0x0002	Port 2 EEE and Link Partner Advertisement Register [15:0]
0x0EE - 0x0EF	0x0EE 0x0EF	P2EEEWEC	0x0000	Port 2 EEE Wake Error Count Register [15:0]
0x0F0 - 0x0F1	0x0F0 0x0F1	P2EEECS	0x8064	Port 2 EEE Control/Status and Auto-Negotiation Expansion Register [15:0]
0x0F2 - 0x0F3	0x0F2 0x0F3	P2LPIRTC PCSEEEC	0x27 0x03	Port 2 LPI Recovery Time Counter Register [7:0] PCS EEE Control Register [7:0]
0x0F4 - 0x0F5	0x0F4 0x0F5	ETLWTC	0x03E8	Empty TXQ to LPI Wait Time Control Register [15:0]
0x0F6 - 0x0F7	0x0F6 0x0F7	BL2LPIC2	0xC040	Buffer Load to LPI Control 2 Register [15:0]
0x0F8 - 0x0FF	0x0F8 0x0FF	Reserved (8−Bytes)	Don’t Care	None

TABLE 4-3: INTERNAL I/O REGISTER SPACE MAPPING FOR HOST INTERFACE UNIT (0X100 - 0X16F)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x100 - 0x107	0x100 0x107	Reserved (8-Bytes)	Don't Care	None
0x108 - 0x109	0x108 0x109	CCR	Read Only	Chip Configuration Register [15:0]
0x10A - 0x10F	0x10A 0x10F	Reserved (6-Bytes)	Don't Care	None
0x110 - 0x111	0x110 0x111	MARL	—	MAC Address Register Low [15:0]
0x112 - 0x113	0x112 0x113	MARM	—	MAC Address Register Middle [15:0]
0x114 - 0x115	0x114 0x115	MARH	—	MAC Address Register High [15:0]
0x116 - 0x121	0x116 0x121	Reserved (12-Bytes)	Don't Care	None
0x122 - 0x123	0x122 0x123	EEPCR	0x0000	EEPROM Control Register [15:0]
0x124 - 0x125	0x124 0x125	MBIR	0x0000	Memory BIST Info Register [15:0]
0x126 - 0x127	0x126 0x127	GRR	0x0000	Global Reset Register [15:0]
0x128 - 0x129	0x128 0x129	Reserved (2-Bytes)	Don't Care	None
0x12A - 0x12B	0x12A 0x12B	WFCR	0x0000	Wake-Up Frame Control Register [15:0]
0x12C - 0x12F	0x12C 0x12F	Reserved (4-Bytes)	Don't Care	None
0x130 - 0x131	0x130 0x131	WF0CRC0	0x0000	Wake-Up Frame 0 CRC0 Register [15:0]
0x132 - 0x133	0x132 0x133	WF0CRC1	0x0000	Wake-Up Frame 0 CRC1 Register [15:0]
0x134 - 0x135	0x134 0x135	WF0BM0	0x0000	Wake-Up Frame 0 Byte Mask 0 Register [15:0]
0x136 - 0x137	0x136 0x137	WF0BM1	0x0000	Wake-Up Frame 0 Byte Mask 1 Register [15:0]
0x138 - 0x139	0x138 0x139	WF0BM2	0x0000	Wake-Up Frame 0 Byte Mask 2 Register [15:0]
0x13A - 0x13B	0x13A 0x13B	WF0BM3	0x0000	Wake-Up Frame 0 Byte Mask 3 Register [15:0]
0x13C - 0x13F	0x13C 0x13F	Reserved (4-Bytes)	Don't Care	None
0x140 - 0x141	0x140 0x141	WF1CRC0	0x0000	Wake-Up Frame 1 CRC0 Register [15:0]
0x142 - 0x143	0x142 0x143	WF1CRC1	0x0000	Wake-Up Frame 1 CRC1 Register [15:0]
0x144 - 0x145	0x144 0x145	WF1BM0	0x0000	Wake-Up Frame 1 Byte Mask 0 Register [15:0]

TABLE 4-3: INTERNAL I/O REGISTER SPACE MAPPING FOR HOST INTERFACE UNIT (0X100 - 0X16F) (CONTINUED)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x146 - 0x147	0x146 0x147	WF1BM1	0x0000	Wake-Up Frame 1 Byte Mask 1 Register [15:0]
0x148 - 0x149	0x148 0x149	WF1BM2	0x0000	Wake-Up Frame 1 Byte Mask 2 Register [15:0]
0x14A - 0x14B	0x14A 0x14B	WF1BM3	0x0000	Wake-Up Frame 1 Byte Mask 3 Register [15:0]
0x14C - 0x14F	0x14C 0x14F	Reserved (4-Bytes)	Don’t Care	None
0x150 - 0x151	0x150 0x151	WF2CRC0	0x0000	Wake-Up Frame 2 CRC0 Register [15:0]
0x152 - 0x153	0x152 0x153	WF2CRC1	0x0000	Wake-Up Frame 2 CRC1 Register [15:0]
0x154 - 0x155	0x154 0x155	WF2BM0	0x0000	Wake-Up Frame 2 Byte Mask 0 Register [15:0]
0x156 - 0x157	0x156 0x157	WF2BM1	0x0000	Wake-Up Frame 2 Byte Mask 1 Register [15:0]
0x158 - 0x159	0x158 0x159	WF2BM2	0x0000	Wake-Up Frame 2 Byte Mask 2 Register [15:0]
0x15A - 0x15B	0x15A 0x15B	WF2BM3	0x0000	Wake-Up Frame 2 Byte Mask 3 Register [15:0]
0x15C - 0x15F	0x15C 0x15F	Reserved (4-Bytes)	Don’t Care	None
0x160 - 0x161	0x160 0x161	WF3CRC0	0x0000	Wake-Up Frame 3 CRC0 Register [15:0]
0x162 - 0x163	0x162 0x163	WF3CRC1	0x0000	Wake-Up Frame 3 CRC1 Register [15:0]
0x164 - 0x165	0x164 0x165	WF3BM0	0x0000	Wake-Up Frame 3 Byte Mask 0 Register [15:0]
0x166 - 0x167	0x166 0x167	WF3BM1	0x0000	Wake-Up Frame 3 Byte Mask 1 Register [15:0]
0x168 - 0x169	0x168 0x169	WF3BM2	0x0000	Wake-Up Frame 3 Byte Mask 2 Register [15:0]
0x16A - 0x16B	0x16A 0x16B	WF3BM3	0x0000	Wake-Up Frame 3 Byte Mask 3 Register [15:0]
0x16C - 0x16F	0x16C 0x16F	Reserved (4-Bytes)	Don’t Care	None

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR THE QMU (0X170 - 0X1FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x170 - 0x171	0x170 0x171	TXCR	0x0000	Transmit Control Register [15:0]
0x172 - 0x173	0x172 0x173	TXCR	0x0000	Transmit Status Register [15:0]
0x174 - 0x175	0x174 0x175	RXCR1	0x0800	Receive Control Register 1 [15:0]
0x176 - 0x177	0x176 0x177	RXCR1	0x0114	Receive Control Register 2 [15:0]
0x178 - 0x179	0x178 0x179	TXMIR	0x1800	TXQ Memory Information Register [15:0]
0x17A - 0x17B	0x17A 0x17B	Reserved	Don't Care	None
0x17C - 0x17D	0x17C 0x17D	RXFHSR	0x0000	Receive Frame Header Status Register [15:0]
0x17E - 0x17F	0x17E 0x17F	RXFHBCR	0x0000	Receive Frame Header Byte Count Register [15:0]
0x180 - 0x181	0x180 0x181	TXQCR	0x0000	TXQ Command Register [15:0]
0x182 - 0x183	0x182 0x183	RXQCR	0x0000	RXQ Command Register [15:0]
0x184 - 0x185	0x184 0x185	TXFDPR	0x0000	TX Frame Data Pointer Register [15:0]
0x186 - 0x187	0x186 0x187	RXFDPR	—	RX Frame Data Pointer Register [15:0]
0x188 - 0x18B	0x188 0x18B	Reserved (4-Bytes)	Don't Care	None
0x18C - 0x18D	0x18C 0x18D	RXDTTR	0x0000	RX Duration Timer Threshold Register [15:0]
0x18E - 0x18F	0x18E 0x18F	RXDBCTR	0x0000	RX Data Byte Count Threshold Register [15:0]
0x190 - 0x191	0x190 0x191	IER	0x0000	Interrupt Enable Register [15:0]
0x192 - 0x193	0x192 0x193	ISR	0x0000	Interrupt Status Register [15:0]
0x194 - 0x19B	0x194 0x19B	Reserved (8-Bytes)	Don't Care	None
0x19C - 0x19D	0x19C 0x19D	RXFCTR	0x0000	RX Frame Count Threshold Register [7:0], 15:8 are Reserved
0x19E - 0x19F	0x19E 0x19F	TXNTFSR	0x0000	TX Next Total Frames Size Register [15:0]
0x1A0 - 0x1A1	0x1A0 0x1A1	MAHTR0	0x0000	MAC Address Hash Table Register 0 [15:0]
0x1A2 - 0x1A3	0x1A2 0x1A3	MAHTR1	0x0000	MAC Address Hash Table Register 1 [15:0]
0x1A4 - 0x1A5	0x1A4 0x1A5	MAHTR2	0x0000	MAC Address Hash Table Register 2 [15:0]
0x1A6 - 0x1A7	0x1A6 0x1A7	MAHTR3	0x0000	MAC Address Hash Table Register 3 [15:0]

TABLE 4-4: INTERNAL I/O REGISTER SPACE MAPPING FOR THE QMU (0X170 - 0X1FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x1A8 - 0x1AF	0x1A8 0x1AF	Reserved (8-Bytes)	Don't Care	None
0x1B0 - 0x1B1	0x1B0 0x1B1	FCLWR	0x0600	Flow Control Low Water Mark Register [15:0]
0x1B2 - 0x1B3	0x1B2 0x1B3	FCHWR	0x0400	Flow Control High Water Mark Register [15:0]
0x1B4 - 0x1B5	0x1B4 0x1B5	FCOWR	0x0400	Flow Control Overrun Water Mark Register [15:0]
0x1B6 - 0x1B7	0x1B6 0x1B7	Reserved (8-Bytes)	Don't Care	None
0x1B8 - 0x1B9	0x1B8 0x1B9	RXFC	0x0000	RX Frame Count[15:8], Reserved [7:0]
0x1BA - 0x1FF	0x1BA 0x1FF	Reserved (70-Bytes)	Don't Care	None

TABLE 4-5: SPECIAL CONTROL REGISTERS (0X700 - 0X7FF)

I/O Register Offset Location		Register Name	Default Value	Description
16-Bit	8-Bit			
0x700 - 0x747	0x700 0x747	Reserved (72-Bytes)	Don't Care	None
0x748 - 0x749	0x748 0x749	ANA_CNTRL_1	0x0000	Analog Control 1 Register
0x74A - 0x74B	0x74A 0x749B	Reserved (2-Bytes)	Don't Care	None
0x74C - 0x74D	0x74C 0x74D	ANA_CNTRL_3	0x0000	Analog Control 3 Register
0x74E - 0x7FF	0x74E 0x7FF	Reserved (178-Bytes)	Don't Care	None

4.3 Register Bit Definitions

The section provides details of the bit definitions for the registers summarized in the previous section. Writing to a bit or register defined as reserved could potentially cause unpredictable results. If it is necessary to write to registers which contain both writable and reserved bits in the same register, the user should first read back the reserved bits (RO or RW), then "OR" the desired settable bits with the value read and write back the "ORed" value back to the register.

Bit Type Definition:

RO = Read only

WO = Write only

RW = Read/Write

SC = Self-Clear

W1C = Write "1" to Clear (Write a "1" to clear this bit)

Internal I/O Register Mapping for Switch Control and Configuration (0x000 - 0x0FF)

This register contains the chip ID and switch-enable control.

TABLE 4-6: CHIP ID AND ENABLE REGISTER (0X00 - 0X001): CIDER

Bit	Default Value	R/W	Description
15-8	0x84	RO	**Family ID** Chip family ID.
7-4	0x3	RO	**Chip ID** 0x3 is assigned to the KSZ8852HL.
3-1	001	RO	**Revision ID** Chip revision ID.
0	1	RW	**Start Switch** 1 = Start the chip. 0 = Switch is disabled.

Switch Global Control Register 1 (0x002 - 0x003): SGCR1

This register contains global control bits for the switch function.

TABLE 4-7: SWITCH GLOBAL CONTROL REGISTER 1 (0X002 - 0X003): SGCR1

Bit	Default	R/W	Description
15	0	RW	**Pass All Frames** 1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with Sniffer mode only.
14	0	RW	**Receive 2000 Byte Packet Length Enable** 1 = Enables the receipt of packets up to and including 2000 bytes in length. 0 = Discards the received packets if their length is greater than 2000 bytes.
13	1	RW	**IEEE 802.3x Transmit Direction Flow Control Enable** 1 = Enables transmit direction flow control feature. 0 = Disable transmit direction flow control feature. The switch will not generate any flow control packets.
12	1	RW	I**EEE 802.3x Receive Direction Flow Control Enable** 1 = Enables receive direction flow control feature. 0 = Disable receive direction flow control feature. The switch will not react to any received flow control packets.
11	0	RW	**Frame Length Field Check** 1 = Enable checking frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500). 0 = Disable checking frame length field in the IEEE packets.
10	1	RW	**Aging Enable** 1 = Enable aging function in the chip. 0 = Disable aging function in the chip.
9	0	RW	**Fast Age Enable** 1 = Turn on fast aging (800 µs).
8	0	RW	**Aggressive Back-Off Enable** 1 = Enable more aggressive back-off algorithm in half-duplex mode to enhance performance. This is not an IEEE standard.
7-6	01	RW	**Reserved**
5	0	RW	**Enable Flow Control when Exceeding Ingress Limit** 1 = Flow control frame will be sent to link partner when exceeding the ingress rate limit. 0 = Frame will be dropped when exceeding the ingress rate limit.

TABLE 4-7: SWITCH GLOBAL CONTROL REGISTER 1 (0X002 - 0X003): SGCR1 (CONTINUED)

Bit	Default	R/W	Description
4	1	RW	**Receive 2K Byte Packets Enable** 1 = Enable packet length up to 2K bytes. While set, SGCR2 bits[2,1] will have no effect. 0 = Discard packet if packet length is greater than 2000 bytes.
3	0	RW	**Pass Flow Control Packet** 1 = Switch will not filter 802.1x “flow control” packets.
2-1	00	RW	**Reserved**
0	0	RW	**Link Change Age** 1 = Link change from “link” to “no link” will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 + 75 seconds). Note: If any port is unplugged, all addresses will be automatically aged out.

Switch Global Control Register 2 (0x004 – 0x005): SGCR2

This register contains global control bits for the switch function.

TABLE 4-8: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 - 0X005): SGCR2

Bit	Default	R/W	Description
15	0	RW	**802.1Q VLAN Enable** 1 = 802.1Q VLAN mode is turned on. VLAN table must be set up before the operation. 0 = 802.1Q VLAN is disabled.
14	0	RW	**IGMP Snoop Enable** 1 = IGMP snoop is enabled. 0 = IGMP snoop is disabled.
13	0	RW	**IPv6 MLD Snooping Enable** 1 = Enable IPv6 MLD snooping.
12	0	RW	**IPv6 MLD Snooping Option** 1 = Enable IPv6 MLD snooping option.
11-9	000	RW	**Reserved**
8	0	RW	**Sniff Mode Select** 1 = Performs RX and TX sniff (both the source port and destination port need to match). 0 = Performs RX or TX sniff (either the source port or destination port needs to match). This is the mode used to implement RX only sniff.
7	1	RW	**Unicast Port-VLAN Mismatch Discard** 1 = No packets can cross the VLAN boundary. 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross the VLAN boundary.
6	1	RW	**Multicast Storm Protection Disable** 1 = “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets are regulated. 0 = “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = “1” packets.
5	1	RW	**Back Pressure Mode** 1 = Carrier sense-based back pressure is selected. 0 = Collision-based back pressure is selected.

TABLE 4-8: SWITCH GLOBAL CONTROL REGISTER 2 (0X004 - 0X005): SGCR2

Bit	Default	R/W	Description
4	1	RW	**Flow Control and Back Pressure Fair Mode** 1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This prevents the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port is flow controlled. This may not be “fair” to the flow control port.
3	0	RW	**No Excessive Collision Drop** 1 = The switch does not drop packets when 16 or more collisions occur. 0 = The switch drops packets when 16 or more collisions occur.
2	0	RW	**Huge Packet Support** 1 = Accepts packet sizes up to 1916 bytes (inclusive). This bit setting overrides setting from bit 1 of the same register. 0 = The max packet size is determined by bit [1] of this register.
1	0	RW	**Legal Maximum Packet Size Check Enable** 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value are dropped. 0 = Accepts packet sizes up to 1536 bytes (inclusive).
0	0	RW	**Priority Buffer Reserve** 1 = Each port is pre-allocated 48 buffers, used exclusively for high priority (q3, q2, and q1) packets. Effective only when the multiple queue feature is turned on. 0 = Each port is pre-allocated 48 buffers used for all priority packets (q3, q2, q1, and q0).

Switch Global Control Register 3 (0x006 - 0x007): SGCR3

This register contains global control bits for the switch function.

TABLE 4-9: SWITCH GLOBAL CONTROL REGISTER 3 (0X006 - 0X007): SGCR3

Bit	Default	R/W	Description
15 - 8	0x63	RW	**Broadcast Storm Protection Rate Bit [7:0]** These bits, along with SGCR3[2:0], determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%.
7	0	RO	**Reserved**
6	0	RW	**Switch Host Port in Half-Duplex Mode** 1 = Enable host port interface half-duplex mode. 0 = Enable host port interface full-duplex mode.
5	1	RW	**Switch Host Port Flow Control Enable** 1 = Enable full-duplex flow control on Switch Host port. 0 = Disable full-duplex flow control on Switch Host port
4	0	RW	**Switch MII 10BT** 1 = The Switch is in 10 Mbps mode. 0 = The Switch is in 100 Mbps mode.
3	0	RW	**Null VID Replacement** 1 = Replaces NULL VID with port VID (12 bits). 0 = No replacement for NULL VID.

TABLE 4-9: SWITCH GLOBAL CONTROL REGISTER 3 (0X006 - 0X007): SGCR3

Bit	Default	R/W	Description
2 - 0	000	RW	**Broadcast Storm Protection Rate Bit [10:8]** These bits, along with SGCR3[15:8] determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%. Broadcast storm protection rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx. 0x63)

0x008 – 0x00B: Reserved

Switch Global Control Register 6 (0x00C - 0x00D): SGCR6

This register contains global control bits for the switch function.

TABLE 4-10: SWITCH GLOBAL CONTROL REGISTER 6 (0X00C – 0X00D): SGCR6

Bit	Default	R/W	Description
15 - 14	11	R/W	**Tag_0x7** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x7.
13 - 12	11	R/W	**Tag_0x6** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x6.
11 - 10	10	R/W	**Tag_0x5** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x5.
9 - 8	10	R/W	**Tag_0x4** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x4.
7 - 6	01	R/W	**Tag_0x3** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x3.
5 - 4	01	R/W	**Tag_0x2** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x2.
3 - 2	00	R/W	**Tag_0x1** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x1.
1 - 0	00	R/W	**Tag_0x0** IEEE 802.1p mapping. The value in this field is used as the frame's priority when its VLAN Tag has a value of 0x0.

Switch Global Control Register 7 (0x00E - 0x00F): SGCR7

This register contains global control bits for the switch function.

TABLE 4-11: SWITCH GLOBAL CONTROL REGISTER 7 (0X00E - 0X00F): SGCR7

Bit	Default	R/W	Description
15 - 10	0x02	R/W	**Reserved**
9 - 8	00	R/W	**QMU Module Soft Reset** 1: Software reset is active to clear both TXQ and RXQ memories. 0: Software reset is inactive. QMU software reset will flush out all TX/RX packet data inside the TXQ and RXQ memories and reset all QMU registers to default value.
			LED Mode / P1/2LED1 / P1/2LED0 00 / Speed / Link & Activity 01 / Activity / Link 10 / Full-Duplex / Link & Activity 11 / Full-Duplex / Link
7	0	R/W	**Unknown Default Port Enable** Send packets with unknown destination address to specified ports in bits [2:0]. 1 = Enable to send unknown DA packet.
6 - 5	01 or 10	R/W	**Driver Strength Selection** These two bits determine the drive strength of all I/O pins except for the following category of pins: LED pins, INTRN, and RSTN. 00 = 4 mA. 01 = 8 mA. (Default when VDD_IO is 3.3V or 2.5V) 10 = 12 mA. (Default when VDD_IO is 1.8V) 11 = 16 mA.
4 - 3	00	R/W	**Reserved**
2 - 0	111	R/W	**Unknown Packet Default Port(s)** Specify which ports to send packets with unknown destination addresses. Feature is enabled by bit [7]. Bit[2] = For Port 3 (host port). Bit[1] = For Port 2. Bit[0] = For Port 1.

MAC Address Register 1 (0x010 - 0x011): MACAR1

This register contains the expected CRC values of the Wake up frame 0 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-12: MAC ADDRESS REGISTER 1 (0X010 - 0X011): MACAR1

Bit	Default	R/W	Description
15 - 0	0x0010	RW	**MACA[47:32]** Specifies MAC Address 1 for sending PAUSE frame.

MAC Address Register 2 (0x012 - 0x013): MACAR2

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frames.

TABLE 4-13: MAC ADDRESS REGISTER 2 (0X012 - 0X013): MACAR2

Bit	Default	R/W	Description
15 - 0	0xA1FF	RW	**MACA[31:16]** Specifies MAC Address 2 for sending PAUSE frame.

MAC Address Register 3 (0x014 - 0x015): MACAR3

This register contains the two LSBs of the MAC address for the switch function. This MAC address is used for sending PAUSE frames.

TABLE 4-14: MAC ADDRESS REGISTER 3 (0X014 - 0X015): MACAR3

Bit	Default	R/W	Description
15 - 0	0xFFFF	RW	**MACA[15:0]** Specifies MAC Address 3 for sending PAUSE frame.

TABLE 4-15: WAKEUP FRAME 2 BYTE MASK 3 REGISTER (0X5A – 0X5B): WF2BM3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2BM3** Wake-up frame 2 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 2 pattern.

4.4 Type-of-Service (TOS) Priority Control Registers

TOS Priority Control Register 1 (0x016-0x017): TOSR1

The IPv4/IPv6 type-of-service (TOS) priority control registers are used to define a 2-bit priority to each of the 64 possible values in the 6-bit differentiated services code point (DSCP) field in the IP header of ingress frames.

This register contains the TOS priority control bits for the switch function.

TABLE 4-16: TOS PRIORITY CONTROL REGISTER 1 (0X016-0X017): TOSR1

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[15:14]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x1c.
13−12	00	R/W	**DSCP[13:12]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x18.
11−10	00	R/W	**DSCP[11:10]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x14.
9−8	00	R/W	**DSCP[9:8]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x10.
7−6	00	R/W	**DSCP[7:6**] The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x0c.
5−4	00	R/W	**DSCP[5:4]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x08.
3−2	00	R/W	**DSCP[3:2]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x04.
1−0	00	R/W	**DSCP[1:0]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x00.

TOS Priority Control Register 2 (0x018 - 0x019): TOSR2

This register contains the TOS priority control bits for the switch function.

TABLE 4-17: TOS PRIORITY CONTROL REGISTER 2 (0X018-0X018): TOSR2

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[31:30]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x3c.
13−12	00	R/W	**DSCP[29:28]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x38.
11−10	00	R/W	**DSCP[27:26]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x34.
9−8	00	R/W	**DSCP[25:24]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x30.
7−6	00	R/W	**DSCP[23:22]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x2c.
5−4	00	R/W	**DSCP[21:20]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x28.
3−2	00	R/W	**DSCP[19:18]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x24.
1−0	00	R/W	**DSCP[17:16]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x20.

TOS Priority Control Register 3 (0x01A - 0x01B): TOSR3

This register contains the TOS priority control bits for the switch function.

TABLE 4-18: TOS PRIORITY CONTROL REGISTER 3 (0X01A - 0X01B): TOSR3

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[47:46]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x5c.
13−12	00	R/W	**DSCP[45:44]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x58.
11−10	00	R/W	**DSCP[43:42]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x54.
9−8	00	R/W	**DSCP[41:40]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x50.
7−6	00	R/W	**DSCP[39:38]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x4c.
5−4	00	R/W	**DSCP[37:36]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x48.

TABLE 4-18: TOS PRIORITY CONTROL REGISTER 3 (0X01A - 0X01B): TOSR3 (CONTINUED)

Bit	Default	R/W	Description
3−2	00	R/W	**DSCP[35:34]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x44.
1−0	00	R/W	**DSCP[33:32]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x40.

TOS Priority Control Register 4 (0x01C - 0x1D): TOSR4

This register contains the TOS priority control bits for the switch function.

TABLE 4-19: TOS PRIORITY CONTROL REGISTER 4 (0X01C - 0X1D): TOSR4

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[63:62]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x7c.
13−12	00	R/W	**DSCP[61:60]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x78.
11−10	00	R/W	**DSCP[59:58]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x74.
9−8	00	R/W	**DSCP[57:56]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x70.
7−6	00	R/W	**DSCP[55:54]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x6c.
5−4	00	R/W	**DSCP[53:52]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x68.
3−2	00	R/W	**DSCP[51:50]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x64.
1−0	00	R/W	**DSCP[49:48]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x60.

TOS Priority Control Register 5 (0x01E - 0x1F): TOSR5

This register contains the TOS priority control bits for the switch function.

TABLE 4-20: TOS PRIORITY CONTROL REGISTER 5 (0X01E - 0X1F): TOSR5

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[79:78]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x9c.
13−12	00	R/W	**DSCP[77:76]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x98.
11−10	00	R/W	**DSCP[75:74]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x94.
9−8	00	R/W	**DSCP[73:72]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x90.
7−6	00	R/W	**DSCP[71:70]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x8c.
5−4	00	R/W	**DSCP[69:68]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x88.
3−2	00	R/W	**DSCP[67:66]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x84.
1−0	00	R/W	**DSCP[65:64]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x80.

TOS Priority Control Register 6 (0x020 - 0x021): TOSR6

This register contains the TOS priority control bits for the switch function.

TABLE 4-21: TOS PRIORITY CONTROL REGISTER 6 (0X020 - 0X021): TOSR6

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[95:94]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value is 0xbc.
13−12	00	R/W	**DSCP[93:92]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb8.
11−10	00	R/W	**DSCP[91:90]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb4.
9−8	00	R/W	**DSCP[89:88]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb0.
7−6	00	R/W	**DSCP[87:86]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xac.
5−4	00	R/W	**DSCP[85:84]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa8.
3−2	00	R/W	**DSCP[83:82]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa4.
1−0	00	R/W	**DSCP[81:80]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa0.

TOS Priority Control Register 7 (0x022 - 0x023): TOSR7

This register contains the TOS priority control bits for the switch function.

TABLE 4-22: TOS PRIORITY CONTROL REGISTER 7 (0X022 - 0X023): TOSR7

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[111:110]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xdc.
13−12	00	R/W	**DSCP[109:108]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd8.
11−10	00	R/W	**DSCP[107:106]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd4.
9−8	00	R/W	**DSCP[105:104]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd0.
7−6	00	R/W	**DSCP[103:102]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xcc.
5−4	00	R/W	**DSCP[101:100]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc8.
3−2	00	R/W	**DSCP[99:98]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc4.
1−0	00	R/W	**DSCP[97:96]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc0.

TOS Priority Control Register 7 (0x024 - 0x025): TOSR8

This register contains the TOS priority control bits for the switch function.

TABLE 4-23: TOS PRIORITY CONTROL REGISTER 7 (0X024 - 0X025): TOSR8

Bit	Default	R/W	Description
15−14	00	RW	**DSCP[127:126]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xfc.
13−12	00	R/W	**DSCP[125:124]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf8.
11−10	00	R/W	**DSCP[123:122]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf4.
9−8	00	R/W	**DSCP[121:120]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf0.
7−6	00	R/W	**DSCP[119:118]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xec.
5−4	00	R/W	**DSCP[117:116]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe8.
3−2	00	R/W	**DSCP[115:114]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe4.
1−0	00	R/W	**DSCP[113:112]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe0.

4.5 Indirect Access Data Registers

Indirect Access Data Register 1 (0x026 - 0x027): IADR1

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table.

TABLE 4-24: INDIRECT ACCESS DATA REGISTER 1 (0X026 - 0X027): IADR1

Bit	Default	R/W	Description
15 - 8	0x00	RO	**Reserved**
7	0	RO	**CPU Read Status** Only for dynamic and statistics counter reads. 1 = Read is still in progress. 0 = Read has completed.
6 - 3	0x0	RO	**Reserved**
2 - 0	000	RO	**Indirect Data [66:64]** Bits [66:64] of indirect data.

Indirect Access Data Register 2 (0x028 - 0x029): IADR2

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table.

TABLE 4-25: INDIRECT ACCESS DATA REGISTER 2 (0X028 - 0X029): IADR2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Indirect Data [47:32]** Bits [47:32] of indirect data.

Indirect Access Data Register 3 (0x02A - 0x02B): IADR3

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table.

TABLE 4-26: INDIRECT ACCESS DATA REGISTER 3 (0X02A - 0X02B): IADR3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Indirect Data [63:48]** Bits [63:48] of indirect data.

Indirect Access Data Register 4 (0x02C - 0x02D): IADR4

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table.

TABLE 4-27: INDIRECT ACCESS DATA REGISTER 4 (0X02C - 0X02D): IADR4

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Indirect Data [15:0]** Bits [15:0] of indirect data.

Indirect Access Data Register 5 (0x02E - 0x02F): IADR5

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table.

TABLE 4-28: INDIRECT ACCESS DATA REGISTER 5 (0X02E - 0X02F): IADR5

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Indirect Data [31:16]** Bits [31:16] of indirect data.

Indirect Access Control Register (0x030 - 0x031): IACR

This register is used to indirectly read or write the data in the Management Information Base (MIB) Counters, Static MAC Address Table, Dynamic MAC Address Table, or the VLAN Table. Writing to IACR triggers a command. Read or write access is determined by register bit [12].

TABLE 4-29: INDIRECT ACCESS CONTROL REGISTER (0X030 - 0X031): IACR

Bit	Default	R/W	Description
15 - 13	000	RW	**Reserved**
12	0	RW	**Read or Write Access Selection** 1 = Read cycle. 0 = Write cycle.
11 - 10	00	RW	**Table Select** 00 = Static MAC address table selected. 01 = VLAN table selected. 10 = Dynamic MAC address table selected. 11 = MIB counter selected.

TABLE 4-29: INDIRECT ACCESS CONTROL REGISTER (0X030 - 0X031): IACR (CONTINUED)

Bit	Default	R/W	Description
9 - 0	0x000	RW	**Indirect Address [9:0]** Bits [9:0] of indirect address.

4.6 Power Management Control and Wake-Up Event Status

Power Management Control and Wake-Up Event Status (0x032 – 0x033): PMCTRL

This register controls the power management mode and provides Wake-Up event status.

TABLE 4-30: POWER MANAGEMENT CONTROL AND WAKE-UP EVENT STATUS (0X032 – 0X033): PMCTRL

Bit	Default	R/W	Description
15 - 6	0x000	RO	**Reserved**
5	0	RW (W1C)	**Wake-Up Frame Detect Status** 1 = A wake-up frame has been detected at the host QMU (Write a “1” to clear). 0 = No wake-up frame has been detected.
4	0	RW (W1C)	**Magic Packet Detect Status** 1 = A Magic Packet has been detected at either Port 1 or Port 2 (Write a “1” to clear). 0 = No Magic Packet has been detected.
3	0	RW (W1C)	**Link-Up Detect Status** 1 = Link-up has been detected at either Port 1 or Port 2 (Write a “1” to clear). 0 = No link-up has been detected.
2	0	RW (W1C)	**Energy Detect Status** 1 = Energy is detected at either Port 1 or Port 2 (Write a “1” to clear). 0 = No energy is detected.
1 - 0	00	RW	**Power Management Mode** These two bits are used to control device power management mode. 00 = Normal mode. 01 = Energy detect mode. 10 = Global soft power-down mode. 11 = Reserved. Write “0001” to PMECR[5:2] to clear this bit.

Power Management Event Enable Register (0x034 - 0x035): PMEE

This register contains the power management event enable control bits.

TABLE 4-31: POWER MANAGEMENT EVENT ENABLE REGISTER (0X034 - 0X035): PMEE

Bit	Default	R/W	Description
15 - 5	0x000	RW	**Reserved**
4	0	RW	**PME Polarity** 1 = The PME pin is active high. 0 = The PME pin is active low.
3	0	RW	**PME Waked Up By Wake-Up Frame Enable** 1 = The PME pin will be asserted when a wake-up frame is detected. 0 = PME won’t be asserted by the wake-up frame detection.
2	0	RW	**PME Waked Up By Magic Packet Enable** 1 = The PME pin will be asserted when a magic packet is detected. 0 = PME won’t be asserted by the magic packet detection.
1	0	RW	**PME Waked Up By Link-Up Enable** 1 = The PME pin will be asserted when a link-up is detected at Port 1 or Port 2. 0 = PME won’t be asserted by the link-up detection.

TABLE 4-31: POWER MANAGEMENT EVENT ENABLE REGISTER (0X034 - 0X035): PMEE

Bit	Default	R/W	Description
0	0	RW	**PME Waked Up By Energy Detect Enable** 1 = The PME pin will be asserted when energy on line is detected at Port 1 or Port 2. 0 = PME won't be asserted by the energy detection.

4.7 Go Sleep Time and Clock Tree Power-Down Control Registers

This register contains the value which is used to control the minimum go-sleep time period when the device transitions from normal power state to low power state in energy detect mode.

TABLE 4-32: GO SLEEP TIME REGISTER (0X036 - 0X037): GST

Bit	Default	R/W	Description
15 - 8	0x00	RO	**Reserved**
7 - 0	0x8E	RW	**Go Sleep Time** This value is used to control the minimum period the no-energy event has to be detected consecutively before the device enters the low power state during energy detect mode. The unit is 20 ms. The default go sleep time is around 3.0 seconds.

Clock Tree Power-Down Control Register (0x038 - 0x039): CTPDC

This register contains the power down control bits for all clocks.

TABLE 4-33: CLOCK TREE POWER-DOWN CONTROL REGISTER (0X038 - 0X039): CTPDC

Bit	Default	R/W	Description
15 - 5	0x000	RO	**Reserved**
4	0	RW	**Reserved**
3	0	RW	**Switch Clock Auto Shut Down Enable** 1 = When no packet transfer is detected on the MII interface of all ports (Port 1, Port 2, and Port 3) longer than the time specified in bit[1:0] of current register, the device will shut down the switch clock automatically. The switch clock will be woken up automatically when the MII interface on any port becomes busy. 0 = Switch clock is always on.
2	0	RW	**CPU Clock Auto Shut Down Enable** 1 = When no packet transfer is detected on either the host interface or the MII interface of all ports (Port 1, Port 2, and Port 3) for a time period longer than the time specified in bit[1:0] of current register, the device will shut down the CPU clock automatically. The CPU clock will be woken up automatically when host activity is detected or the MII interface of any port becomes busy. 0 = CPU clock is always on.
1 - 0	00	RW	**Shutdown Wait Period** These two bits specify the time for device to monitor host/MII activity continuously before it could shut down switch or CPU clock. 00 = 5.3 second. 01 = 1.6 second. 10 = 1 ms. 11 = 3.2 µs.

0x03A – 0x04B: Reserved

4.8 PHY and MII Basic Control Registers

PHY 1 MII-Register Basic Control Register (0x04C – 0x04D): P1MBCR

This register contains Media Independent Interface (MII) control bits for the switch Port 1 function as defined in the IEEE 802.3 specification.

TABLE 4-34: PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0XE4 – 0XE5): P1MBCR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Reserved**	—
14	0	RW	**Far-End Loopback** 1 = Perform loopback as follows: Start: RXP2/RXM2 (Port 2) Loop back: PMD/PMA of Port 1's PHY End: TXP2/TXM2 (Port 2) 0 = Normal operation.	Bit [8] in P1CR4
13	1	RW	**Force 100BT** 1 = Force 100 Mbps if auto-negotiation is disabled (bit [12]) 0 = Force 10 Mbps if auto-negotiation is disabled (bit [12])	Bit [6] in P1CR4
12	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bit [7] in P1CR4
11	0	RW	**Power-Down** 1 = Power-down. 0 = Normal operation.	Bit [11] in P1CR4
10	0	RO	**Isolate** Not supported.	—
9	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.	Bit [11] in P1CR4
8	1	RW	**Force Full-Duplex** 1 = Force full-duplex. 0 = Force half-duplex. This bit determines duplex when auto-negotiation is disabled (bit [12]). It also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bit 5 in P1CR
7	0	RO	**Collision Test** Not supported.	—
6	0	RO	**Reserved**	—
5	1	RW	**HP_MDI-X** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	Bit [15] in P1SR
4	0	RW	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bit [9] in P1CR4
3	0	RW	**Disable MDI-X** 1 = Disable auto MDI-X. 0 = Normal operation.	Bit [10] in P1CR4
2	0	RW	**Reserved**	Bit [12] in P1CR4
1	0	RW	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bit [14] in P1CR4

TABLE 4-34: PHY 1 MII-REGISTER BASIC CONTROL REGISTER (0XE4 – 0XE5): P1MBCR

Bit	Default	R/W	Description	Bit Same As
0	0	RW	**Reserved**	—

PHY 1 MII-Register Basic Status Register (0x04E - 0x04F): P1MBSR

This register contains the Media Independent Interface (MII) status bits for the switch Port 1 function.

TABLE 4-35: PHY 1 AND MII BASIC STATUS REGISTER (0X04E - 0X04F): P1MBSR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**T4 Capable** 1 = 100 BASE-T4 capable. 0 = Not 100 BASE-T4 capable.	—
14	1	RO	**100BT Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	—
13	1	RO	**100BT Half Capable** 1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10BT Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10BT Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 - 7	0x0	RO	**Reserved**	—
6	0	RO	**Preamble suppressed** Not supported.	—
5	0	RO	**Auto-Negotiation Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bit 6 in P1SR
4	0	RO	Reserved	—
3	1	RO	**Auto-Negotiation Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bit 5 in P1SR
1	0	RO	**Jabber Test** Not supported	—
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

PHY 1 PHYID Low Register (0x050 - 0x051): PHY1ILR

This register contains the PHY ID (low) for the switch Port 1 function.

TABLE 4-36: PHY 1 PHYID LOW REGISTER (0X050 - 0X051): PHY1ILR

Bit	Default	R/W	Description
15 - 0	0x1430	RO	**PHY 1 ID Low Word** Low order PHY 1 ID bits.

PHY 1 PHYID High Register (0x052 - 0x053): PHY1IHR

This register contains the PHY ID (high) for the switch Port 1 function.

TABLE 4-37: PHY 1 PHY ID HIGH REGISTER (0XEA – 0XEB): PHY1IHR

Bit	Default	R/W	Description
15 - 0	0x0022	RO	**PHY 1 ID High Word** High order PHY 1 ID bits.

PHY 1 Auto-Negotiation Advertisement Register (0x054 - 0x055): P1ANAR

This register contains the auto-negotiation advertisement for the PHY function.

TABLE 4-38: PHY 1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0XEC – 0XED): P1ANAR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**Reserved**	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0x0	RO	**Reserved**	—
10	1	RW	**Pause (flow control capability)** 1 = Advertise pause capability. 0 = Do not advertise pause capability.	Bit [4] in P1CR4
9	0	RW	Reserved	—
8	1	RW	**Advertise 100BT Full-Duplex** 1 = Advertise 100 full-duplex capability. 0 = Do not advertise 100 full-duplex capability	Bit [3] in P1CR4
7	1	RW	**Advertise 100BT Half-Duplex** 1= Advertise 100 half-duplex capability. 0 = Do not advertise 100 half-duplex capability.	Bit [2] in P1CR4
6	1	RW	**Advertise 10BT Full-Duplex** 1 = Advertise 10 full-duplex capability. 0 = Do not advertise 10 full-duplex capability.	Bit [1] in P1CR4
5	1	RW	**Advertise 10BT Half-Duplex** 1 = Advertise 10 half-duplex capability. 0 = Do not advertise 10 half-duplex capability.	Bit [0] in P1CR4
4 - 0	0x01	RO	**Selector Field** 802.3	—

PHY 1 Auto-Negotiation Link Partner Ability Register (0x056 - 0x057): P1ANLPR

This register contains the auto-negotiation link partner ability bits for the switch Port 1 function.

TABLE 4-39: PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X056 - 0X057): P1ANLPR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0x0	RO	**Reserved**	—

TABLE 4-39: PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X056 - 0X057): P1ANLPR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As
10	0	RO	**Pause** Link partner pause capability.	Bit [4] in P1SR
9	0	RO	**Reserved**	—
8	0	RO	**Advertise 100BT Full-Duplex** Link partner 100BT full-duplex capability.	Bit [3] in P1SR
7	0	RO	**Advertise 100BT Half-Duplex** Link partner 100 half-duplex capability.	Bit [2] in P1SR
6	0	RO	**Advertise 100BT Half-Duplex** Link partner 100 half-duplex capability.	Bit [1] in P1SR
5	0	RO	**Advertise 10BT Half-Duplex** Link partner 10BT half-duplex capability.	Bit [0] in P1SR
4 - 0	0x01	RO	**Reserved**	—

PHY 2 and MII Basic Control Register (0x058 - 0x059): P2MBCR

This register contains Media Independent Interface (MII) control bits for the switch Port 2 function as defined in the IEEE 802.3 specification.

TABLE 4-40: PHY 2 AND MII BASIC CONTROL REGISTER (0X058 - 0X059): P2MBCR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Reserved**	—
14	0	RO	**Far-End Loopback** 1 = Perform loopback, as follows: Start: RXP1/RXM1 (Port 1) Loopback: PMD/PMA of Port 2's PHY End: TXP1/TXM1 (Port 1) 0 = Normal operation.	Bit [8] in P2CR4
13	1	RW	**Force 100BT** 1 = Force 100 Mbps if auto-negotiation is disabled (bit [12]) 0 = Force 10 Mbps if auto-negotiation is disabled (bit [12])	Bit [6] in P2CR4
12	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	Bit [7] in P2CR4
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation.	Bit [11] in P2CR4
10	0	RO	**Isolate** Not supported.	—
9	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation,	Bit [13] in P2CR4
8	1	RW	**Force Full Duplex** 1 = Force full-duplex. 0 = Force half-duplex. This bit determines duplex when auto-negotiation is disabled (bit [12]). It also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bit [5] in P2CR4
7	0	RO	**Collision Test** Not supported.	—
6	0	RO	**Reserved**	—

TABLE 4-40: PHY 2 AND MII BASIC CONTROL REGISTER (0X058 - 0X059): P2MBCR

Bit	Default	R/W	Description	Bit Same As
5	1	R/W	**HP_MDI-X** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	Bit [15] in P2CR4
4	0	RW	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	Bit [9] in P2CR4
3	0	RW	**Disable Auto MDI-X** 1 = Disable Auto MDI-X. 0 = Normal operation.	Bit [10] in P2CR4
2	0	RW	**Reserved**	Bit [12] in P2CR4
1	0	RW	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	Bit [14] in P2CR4
0	0	RW	**Reserved**	—

PHY 2 and MII Basic Status Register (0x05A - 0x05B): P2MBSR

This register contains the Media Independent Interface (MII) status bits for the switch Port 2 function.

TABLE 4-41: PHY 2 AND MII BASIC STATUS REGISTER (0X05A - 0X05B): P2MBSR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**T4 Capable** 1 = 100BASE-T4 capable. 0 = Not 100BASE-T4 capable.	—
14	1	RO	**100BT Full Capable** 1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	—
13	1	RO	**100BT Half Capable** 1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	—
12	1	RO	**10BT Full Capable** 1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	—
11	1	RO	**10BT Half Capable** 1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	—
10 - 7	0x0	RO	**Reserved**	—
6	0	RO	**Preamble suppressed** Not supported.	—
5	0	RO	**Auto-Negotiation Complete** 1 = Auto-negotiation complete. 0 = Auto-negotiation not completed.	Bit [6] in P2SR
4	0	RO	**Reserved**	Bit [8] in P2SR
3	1	RO	**Auto-Negotiation Capable** 1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	—
2	0	RO	**Link Status** 1 = Link is up. 0 = Link is down.	Bit [5] in P2SR
1	0	RO	**Jabber Test** Not supported.	—

TABLE 4-41: PHY 2 AND MII BASIC STATUS REGISTER (0X05A - 0X05B): P2MBSR

Bit	Default	R/W	Description	Bit Same As
0	0	RO	**Extended Capable** 1 = Extended register capable. 0 = Not extended register capable.	—

PHY 2 PHYID Low Register (0x05C - 0x05D): PHY2ILR

This register contains the PHY ID (low) for the switch Port 2 function.

TABLE 4-42: PHY 2 PHYID LOW REGISTER (0X05C - 0X05D): PHY2ILR

Bit	Default	R/W	Description
15 - 0	0x1430	RO	**PHY 2 ID Low Word** Low order PHY 1 ID bits.

PHY 2 PHYID High Register (0x05E - 0x05F): PHY2IHR

This register contains the PHY ID (high) for the switch Port 2 function.

TABLE 4-43: PHY 1 PHY ID HIGH REGISTER (0x05E - 0x05F): PHY2IHR

Bit	Default	R/W	Description
15 - 0	0x0022	RO	**PHY 2 ID High Word** High order PHY 2 ID bits.

PHY 2 Auto-Negotiation Advertisement Register (0x060 - 0x061): P2ANAR

This register contains the auto-negotiation advertisement bits for the switch Port 2 function.

TABLE 4-44: PHY 2 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (0X060 - 0X061): P2ANAR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**Reserved**	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0x0	RO	**Reserved**	—
10	1	RW	**Pause (flow control capability)** 1 = Advertise pause capability. 0 = Do not advertise pause capability.	Bit [4] in P2CR4
9	0	RW	Reserved	—
8	1	RW	**Advertise 100BT Full-Duplex** 1 = Advertise 100 full-duplex capability. 0 = Do not advertise 100 full-duplex capability	Bit [3] in P2CR4
7	1	RW	**Advertise 100BT Half-Duplex** 1= Advertise 100 half-duplex capability. 0 = Do not advertise 100 half-duplex capability.	Bit [2] in P2CR4
6	1	RW	**Advertise 10BT Full-Duplex** 1 = Advertise 10 full-duplex capability. 0 = Do not advertise 10 full-duplex capability.	Bit [1] in P2CR4
5	1	RW	**Advertise 10BT Half-Duplex** 1 = Advertise 10 half-duplex capability. 0 = Do not advertise 10 half-duplex capability.	Bit [0] in P2CR4
4 - 0	0x01	RO	**Selector Field** 802.3	—

PHY 2 Auto-Negotiation Link Partner Ability Register (0x062 -0x063): P2ANLPR

This register contains the auto-negotiation link partner ability bits for the switch Port 2 function.

TABLE 4-45: PHY 2 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (0X062 -0X063): P2ANLPR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**Next page** Not supported.	—
14	0	RO	**LP ACK** Not supported.	—
13	0	RO	**Remote fault** Not supported.	—
12 - 11	0x0	RO	**Reserved**	—
10	0	RO	**Pause** Link partner pause capability.	Bit [4] in P2SR
9	0	RO	**Reserved**	—
8	0	RO	**Advertise 100BT Full-Duplex** Link partner 100BT full-duplex capability.	Bit [3] in P2SR
7	0	RO	**Advertise 100BT Half-Duplex** Link partner 100 half-duplex capability.	Bit [2] in P2SR
6	0	RO	**Advertise 100BT Half-Duplex** Link partner 100 half-duplex capability.	Bit [1] in P2SR
5	0	RO	**Advertise 10BT Half-Duplex** Link partner 10BT half-duplex capability.	Bit [0] in P2SR
4 - 0	0x01	RO	**Reserved**	—

0x0x064 - 0x065: Reserved

PHY1 Special Control and Status Register (0x066 - 0x067): P1PHYCTRL

This register contains control and status information of PHY 1.

TABLE 4-46: PHY1 SPECIAL CONTROL AND STATUS REGISTER (0X066 - 0X067): P1PHYCTRL

Bit	Default	R/W	Description	Bit Same As
15 - 6	0x000	RO	**Reserved**	—
5	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit [13] in P1SR
4	0	RO	**MDI-X Status** 0 = MDI 1 = MDI-X	Bit [7] in P1SR
3	0	RW	**Force Link** 1 = Force link pass. 0 = Normal operation.	Bit [11] in P1SCSLMD
2	1	RW	**Enable Energy Efficient Ethernet (EEE) on 10BTe** 1 = Disable 10BTe. 0 = Enable 10BTe.	—
51	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 1's PHY (RXP1/RXM1 −> TXP1/TXM1). 0 = Normal operation.	Bit [9] in P1SCSLMD
0	0	RW	**Reserved**	—

0x068 - 0x069: Reserved

PHY2 Special Control and Status Register (0x06A - 0x06B): P2PHYCTRL

This register contains control and status information of PHY 2.

TABLE 4-47: PHY2 SPECIAL CONTROL AND STATUS REGISTER (0X06A - 0X06B): P2PHYCTRL

Bit	Default	R/W	Description	Bit Same As
15 - 6	0x000	RO	**Reserved**	—
5	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit [13] in P2SR
4	0	RO	**MDI-X Status** 0 = MDI 1 = MDI-X	Bit [7] in P2SR
3	0	RW	**Force Link** 1 = Force link pass. 0 = Normal operation.	Bit [11] in P2SCSLMD
2	1	RW	**Enable Energy Efficient Ethernet (EEE) on 10BTe** 1 = Disable 10BTe. 0 = Enable 10BTe.	—
1	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 2's PHY (RXP2/RXM2 −> TXP2/TXM2). 0 = Normal operation.	Bit [9] in P2SCSLMD
0	0	RW	**Reserved**	—

4.9 Port 1 Control Registers

Port 1 Control Register 1 (0x06C - 0x06D): P1CR1

This register contains control bits for the switch Port 1 function.

TABLE 4-48: PORT 1 CONTROL REGISTER 1 (0X06C - 0X06D): P1CR1

Bit	Default	R/W	Description
15	0	RO	**Reserved**
14 - 12	0x00	R/W	**Port 1 LED Direct Control** These bits directly control the Port 1 LED pins. 0xx = Normal LED function as set up via Reg. 0x00E - 0x00F, Bits [9:8]. 100 = Both Port 1 LEDs off. 101 = Port 1 LED1 off, LED0 on. 110 = Port 1 LED1 on, LED0 off. 111 = Both Port 1 LEDs on.
11	0	RW	**Source Address Filtering Enable for MAC Address 2** 1 = Enable the source address filtering function when the SA matches MAC Address 2 in SAFMACA2 (0x0B6 - 0x0BB). 0 = Disable source address filtering function.
10	0	RW	**Source Address Filtering Enable for MAC Address 1** 1 = Enable the source address filtering function when the SA matches MAC Address 1 in SAFMACA1 (0x0B0 - 0x0B5). 0 = Disable source address filtering function.
9	0	RW	**Drop Tagged Packet Enable** 1 = Enable to drop tagged ingress packets. 0 = Disable to drop tagged ingress packets.
8	0	RW	**TX Two Queues Select Enable** 1 = The Port 1 output queue is split into two priority queues (q0 and q1). 0 = Single output queue on Port 1. There is no priority differentiation even though packets are classified into high or low priority.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on Port 1. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on Port 1. 0 = Disable DiffServ function.
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on Port 1. 0 = Disable 802.1p.
4 - 3	0x0	RW	**Port-Based Priority Classification** 00 = Ingress packets on Port 1 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 1 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 1 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 1 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.

TABLE 4-48: PORT 1 CONTROL REGISTER 1 (0X06C - 0X06D): P1CR1 (CONTINUED)

Bit	Default	R/W	Description
2	0	RW	**Tag Insertion** 1 = When packets are output on Port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port's "port VID". 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on Port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The Port 1 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on Port 1. There is no priority differentiation even though packets are classified into high or low priority.

Port 1 Control Register 2 (0x06E - 0x06F): P1CR2

This register contains control bits for the switch Port 1 function.

TABLE 4-49: PORT 1 CONTROL REGISTER 2 (0X06E - 0X06F): P1CR2

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.

TABLE 4-49: PORT 1 CONTROL REGISTER 2 (0X06E - 0X06F): P1CR2 (CONTINUED)

Bit	Default	R/W	Description
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No transmit monitoring.
4	0	RW	**Reserved**
3	0	RO	**User Priority Ceiling** 1 = If the packet’s “priority field” is greater than the “user priority field” in the port VID control register bit[15:13], replace the packet’s “priority field” with the “user priority field” in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet’s “priority field.”
2 - 0	1x1x1	RO	**Port VLAN Membership** Define the port’s Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership; a ‘0’ excludes a port from the membership.

Port 1 VID Control Register (0x070 - 0x071): P1VIDCR

This register contains the control bits for the switch Port 1 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-50: PORT 1 VID CONTROL REGISTER (0X070 - 0X071): P1VIDCR

Bit	Default	R/W	Description
15 - 13	0x00	RW	**Default Tag[15:13]** Port’s default tag, containing “User Priority Field” bits.
12	0	RW	**Default Tag[12]** Port’s default tag, containing the CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port’s default tag, containing the VID[11:0].

Port 1 Control Register 3 (0x072 - 0x073): P1CR3

This register contains control bits for the switch Port 1 function.

TABLE 4-51: PORT 1 CONTROL REGISTER 3 (0X072 - 0X073): P1CR3

Bit	Default	R/W	Description
15 - 5	0x000	RO	**Reserved**
4	0	RW	**Reserved**
3 - 2	0x0	RW	Ingress Limit Mode These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.

TABLE 4-51: PORT 1 CONTROL REGISTER 3 (0X072 - 0X073): P1CR3 (CONTINUED)

Bit	Default	R/W	Description
1	1x11	RW	Count Inter Frame Gap Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	Count Preamble Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Port 1 Ingress Rate Control Register 0 (0x074 - 0x075): P1IRCR0

This register contains the Port 1 ingress rate limiting control for priority 1 and priority 0.

TABLE 4-52: PORT 1 INGRESS RATE CONTROL REGISTER 0 (0X074 - 0X075): P1IRCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

TABLE 4-53: INGRESS OR EGRESS DATA RATE LIMITS

Data Rate Limit for Ingress or Egress	100BT for Priority [3:0] Register Bit [14:8] or Bit[6:0]	10BT for Priority [3:0] Register Bit [14:8] or Bit[6:0]
	0x01 to 0x64 for the rate matches 1Mbps to 100 Mbps respectively	0x01 to 0x0A for the rate matches 1Mbps to 10 Mbps respectively
	0x00 (default) for the rate is no limit (full 100 Mbps)	0x00 (default) for the rate is no limit (full 10 Mbps)
64 Kbps	0x65	
128 Kbps	0x66	
192 Kbps	0x67	
256 Kbps	0x68	
320 Kbps	0x69	
384 Kbps	0x6A	
448 Kbps	0x6B	
512 Kbps	0x6C	
576 Kbps	0x6D	
640 Kbps	0x6E	
704 Kbps	0x6F	
768 Kbps	0x70	

TABLE 4-53: INGRESS OR EGRESS DATA RATE LIMITS (CONTINUED)

Data Rate Limit for Ingress or Egress	100BT for Priority [3:0] Register Bit [14:8] or Bit[6:0]	10BT for Priority [3:0] Register Bit [14:8] or Bit[6:0]
	0x01 to 0x64 for the rate matches 1Mbps to 100 Mbps respectively	0x01 to 0x0A for the rate matches 1Mbps to 10 Mbps respectively
	0x00 (default) for the rate is no limit (full 100 Mbps)	0x00 (default) for the rate is no limit (full 10 Mbps)
832 Kbps	0x71	
896 Kbps	0x72	
960 Kbps	0x73	

Port 1 Ingress Rate Control Register 1 (0x076 - 0x077): P1IRCR1

This register contains the Port 1 ingress rate limiting control bits for priority 3 and priority 2.

TABLE 4-54: PORT 1 INGRESS RATE CONTROL REGISTER 1 (0X076 - 0X077): P1IRCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 1 Egress Rate Control Register 0 (0x078 - 0x079): P1ERCR0

This register contains the Port 1 egress rate limiting control bits for priority 3 and priority 2.

TABLE 4-55: PORT 1 EGRESS RATE CONTROL REGISTER 0 (0X078 - 0X079): P1IRCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Egress Rate Limit Control Enable** 1 = Enable egress rate limit control. 0 = Disable egress rate limit control.
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 1 Egress Rate Control Register 1 (0x07A - 0x07B): P1ERCR1

This register contains the Port 1 egress rate limiting control bits for priority 3 and priority 2.

TABLE 4-56: PORT 1 EGRESS RATE CONTROL REGISTER 1 (0X07A - 0X07B): P1ERCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 1 PHY Special Control/Status, LinkMD (0x07C - 0x07D): P1SCSLMD

This register contains the LinkMD control and status information of PHY 1.

TABLE 4-57: PORT 1 PHY SPECIAL CONTROL/STATUS, LINKMD (0X07C - 0X07D): P1SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**CDT_10m_Short** 1 = Less than 10 meter short.	—
14 - 13	0x0	RO	**CDT_Result** [00] = Normal condition. [01] = Open condition has been detected in cable. [10] = Short condition has been detected in cable. [11] = Cable diagnostic test has failed.	—
12	0	RW/SC	**CDT_Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the CDT test is done. 0 = Indicates that the cable diagnostic test is completed and the status information is valid for reading.	—
11	0	RW	**Force_Link** Force link. 1 = Force link pass. 0 = Normal operation.	Bit [3] in P1PHYCTRL
10	1	RW	**Reserved**	—
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 1's PHY (RXP1/RXM1 −> TXP1/TXM1) 0 = Normal operation	Bit [1] in P1PHYCTRL
8 - 0	0x000	RO	**CDT_Fault_Count** Distance to the fault. It's approximately 0.4m*CDT-Fault_Count.	—

Port 1 Control Register 4 (0x07E - 0x07F): P1CR4

This register contains control bits for the switch Port 1 function.

TABLE 4-58: PORT 1 CONTROL REGISTER 4 (0X07E - 0X07F): P1CR4

Bit	Default	R/W	Description	Bit Same As:
15	0	RW	**Reserved**	—
14	0	RW	**Disable Transmit** 1 = Disable the port's transmitter. 0 = Normal operation.	Bit [1] in P1MBCR
13	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation..	Bit [9] in P1MBCR
12	0	RW	**Reserved**	Bit [2] in P1MBCR
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation. No change to registers setting.	Bit [11] in P1MBCR
10	0	RW	**Disable Auto MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto-MDI/MDI-X function.	Bit [3] in P1MBCR
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bit [4] in P1MBCR
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP2/RXM2 (Port 2). Loopback: PMD/PMA of Port 1's PHY. End: TXP2/TXM2 (Port 2). 0 = Normal operation.	Bit [14] in P1MBCR
7	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register.	Bit [12] in P1MBCR
6	1	RW	**Force Speed** 1 = Force 100BT if auto-negotiation is disabled (bit [7]). 0 = Force 10BT if auto-negotiation is disabled (bit [7]).	Bit [13] in P1MBCR
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. This bit also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bit [8] in P1MBCR
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bit [10] in P1ANAR
3	1	RW	**Advertised 100BT Full-Duplex Capability** 1 = Advertise 100BT full-duplex capability. 0 = Suppress 100BT full-duplex capability from transmission to link partner.	Bit [8] in P1ANAR

TABLE 4-58: PORT 1 CONTROL REGISTER 4 (0X07E - 0X07F): P1CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit Same As:
2	1	RW	**Advertised 100BT Half-Duplex Capability** 1 = Advertise 100BT half-duplex capability. 0 = Suppress 100BT half-duplex capability from transmission to link partner.	Bit [7] in P1ANAR
1	1	RW	**Advertised 10BT Full-Duplex Capability** 1 = Advertise 10BT full-duplex capability. 0 = Suppress 10BT full-duplex capability from transmission to link partner.	Bit [6] in P1ANAR
0	1	RW	**Advertised 10BT Half-Duplex Capability** 1 = Advertise 10BT half-duplex capability. 0 = Suppress 10BT half-duplex capability from transmission to link partner.	Bit [5] in P1ANAR

Port 1 Status Register (0x080 - 0x081): P1SR

This register contains control bits for the switch Port 1 function.

TABLE 4-59: PORT 1 STATUS REGISTER (0X080 - 0X081): P1SR

Bit	Default	R/W	Description	Bit Same As:
15	1	RW	**HP_MDI-X** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit [5] in P1MBCR
14	0	RO	**Reserved**	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit [5] in P1PHYCTRL
12	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—
11	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	**Reserved**	Bit [4] in P1MBSR
7	0	RO	**MDI-X Status** 0 = MDI. 1 = MDI-X	Bit [4] in P1PHYCTRL
6	0	RO	**Auto-Negotiation Done** 1 = Auto-negotiation done. 0 = Auto-negotiation not done.	Bit [5] in P1MBSR
5	0	RO	**Link Status** 1 = Link good. 0 = Link not good.	Bit [2] in P1MBSR
4	0	RO	**Partner Flow Control Capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bit [10] in P1ANLPR

TABLE 4-59: PORT 1 STATUS REGISTER (0X080 - 0X081): P1SR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As:
3	0	RO	**Partner 100BT Full-Duplex Capability** 1 = Link partner 100BT full-duplex capable. 0 = Link partner not 100BT full-duplex capable.	Bit [8] in P1ANLPR
2	0	RO	**Partner 100BT Half-Duplex Capability** 1 = Link partner 100BT half-duplex capable. 0 = Link partner not 100BT half-duplex capable.	Bit [7] in P1ANLPR
1	0	RO	**Partner 10BT Full-Duplex Capability** 1 = Link partner 10BT full-duplex capable. 0 = Link partner not 10BT full-duplex capable.	Bit [6] in P1ANLPR
0	0	RO	**Partner 10BT Half-Duplex Capability** 1 = Link partner 10BT half-duplex capable. 0 = Link partner not 10BT half-duplex capable.	Bit [5] in P1ANLPR

0x082 - 0x083: Reserved

4.10 Port 2 Control Registers

Port 2 Control Register 1 (0x084 - 0x085): P2CR1

This register contains control bits for the switch Port 2 function.

TABLE 4-60: PORT 2 CONTROL REGISTER 1 (0X084 - 0X085): P2CR1

Bit	Default	R/W	Description
15	0	RO	**Reserved**
14 - 12	0x00	R/W	**Port 1 LED Direct Control** These bits directly control the Port 2 LED pins. 0xx = Normal LED function as set up via Reg. 0x00E - 0x00F, Bits [9:8]. 100 = Both Port 2 LEDs off. 101 = Port 2 LED1 off, LED0 on. 110 = Port 2 LED1 on, LED0 off. 111 = Both Port 2 LEDs on.
11	0	RW	**Source Address Filtering Enable for MAC Address 2** 1 = Enable the source address filtering function when the SA matches MAC Address 2 in SAFMACA2 (0x0B6 - 0x0BB). 0 = Disable source address filtering function.
10	0	RW	**Source Address Filtering Enable for MAC Address 1** 1 = Enable the source address filtering function when the SA matches MAC Address 1 in SAFMACA1 (0x0B0 - 0x0B5). 0 = Disable source address filtering function.
9	0	RW	**Drop Tagged Packet Enable** 1 = Enable to drop tagged ingress packets. 0 = Disable to drop tagged ingress packets.
8	0	RW	**TX Two Queues Select Enable** 1 = The Port 2 output queue is split into two priority queues (q0 and q1). 0 = Single output queue on Port 2. There is no priority differentiation even though packets are classified into high or low priority.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on Port 2. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on Port 2. 0 = Disable DiffServ function.

TABLE 4-60: PORT 2 CONTROL REGISTER 1 (0X084 - 0X085): P2CR1

Bit	Default	R/W	Description
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on Port 2. 0 = Disable 802.1p.
4 - 3	0x0	RW	**Port-Based Priority Classification** 00 = Ingress packets on Port 2 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 2 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 2 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 2 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	**Tag Insertion** 1 = When packets are output on Port 2, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on Port 2, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The Port 1 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on Port 2. There is no priority differentiation even though packets are classified into high or low priority.

Port 2 Control Register 2 (0x086 - 0x087): P2CR2

This register contains control bits for the switch Port 2 function.

TABLE 4-61: PORT 2 CONTROL REGISTER 2 (0X086 - 0X087): P2CR2

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port’s half-duplex back pressure. 0 = Disable port’s half-duplex back pressure.

TABLE 4-61: PORT 2 CONTROL REGISTER 2 (0X086 - 0X087): P2CR2 (CONTINUED)

Bit	Default	R/W	Description
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No transmit monitoring.
4	0	RW	**Reserved**
3	0	RO	**User Priority Ceiling** 1 = If the packet’s “priority field” is greater than the “user priority field” in the port VID control register bit[15:13], replace the packet’s “priority field” with the “user priority field” in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet’s “priority field.”
2 - 0	1x1x1	RO	**Port VLAN Membership** Define the port’s Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership; a ‘0’ excludes a port from the membership.

Port 2 VID Control Register (0x088 - 0x089): P2VIDCR

This register contains the control bits for the switch Port 2 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-62: PORT 2 VID CONTROL REGISTER (0X088 - 0X089): P2VIDCR

Bit	Default	R/W	Description
15 - 13	0x00	RW	**Default Tag[15:13]** Port’s default tag, containing “User Priority Field” bits.
12	0	RW	**Default Tag[12]** Port’s default tag, containing the CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port’s default tag, containing the VID[11:0].

Port 2 Control Register 3 (0x08A-0x08B): P2CR3

This register contains control bits for the switch Port 2 function.

TABLE 4-63: PORT 2 CONTROL REGISTER 3 (0X08A-0X08B): P2CR3

Bit	Default	R/W	Description
15 - 5	0x000	RO	**Reserved**
4	0	RW	**Reserved**
3 - 2	0x0	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	1x11	RW	**Count Inter Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Port 2 Ingress Rate Control Register 0 (0x08C - 0x08D): P2IRCR0

This register contains the Port 2 ingress rate limiting control for priority 1 and priority 0.

TABLE 4-64: PORT 2 INGRESS RATE CONTROL REGISTER 0 (0X08C - 0X08D): P2IRCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 2 Ingress Rate Control Register 1 (0x08E - 0x08F): P2IRCR1

This register contains the Port 2 ingress rate limiting control bits for priority 3 and priority 2 frames.

TABLE 4-65: PORT 2 INGRESS RATE CONTROL REGISTER 1 (0X08E - 0X08F): P2IRCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**

TABLE 4-65: PORT 2 INGRESS RATE CONTROL REGISTER 1 (0X08E - 0X08F): P2IRCR1

Bit	Default	R/W	Description
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 2 Egress Rate Control Register 0 (0x090 - 0x091): P2ERCR0

This register contains the Port 2 egress rate limiting control bits for priority 1 and priority 0.

TABLE 4-66: PORT 2 EGRESS RATE CONTROL REGISTER 0 (0X090 - 0X091): P2ERCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Egress Rate Limit Control Enable** 1 = Enable egress rate limit control. 0 = Disable egress rate limit control.
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited or discarded as shown in Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 2 Egress Rate Control Register 1 (0x092 – 0x093): P2ERCR1

This register contains the Port 2 egress rate limiting control bits for priority 3 and priority 2 frames.

TABLE 4-67: PORT 2 EGRESS RATE CONTROL REGISTER 1 (0X092 – 0X093): P2ERCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 2 PHY Special Control/Status, LinkMD (0x094 - 0x095): P2SCSLMD

This register contains the LinkMD control and status information of PHY 2.

TABLE 4-68: PORT 2 PHY SPECIAL CONTROL/STATUS, LINKMD (0X094 - 0X095): P2SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	**CDT_10m_Short** 1 = Less than 10 meter short.	—
14 - 13	0x0	RO	**CDT_Result** [00] = Normal condition. [01] = Open condition has been detected in cable. [10] = Short condition has been detected in cable. [11] = Cable diagnostic test has failed.	—
12	0	RW/SC	**CDT_Enable** 1 = Cable diagnostic test is enabled. It is self-cleared after the CDT test is done. 0 = Indicates that the cable diagnostic test is completed and the status information is valid for reading.	—
11	0	RW	**Force_Link** Force link. 1 = Force link pass. 0 = Normal operation.	Bit [3] in P2PHYCTRL
10	1	RW	**Reserved**	—
9	0	RW	**Remote (Near-End) Loopback** 1 = Perform remote loopback at Port 1's PHY (RXP1/RXM1 −> TXP1/TXM1) 0 = Normal operation	—Bit [1] in P2PHYCTRL
8 - 0	0x000	RO	**CDT_Fault_Count** Distance to the fault. It's approximately 0.4m*CDT-Fault_Count.	—

Port 2 Control Register 4 (0x096 - 0x097): P2CR4

This register contains control bits for the switch Port 2 function.

TABLE 4-69: PORT 2 CONTROL REGISTER 4 (0X096 - 0X097): P2CR4

Bit	Default	R/W	Description	Bit Same As:
15	0	RW	**Reserved**	—
14	0	RW	**Disable Transmit** 1 = Disable the port's transmitter. 0 = Normal operation.	Bit [1] in P2MBCR
13	0	RW/SC	**Restart Auto-Negotiation** 1 = Restart auto-negotiation. 0 = Normal operation.	Bit [9] in P2MBCR
12	0	RW	**Reserved**	Bit [2] in P2MBCR
11	0	RW	**Power Down** 1 = Power down. 0 = Normal operation. No change to registers setting.	Bit [11] in P2MBCR
10	0	RW	**Disable Auto MDI/MDI-X** 1 = Disable Auto-MDI/MDI-X function. 0 = Enable Auto-MDI/MDI-X function.	Bit [3] in P2MBCR

TABLE 4-69: PORT 2 CONTROL REGISTER 4 (0X096 - 0X097): P2CR4

Bit	Default	R/W	Description	Bit Same As:
9	0	RW	**Force MDI-X** 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode. 0 = Do not force PHY into MDI-X mode.	Bit [4] in P2MBCR
8	0	RW	**Far-End Loopback** 1 = Perform loopback, as indicated: Start: RXP1/RXM1(Port 1). Loopback: PMD/PMA of Port 2's PHY. End: TXP2/TXM1 (Port 1). 0 = Normal operation.	Bit [14] in P2MBCR
7	1	RW	**Auto-Negotiation Enable** 1 = Auto-negotiation is enabled. 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register.	Bit [12] in P2MBCR
6	1	RW	**Force Speed** 1 = Force 100 BT if auto-negotiation is disabled (bit [7]). 0 = Force 10 BT if auto-negotiation is disabled (bit [7]).	Bit [13] in P2MBCR
5	1	RW	**Force Duplex** 1 = Force full-duplex if auto-negotiation is disabled. 0 = Force half-duplex if auto-negotiation is disabled. This bit also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero.	Bit [8] in P2MBCR
4	1	RW	**Advertised Flow Control Capability** 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner.	Bit [10] in P2ANAR
3	1	RW	**Advertised 100BT Full-Duplex Capability** 1 = Advertise 100 BT full-duplex capability. 0 = Suppress 100 BT full-duplex capability from transmission to link partner.	Bit [8] in P2ANAR
2	1	RW	**Advertised 100BT Half-Duplex Capability** 1 = Advertise 100 BT half-duplex capability. 0 = Suppress 100 BT half-duplex capability from transmission to link partner.	Bit [7] in P2ANAR
1	1	RW	**Advertised 10BT Full-Duplex Capability** 1 = Advertise 10 BT full-duplex capability. 0 = Suppress 10 BT full-duplex capability from transmission to link partner.	Bit [6] in P2ANAR
0	1	RW	**Advertised 10BT Half-Duplex Capability** 1 = Advertise 10 BT half-duplex capability. 0 = Suppress 10 BT half-duplex capability from transmission to link partner.	Bit [5] in P2ANAR

Port 2 Status Register (0x098 - 0x099): P2SR

This register contains control bits for the switch Port 2 function.

TABLE 4-70: PORT 2 STATUS REGISTER (0X098 - 0X099): P2SR

Bit	Default	R/W	Description	Bit Same As:
15	1	RW	**HP_MDI-X** 1 = HP Auto-MDI-X mode. 0 = Microchip Auto-MDI-X mode.	Bit [5] in P2MBCR

TABLE 4-70: PORT 2 STATUS REGISTER (0X098 - 0X099): P2SR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As:
14	0	RO	**Reserved**	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	Bit [5] in P2PHYCTRL
12	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—
11	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	**Reserved**	Bit [4] in P2MBSR
7	0	RO	**MDI-X Status** 0 = MDI. 1 = MDI-X	Bit [4] in P2PHYCTRL
6	0	RO	**Auto-Negotiation Done** 1 = Auto-negotiation done. 0 = Auto-negotiation not done.	Bit [5] in P2MBSR
5	0	RO	**Link Status** 1 = Link good. 0 = Link not good.	Bit [2] in P2MBSR
4	0	RO	**Partner Flow Control Capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	Bit [10] in P2ANLPR
3	0	RO	**Partner 100BT Full-Duplex Capability** 1 = Link partner 100 BT full-duplex capable. 0 = Link partner not 100 BT full-duplex capable.	Bit [8] in P2ANLPR
2	0	RO	**Partner 100BT Half-Duplex Capability** 1 = Link partner 100 BT half-duplex capable. 0 = Link partner not 100 BT half-duplex capable.	Bit [7] in P2ANLPR
1	0	RO	**Partner 10BT Full-Duplex Capability** 1 = Link partner 10 BT full-duplex capable. 0 = Link partner not 10 BT full-duplex capable.	Bit [6] in P2ANLPR
0	0	RO	**Partner 10BT Half-Duplex Capability** 1 = Link partner 10 BT half-duplex capable. 0 = Link partner not 10 BT half-duplex capable.	Bit [5] in P2ANLPR

0x09A – 0x09B: Reserved

4.11 Port 3 Control Registers

Port 3 Control Register 1 (0x09C - 0x09D): P3CR1

This register contains control bits for the switch Port 3 function.

TABLE 4-71: PORT 3 CONTROL REGISTER 1 (0X09C - 0X09D): P3CR1

Bit	Default	R/W	Description
15 - 10	0x00	RO	**Reserved**
9	0	R/W	Drop Tagged Packet Enable 1 = Enable to drop tagged ingress packets. 0 = Disable to drop tagged ingress packets.
8	0	RW	**TX Two Queues Select Enable** 1 = The Port 3 output queue is split into two priority queues (q0 and q1). 0 = Single output queue on Port 3. There is no priority differentiation even though packets are classified into high or low priority.
7	0	RW	**Broadcast Storm Protection Enable** 1 = Enable broadcast storm protection for ingress packets on Port 3. 0 = Disable broadcast storm protection.
6	0	RW	**Diffserv Priority Classification Enable** 1 = Enable DiffServ priority classification for ingress packets on Port 3. 0 = Disable DiffServ function.
5	0	RW	**802.1p Priority Classification Enable** 1 = Enable 802.1p priority classification for ingress packets on Port 3. 0 = Disable 802.1p.
4 - 3	0x0	RW	**Port-Based Priority Classification** 00 = Ingress packets on Port 3 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 3 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 3 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 3 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	**Tag Insertion** 1 = When packets are output on Port 3, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	**Tag Removal** 1 = When packets are output on Port 3, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	**TX Multiple Queues Select Enable** 1 = The Port 3 output queue is split into four priority queues (q0, q1, q2 and q3). 0 = Single output queue on Port 3. There is no priority differentiation even though packets are classified into high or low priority.

Port 3 Control Register 2 (0x09E - 0x09F): P3CR2

This register contains control bits for the switch Port 3 function.

TABLE 4-72: PORT 3 CONTROL REGISTER 2 (0X09E - 0X09F): P3CR2

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14	0	RW	**Ingress VLAN Filtering** 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	**Discard Non PVID Packets** 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	**Force Flow Control** 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	**Back Pressure Enable** 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	**Transmit Enable** 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	**Receive Enable** 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	**Learning Disable** 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	**Sniffer Port** 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	**Receive Sniff** 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	**Transmit Sniff** 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RW	**Reserved**
3	0	RW	**User Priority Ceiling** 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	**Port VLAN Membership** Define the port's Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

Port 3 VID Control Register (0x0A0 - 0x0A1): P3VIDCR

This register contains the control bits for the switch Port 2 function. This register has two main uses. It is associated with the ingress of untagged packets and used for egress tagging as well as being used for address lookup and providing a default VID for the ingress of untagged or null-VID-tagged packets.

TABLE 4-73: PORT 3 VID CONTROL REGISTER (0X0A0 - 0X0A1): P3VIDCR

Bit	Default	R/W	Description
15 - 13	0x00	RW	**Default Tag[15:13]** Port's default tag, containing "User Priority Field" bits.
12	0	RW	**Default Tag[12]** Port's default tag, containing the CFI bit.
11 - 0	0x001	RW	**Default Tag[11:0]** Port's default tag, containing the VID[11:0].

Port 3 Control Register 3 (0x0A2 - 0x0A3): P3CR3

This register contains control bits for the switch Port 3 function.

TABLE 4-74: PORT 3 CONTROL REGISTER 3 (0X0A2 - 0X0A3): P3CR3

Bit	Default	R/W	Description
15 - 8	0x000	RO	**Reserved**
7	0	RW	**Reserved**
6 - 4	0	RW	**Reserved**
3 - 2	0x0	RW	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	1x11	RW	**Count Inter Frame Gap** Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	**Count Preamble** Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Port 3 Ingress Rate Control Register 0 (0x0A4 - 0x0A5): P3IRCR0

This register contains the Port 3 ingress rate limiting control for priority 1 and priority 0.

TABLE 4-75: PORT 3 INGRESS RATE CONTROL REGISTER 0 (0X0A4 - 0X0A5): P3IRCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 1 Frames** Ingress priority 1 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**

TABLE 4-75: PORT 3 INGRESS RATE CONTROL REGISTER 0 (0X0A4 - 0X0A5): P3IRCR0

Bit	Default	R/W	Description
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 0 Frames** Ingress priority 0 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 3 Ingress Rate Control Register 1 (0x0A6 - 0x0A7): P3IRCR1

This register contains the Port 3 ingress rate limiting control bits for priority 3 and priority 2 frames.

TABLE 4-76: PORT 3 INGRESS RATE CONTROL REGISTER 1 (0X0A6 - 0X0A7): P3IRCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Ingress Data Rate Limit for Priority 3 Frames** Ingress priority 3 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Ingress Data Rate Limit for Priority 2 Frames** Ingress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 3 Egress Rate Control Register 0 (0x0A8 - 0x0A9): P3ERCR0

This register contains the Port 2 egress rate limiting control bits for priority 1 and priority 0.

TABLE 4-77: PORT 3 EGRESS RATE CONTROL REGISTER 0 (0X0A8 - 0X0A9): P3ERCR0

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 1 Frames** Egress priority 1 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Egress Rate Limit Control Enable** 1 = Enable egress rate limit control. 0 = Disable egress rate limit control.
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 0 Frames** Egress priority 0 frames will be limited or discarded as shown in Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

Port 3 Egress Rate Control Register 1 (0x0AA - 0x0AB): P3ERCR1

This register contains the Port 3 egress rate limiting control bits for priority 3 and priority 2 frames.

TABLE 4-78: PORT 3 EGRESS RATE CONTROL REGISTER 1 (0X0AA - 0X0AB): P3ERCR1

Bit	Default	R/W	Description
15	0	RW	**Reserved**
14 - 8	0x00	RW	**Egress Data Rate Limit for Priority 3 Frames** Egress priority 3 frames will be limited or discarded as shown in Table 4-53 Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.
7	0	RW	**Reserved**
6 - 0	0x00	RW	**Egress Data Rate Limit for Priority 2 Frames** Egress priority 2 frames will be limited or discarded as shown in the Table 4-53. Note: The default value 0x00 is full rate at 10 Mbps or 100 Mbps with no limit.

4.12 Switch Global Control Registers

Switch Global Control Register 8 (0x0AC - 0x0AD): SGCR8

This register contains global control bits for the switch function.

TABLE 4-79: SWITCH GLOBAL CONTROL REGISTER 8 (0X0AC - 0X0AD): SGCR8

Bit	Default	R/W	Description
15 - 14	1x0	RW	**Two Queue Priority Mapping** These bits determine the mapping between the priority of the incoming frames and the destination on-chip queue in a two queue configuration which uses egress queues 0 and 1. ‘00’ = Egress Queue 1 receives priority 3 frames Egress Queue 0 receives priority 0, 1, 2 frames ‘01’ = Egress Queue 1 receives priority 1, 2, 3 frames Egress Queue 0 receives priority 0 frames ‘10’ = Egress Queue 1 receives priority 2, 3 frames Egress Queue 0 receives priority 0, 1 frames ‘11’ = Egress Queue 1 receives priority 1, 2, 3 frames Egress Queue 0 receives priority 0 frames
13 - 11	0x00	RO	**Reserved**
10	0	RW	**Flush Dynamic MAC Table** Before flushing the dynamic MAC table, switch address learning must be disabled by setting bit[8] in the P1CR2, P2CR2 and P3CR2 registers.
9	1	RW	**Flush Static MAC Table** 1 = Enable flush static MAC table for spanning tree application 0 = Disable flush static MAC table for spanning tree application
8	0	RW	**Port 3 Tail Tag Mode Enable** 1 = Enable tail tag mode 0 = Disable tail tag mode
7 - 0	0x00	RW	**Force PAUSE Off Iteration Limit Time Enable** 0x01 - 0xFF = Enable to force PAUSE off iteration limit time (a unit number is 160 ms) 0x00 = Disable Force PAUSE Off Iteration Limit

Switch Global Control Register 9 (0x0AE - 0x0AF): SGCR9

This register contains global control bits for the switch function.

TABLE 4-80: SWITCH GLOBAL CONTROL REGISTER 9 (0X0AE - 0X0AF): SGCR9

Bit	Default	R/W	Description
15 - 11	0x00	RO	**Reserved**
10 - 08	000	RW	**Forwarding Invalid Frame** Define the forwarding port for frame with invalid VID. Bit [10] stands for the host port, bit [9] for Port 2, and bit [8] for Port 1.
7 - 6	00	RW	**Reserved**
5	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 3 to Port 2** 1 = Enable 0 = Disable
4	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 3 to Port 1** 1 = Enable 0 = Disable
3	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 2 to Port 3** 1 = Enable 0 = Disable
2	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 2 to Port 1** 1 = Enable 0 = Disable
1	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 1 to Port 3** 1 = Enable 0 = Disable
0	0	RW	**Enable Insert Source Port PVID Tag when Untagged Frame from Port 1 to Port 2** 1 = Enable 0 = Disable

4.13 Source Address Filtering Registers

Source Address Filtering MAC Address 1 Register Low (0x0B0 - 0x0B1): SAFMACA1L

Register bit fields for the low word of MAC Address 1.

TABLE 4-81: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER LOW (0X0B0 - 0X0B1): SAFMACA1L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 1 Low** The least significant word of MAC Address 1.

Source Address Filtering MAC Address 1 Register Middle (0x0B2 - 0x0B3): SAFMACA1M

Register bit fields for the low word of MAC Address 1.

TABLE 4-82: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER MIDDLE (0X0B2 - 0X0B3): SAFMACA1M

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 1 Middle** The middle word of MAC Address 1.

Source Address Filtering MAC Address 1 Register High (0x0B4 - 0x0B5): SAFMACA1H

Register bit fields for the low word of MAC Address 1.

TABLE 4-83: SOURCE ADDRESS FILTERING MAC ADDRESS 1 REGISTER HIGH (0X0B4 - 0X0B5): SAFMACA1H

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 1 High** The most significant word of MAC Address 1.

Source Address Filtering MAC Address 2 Register Low (0x0B0 - 0x0B1): SAFMACA2L

Register bit fields for the low word of MAC Address 2.

TABLE 4-84: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER LOW (0X0B0 - 0X0B1): SAFMACA2L

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 2 Low** The least significant word of MAC Address 2.

Source Address Filtering MAC Address 2 Register Middle (0x0B2 - 0x0B3): SAFMACA2M

Register bit fields for the low word of MAC Address 2.

TABLE 4-85: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER MIDDLE (0X0B2 - 0X0B3): SAFMACA2M

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 2 Middle** The middle word of MAC Address 2.

Source Address Filtering MAC Address 2 Register High (0x0B4 - 0x0B5): SAFMACA2H

Register bit fields for the low word of MAC Address 2.

TABLE 4-86: SOURCE ADDRESS FILTERING MAC ADDRESS 2 REGISTER HIGH (0X0B4 - 0X0B5): SAFMACA2H

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Source Filtering MAC Address 2 High** The most significant word of MAC Address 2.

0x0BC - 0x0C7: Reserved

4.14 TXQ Rate Control Registers

Port 1 TXQ Rate Control Register 1 (0x0C8 - 0x0C9): P1TXQRCR1

This register contains the q2 and q3 rate control bits for Port 1.

TABLE 4-87: PORT 1 TXQ RATE CONTROL REGISTER 1 (0X0C8 - 0X0C9): P1TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 1 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 2 within a certain time.
14 - 8	0x04	RW	**Port 1 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high-priority packet can transmit within a given period.
7	1	RW	**Port 1 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 3 within a certain time.
6 - 0	0x08	RW	**Port 1 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

Port 1 TXQ Rate Control Register 2 (0x0CA - 0x0CB): P1TXQRCR2

This register contains the q0 and q1 rate control bits for Port 1.

TABLE 4-88: PORT 1 TXQ RATE CONTROL REGISTER 2 (0X0CA - 0X0CB): P1TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 1 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 0 within a certain time.
14 - 8	0x01	RW	**Port 1 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 1 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 1 within a certain time.
6 - 0	0x02	RW	**Port 1 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

Port 2 TXQ Rate Control Register 1 (0x0CC - 0x0CD): P2TXQRCR1

This register contains the q2 and q3 rate control bits for Port 2.

TABLE 4-89: PORT 2 TXQ RATE CONTROL REGISTER 1 (0X0CC - 0X0CD): P2TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 2 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 2 within a certain time.
14 - 8	0x04	RW	**Port 2 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high-priority packet can transmit within a given period.
7	1	RW	**Port 2 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 3 within a certain time.
6 - 0	0x08	RW	**Port 2 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

Port 2 TXQ Rate Control Register 2 (0x0CE - 0x0CF): P2TXQRCR2

This register contains the q0 and q1 rate control bits for Port 1.

TABLE 4-90: PORT 2 TXQ RATE CONTROL REGISTER 2 (0X0CE - 0X0CF): P2TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 2 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 0 within a certain time.
14 - 8	0x01	RW	**Port 2 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 2 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 1 will transmit all the packets from this priority queue 1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 1 within a certain time.
6 - 0	0x02	RW	**Port 2 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

Port 3 TXQ Rate Control Register 1 (0x0D0 - 0x0D1): P3TXQRCR1

This register contains the q2 and q3 rate control bits for Port 3.

TABLE 4-91: PORT 3 TXQ RATE CONTROL REGISTER 1 (0X0D0 - 0X0D1): P3TXQRCR1

Bit	Default	R/W	Description
15	1	RW	**Port 3 Transmit Queue 2 (high) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority queue 2 before transmit lower priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 2 within a certain time.
14 - 8	0x04	RW	**Port 3 Transmit Queue 2 (high) Ratio** This ratio indicates the number of packet for high-priority packet can transmit within a given period.
7	1	RW	**Port 3 Transmit Queue 3 (highest) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority queue 3 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 3 within a certain time.
6 - 0	0x08	RW	**Port 3 Transmit Queue 3 (highest) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

Port 3 TXQ Rate Control Register 2 (0x0D2 - 0x0D3): P3TXQRCR2

This register contains the q0 and q1 rate control bits for Port 3.

TABLE 4-92: PORT 3 TXQ RATE CONTROL REGISTER 2 (0X0D2 - 0X0D3): P3TXQRCR2

Bit	Default	R/W	Description
15	1	RW	**Port 3 Transmit Queue 0 (lowest) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority queue 0 after transmit higher priority queue. 1 = Bit[14:8] reflect the number of packets allow to transmit from this priority queue 0 within a certain time.
14 - 8	0x01	RW	**Port 3 Transmit Queue 0 (lowest) Ratio** This ratio indicates the number of packet for lowest priority packet can transmit within a given period.
7	1	RW	**Port 3 Transmit Queue 1 (low) Ratio Control** 0 = Strict priority. Port 3 will transmit all the packets from this priority queue 1 before transmit lower priority queue. 1 = Bit[6:0] reflect the number of packets allow to transmit from this priority queue 1 within a certain time.
6 - 0	0x02	RW	**Port 3 Transmit Queue 1 (low) Ratio** This ratio indicates the number of packet for highest priority packet can transmit within a given period.

0x0D4 - 0x0DB: Reserved

4.15 Auto-Negotiation Next Page Registers

Port 1 Auto-Negotiation Next Page Transmit Register (0x0DC - 0x0DD): P1ANPT

This register contains the Port 1 auto-negotiation next page transmit related bits.

TABLE 4-93: PORT 1 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER (0X0DC - 0X0DD): P1ANPT

Bit	Default	R/W	Description
15	1	RO	**Next Page** Next page (NP) is used by the next page function to indicate whether or not this is the last next page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.
14	0	RO	**Reserved**
13	0	RO	**Message Page** Message page (MP) is used by the next page function to differentiate a message page from an unformatted page. MP shall be set as follows: 1 = Message page. 0 = Unformatted page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the toggle bit in the previously exchanged link code word. The initial value of the toggle bit in the first next page transmitted is the inverse of bit [11] in the base link code word and, therefore, may assume a value of logic one or zero. The toggle bit shall be set as follows: 1 = Previous value of the transmitted link code word equal to logic zero. 0 = Previous value of the transmitted link code word equal to logic one.
10 - 0	0	RO	**Message and Unformatted Code Field** Message/Unformatted code field bits [10:0]

Port 1 Auto-Negotiation Link Partner Received Next Page Register (0x0DE - 0x0DF): P1ALPRNP

This register contains the Port 1 auto-negotiation link partner received next page related bits.

TABLE 4-94: PORT 1 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0DE - 0X0DF): P1ALPRNP

Bit	Default	R/W	Description
15	1	RO	**Next Page** Next page (NP) is used by the next page function to indicate whether or not this is the last next page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.

TABLE 4-94: PORT 1 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0DE - 0X0DF): P1ALPRNP (CONTINUED)

Bit	Default	R/W	Description
14	0	RO	**Acknowledge** Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its link partner's link code word. The acknowledge bit is encoded in bit [14] regardless of the value of the selector field or link code word encoding. If no next page information is to be sent, this bit shall be set to logic one in the link code word after the reception of at least three consecutive and consistent FLP Bursts (ignoring the acknowledge bit value).
13	0	RO	**Message Page** Message page (MP) is used by the next page function to differentiate a message page from an unformatted page. MP shall be set as follows: 1 = Message page. 0 = Unformatted page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the toggle bit in the previously exchanged link code word. The initial value of the toggle bit in the first next page transmitted is the inverse of bit [11] in the base link code word and, therefore, may assume a value of logic one or zero. The toggle bit shall be set as follows: 1 = Previous value of the transmitted link code word equal to logic zero. 0 = Previous value of the transmitted link code word equal to logic one.
10 - 0	0	RO	**Message and Unformatted Code Field** Message/Unformatted code field bits [10:0]

4.16 EEE and Link Partner Advertisement Registers

Port 1 EEE and Link Partner Advertisement Register (0x0E0 – 0x0E1): P1EEEA

This register contains the Port 1 EEE advertisement and link partner advertisement information.

TABLE 4-95: PORT 1 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0E0 – 0X0E1): P1EEEA

Bit	Default	R/W	Description
15	0	RO	**Reserved**
14	0	RO	**10GBASE-KR EEE** 1 = Link Partner EEE is supported for 10GBASE-KR. 0 = Link Partner EEE is not supported for 10GBASE-KR.
13	0	RO	**10GBASE-KX4 EEE** 1 = Link Partner EEE is supported for 10GBASE-KX4. 0 = Link Partner EEE is not supported for 10GBASE-KX4.
12	0	RO	**1000BASE-KX EEE** 1 = Link Partner EEE is supported for 1000BASE-KX. 0 = Link Partner EEE is not supported for 1000BASE-KX.

TABLE 4-95: PORT 1 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0E0 – 0X0E1): P1EEEA (CONTINUED)

Bit	Default	R/W	Description
11	0	RO	**10GBASE-T EEE** 1 = Link Partner EEE is supported for 10GBASE-T. 0 = Link Partner EEE is not supported for 10GBASE-T.
10	0	RO	**1000BASE-T EEE** 1 = Link Partner EEE is supported for 1000BASE-T. 0 = Link Partner EEE is not supported for 1000BASE-T
9	0	RO	**100BASE-TX EEE** 1 = Link Partner EEE is supported for 100BASE-TX. 0 = Link Partner EEE is not supported for 100BASE-TX.
8 - 7	0	RO	**Reserved**
6	0	RO	**10GBASE-KR EEE** 1 = Port 1 EEE is supported for 10GBASE-KR. 0 = Port 1 EEE is not supported for 10GBASE-KR.
5	0	RO	**10GBASE-KX4 EEE** 1 = Port 1 EEE is supported for 10GBASE-KX4. 0 = Port 1 EEE is not supported for 10GBASE-KX4.
4	0	RO	**1000BASE-KX EEE** 1 = Port 1 EEE is supported for 1000BASE-KX. 0 = Port 1 EEE is not supported for 1000BASE-KX.
3	0	RO	**10GBASE-T EEE** 1 = Port 1 EEE is supported for 10GBASE−T. 0 = Port 1 EEE is not supported for 10GBASE−T.
2	0	RO	**1000BASE-T EEE** 1 = Port 1 EEE is supported for 1000BASE-T. 0 = Port 1 EEE is not supported for 1000BASE-T.
1	1	RW	**100BASE-TX EEE** 1 = Port 1 EEE is supported for 100BASE-TX. 0 = Port 1 EEE is not supported for 100BASE-TX. To disable EEE capability, clear the Port 1 Next Page Enable bit in the PCSEEEC register (0x0F3).
0	0	RO	**Reserved**

Port 1 EEE Wake Error Count Register (0x0E2 - 0x0E3): P1EEEWEC

This register contains the Port 1 EEE wake error count information.

TABLE 4-96: PORT 2 EEE WAKE ERROR COUNT REGISTER (0X0EE - 0X0EF): P2EEEWEC

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Port 1 EEE Wake Error Count** This counter is incremented by each transition of lpi_wake_timer_done from FALSE to TRUE. It means the Wake-Up time is longer than 20.5 µs. The value will be held at all ones in the case of overflow and will be cleared to zero after this register is read.

Port 1 EEE Control/Status and Auto-Negotiation Expansion Register (0x0E4 - 0x0E5): P1EEECS

This register contains the Port 1 EEE control/status and auto-negotiation expansion information.

TABLE 4-97: PORT 1 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0E4 - 0X0E5): P1EEECS

Bit	Default	R/W	Description
15	1	RW	**Reserved**
14	0	RO	**Hardware 100BT EEE Enable Status** 1 = 100BT EEE is enabled by hardware based NP exchange. 0 = 100BT EEE is disabled.
13	0	RO/LH (Latching High)	**TX LPI Received** 1 = Indicates that the transmit PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
12	0	RO	**TX LPI Indication** 1 = Indicates that the transmit PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the TX LPI signal.
11	0	RO/LH (Latching High)	**RX LPI Received** 1 = Indicates that the receive PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
10	0	RO	**RX LPI Indication** 1 = Indicates that the receive PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the RX LPI signal.
9 - 8	00	RW	**Reserved**
7	0	RO	**Reserved**
6	1	RO	**Received Next Page Location Able** 1 = Received Next Page storage location is specified by bit [6:5]. 0 = Received Next Page storage location is not specified by bit [6:5].
5	1	RO	**Received Next Page Storage Location** 1 = Link partner Next Pages are stored in P1ALPRNP (Reg. 0x0DE - 0x0DF). 0 = Link partner Next Pages are stored in P1ANLPR (Reg. 0x056 - 0x057).
4	0	RO/LH (Latching High)	**Parallel Detection Fault** 1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the parallel detection function.This bit is cleared after read.
3	0	RO	**Link Partner Next Page Able** 1 = Link partner is Next Page abled. 0 = Link partner is not Next Page abled.

TABLE 4-97: PORT 1 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0E4 - 0X0E5): P1EEECS

Bit	Default	R/W	Description
2	1	RO	**Next Page Able** 1 = Local device is Next Page abled. 0 = Local device is not Next Page abled.
1	0	RO/LH (Latching High)	**Page Received** 1 = A New Page has been received. 0 = A New Page has not been received.
0	0	RO	**Link Partner Auto-Negotiation Able** 1 = Link partner is auto-negotiation abled. 0 = Link partner is not auto-negotiation abled.

Port 1 LPI Recovery Time Counter Register (0x0E6): P1LPIRTC

This register contains the Port 1 LPI recovery time counter information.

TABLE 4-98: PORT 1 LPI RECOVERY TIME COUNTER REGISTER (0X0E6): P1LPIRTC

Bit	Default	R/W	Description
7 - 0	0x27 (25 µs)	RW	**Port 1 LPI Recovery Time Counter** This register specifies the time that the MAC device has to wait before it can start to send out packets. This value should be the maximum of the LPI recovery time between local device and remote device. Each count = 640 ns.

Buffer Load to LPI Control 1 Register (0x0E7): BL2LPIC1

This register contains the buffer load to LPI control 1 information.

TABLE 4-99: BUFFER LOAD TO LPI CONTROL 1 REGISTER (0X0E7): BL2LPIC1

Bit	Default	R/W	Description
7	0	RW	**LPI Terminated by Input Traffic Enable** 1 = LPI request will be stopped if input traffic is detected. 0 = LPI request won't be stopped by input traffic.
6	0	RO	**Reserved**
5 - 0	0x08	RW	**Buffer Load Threshold for Source Port LPI Termination** This value defines the maximum buffer usage allowed for a single port before it starts to trigger the LPI termination for the specific source port (512 bytes per unit).

Port 2 Auto-Negotiation Link Partner Received Next Page Register (0x0E8 - 0x0E9): P2ANPT

This register contains the Port 2 auto-negotiation link partner received next page related bits.

TABLE 4-100: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0E8 - 0X0E9): P2ANPT

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next page (NP) is used by the next page function to indicate whether or not this is the last next page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.
14	0	RO	**Reserved**

TABLE 4-100: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0E8 - 0X0E9): P2ANPT

Bit	Default	R/W	Description
13	1	RO	**Message Page** Message page (MP) is used by the next page function to differentiate a message page from an unformatted page. MP shall be set as follows: 1 = Message page. 0 = Unformatted page.
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the toggle bit in the previously exchanged link code word. The initial value of the toggle bit in the first next page transmitted is the inverse of bit [11] in the base link code word and, therefore, may assume a value of logic one or zero. The toggle bit shall be set as follows: 1 = Previous value of the transmitted link code word equal to logic zero. 0 = Previous value of the transmitted link code word equal to logic one.
10 - 0	0x001	RO	**Message and Unformatted Code Field** Message/Unformatted code field bits [10:0]

Port 2 Auto-Negotiation Link Partner Received Next Page Register (0x0EA - 0x0EB): P2ALPRNP

This register contains the Port 2 auto-negotiation link partner received next page related bits.

TABLE 4-101: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0EA - 0X0EB): P2ALPRNP

Bit	Default	R/W	Description
15	0	RO	**Next Page** Next page (NP) is used by the next page function to indicate whether or not this is the last next page to be transmitted. NP shall be set as follows: 1 = Additional Next Page(s) will follow. 0 = Last page.
14	0	RO	**Acknowledge** Acknowledge (Ack) is used by the auto-negotiation function to indicate that a device has successfully received its link partner's link code word. The acknowledge bit is encoded in bit 14] regardless of the value of the selector field or link code word encoding. If no next page information is to be sent, this bit shall be set to logic one in the link code word after the reception of at least three consecutive and consistent FLP bursts (ignoring the acknowledge bit value).
13	0	RO	**Message Page** Message page (MP) is used by the next page function to differentiate a message page from an unformatted page. MP shall be set as follows: 1 = Message page. 0 = Unformatted page.

TABLE 4-101: PORT 2 AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER (0X0EA - 0X0EB): P2ALPRNP

Bit	Default	R/W	Description
12	0	RO	**Acknowledge 2** Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows: 1 = Able to comply with message. 0 = Unable to comply with message.
11	0	RO	**Toggle** Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the toggle bit in the previously exchanged link code word. The initial value of the toggle bit in the first next page transmitted is the inverse of bit [11] in the base link code word and, therefore, may assume a value of logic one or zero. The toggle bit shall be set as follows: 1 = Previous value of the transmitted link code word equal to logic zero. 0 = Previous value of the transmitted link code word equal to logic one.
10 - 0	0x000	RO	**Message and Unformatted Code Field** Message/Unformatted code field bits [10:0]

Port 2 EEE and Link Partner Advertisement Register (0x0EC - 0x0ED): P2EEEA

This register contains the Port 2 EEE advertisement and link partner advertisement information.

TABLE 4-102: PORT 2 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0EC - 0X0ED): P2EEEA

Bit	Default	R/W	Description
15	0	RO	**Reserved**
14	0	RO	**10GBASE-KR EEE** 1 = Link Partner EEE is supported for 10GBASE-KR. 0 = Link Partner EEE is not supported for 10GBASE-KR.
13	0	RO	**10GBASE-KX4 EEE** 1 = Link Partner EEE is supported for 10GBASE-KX4. 0 = Link Partner EEE is not supported for 10GBASE-KX4.
12	0	RO	**1000BASE-KX EEE** 1 = Link Partner EEE is supported for 1000BASE-KX. 0 = Link Partner EEE is not supported for 1000BASE-KX.
11	0	RO	**10GBASE-T EEE** 1 = Link Partner EEE is supported for 10GBASE-T. 0 = Link Partner EEE is not supported for 10GBASE-T.
10	0	RO	**1000BASE-T EEE** 1 = Link Partner EEE is supported for 1000BASE-T. 0 = Link Partner EEE is not supported for 1000BASE-T
9	0	RO	**100BASE-TX EEE** 1 = Link Partner EEE is supported for 100BASE-TX. 0 = Link Partner EEE is not supported for 100BASE-TX.
8 - 7	0	RO	**Reserved**
6	0	RO	**10GBASE-KR EEE** 1 = Port 1 EEE is supported for 10GBASE-KR. 0 = Port 1 EEE is not supported for 10GBASE-KR.
5	0	RO	**10GBASE-KX4 EEE** 1 = Port 1 EEE is supported for 10GBASE-KX4. 0 = Port 1 EEE is not supported for 10GBASE-KX4.

TABLE 4-102: PORT 2 EEE AND LINK PARTNER ADVERTISEMENT REGISTER (0X0EC - 0X0ED): P2EEEA (CONTINUED)

Bit	Default	R/W	Description
4	0	RO	**1000BASE-KX EEE** 1 = Port 1 EEE is supported for 1000BASE-KX. 0 = Port 1 EEE is not supported for 1000BASE-KX.
3	0	RO	**10GBASE-T EEE** 1 = Port 1 EEE is supported for 10GBASE−T. 0 = Port 1 EEE is not supported for 10GBASE−T.
2	0	RO	**1000BASE-T EEE** 1 = Port 1 EEE is supported for 1000BASE-T. 0 = Port 1 EEE is not supported for 1000BASE-T.
1	1	RW	**100BASE-TX EEE** 1 = Port 1 EEE is supported for 100BASE-TX. 0 = Port 1 EEE is not supported for 100BASE-TX. To disable EEE capability, clear the Port 1 Next Page Enable bit in the PCSEEEC register (0x0F3).
0	0	RO	**Reserved**

Port 2 EEE Wake Error Count Register (0x0EE - 0x0EF): P2EEEWEC

This register contains the Port 2 EEE wake error count information.

TABLE 4-103: PORT 2 EEE WAKE ERROR COUNT REGISTER (0X0EE - 0X0EF): P2EEEWEC

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**Port 2 EEE Wake Error Count** This counter is incremented by each transition of lpi_wake_timer_done from FALSE to TRUE. It means the Wake-Up time is longer than 20.5 µs. The value will be held at all ones in the case of overflow and will be cleared to zero after this register is read.

Port 2 EEE Control/Status and Auto-Negotiation Expansion Register (0x0F0 - 0x0F1): P2EEECS

This register contains the Port 2 EEE control/status and auto-negotiation expansion information.

TABLE 4-104: PORT 2 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0F0 - 0X0F1): P2EEECS

Bit	Default	R/W	Description
15	1	RW	**Reserved**
14	0	RO	**Hardware 100BT EEE Enable Status** 1 = 100BT EEE is enabled by hardware based NP exchange. 0 = 100BT EEE is disabled.
13	0	RO/LH (Latching High)	**TX LPI Received** 1 = Indicates that the transmit PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
12	0	RO	**TX LPI Indication** 1 = Indicates that the transmit PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the TX LPI signal.
11	0	RO/LH (Latching High)	**RX LPI Received** 1 = Indicates that the receive PCS has received low power idle (LPI) signaling one or more times since the register was last read. 0 = Indicates that the PCS has not received low power idle (LPI) signaling. The status will be latched high and stay that way until cleared. To clear this status bit, a “1” needs to be written to this register bit.
10	0	RO	**RX LPI Indication** 1 = Indicates that the receive PCS is currently receiving low power idle (LPI) signals. 0 = Indicates that the PCS is not currently receiving low power idle (LPI) signals. This bit will dynamically indicate the presence of the RX LPI signal.
9 - 8	00	RW	**Reserved**
7	0	RO	**Reserved**
6	1	RO	**Received Next Page Location Able** 1 = Received Next Page storage location is specified by bit [6:5]. 0 = Received Next Page storage location is not specified by bit [6:5].
5	1	RO	**Received Next Page Storage Location** 1 = Link partner Next Pages are stored in P2ALPRNP (Reg. 0x0DE - 0x0DF). 0 = Link partner Next Pages are stored in P2ANLPR (Reg. 0x056 - 0x057).
4	0	RO/LH (Latching High)	**Parallel Detection Fault** 1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the parallel detection function.This bit is cleared after read.
3	0	RO	**Link Partner Next Page Able** 1 = Link partner is Next Page abled. 0 = Link partner is not Next Page abled.

TABLE 4-104: PORT 2 EEE CONTROL/STATUS AND AUTO-NEGOTIATION EXPANSION REGISTER (0X0F0 - 0X0F1): P2EEECS

Bit	Default	R/W	Description
2	1	RO	**Next Page Able** 1 = Local device is Next Page abled. 0 = Local device is not Next Page abled.
1	0	RO/LH (Latching High)	**Page Received** 1 = A New Page has been received. 0 = A New Page has not been received.
0	0	RO	**Link Partner Auto-Negotiation Able** 1 = Link partner is auto-negotiation abled. 0 = Link partner is not auto-negotiation abled.

Port 2 LPI Recovery Time Counter Register (0x0F2): P2LPIRTC

This register contains the Port 2 LPI recovery time counter information.

TABLE 4-105: PORT 2 LPI RECOVERY TIME COUNTER REGISTER (0X0F2): P2LPIRTC

Bit	Default	R/W	Description
7 - 0	0x27 (25 µs)	RW	**Port 2 LPI Recovery Time Counter** This register specifies the time that the MAC device has to wait before it can start to send out packets. This value should be the maximum of the LPI recovery time between local device and remote device. Each count = 640 ns.

PCS EEE Control Register (0x0F3): PCSEEEC

This register contains the PCS EEE control information.

TABLE 4-106: PCS EEE CONTROL REGISTER (0X0F3): PCSEEEC

Bit	Default	R/W	Description
7	0	RW	**Reserved**
6	0	RW	**Reserved**
5 - 2	0x0	RO	**Reserved**
1	1	RW	**Port 2 Next Page Enable** 1 = Enable next page exchange during auto-negotiation. 0 = Skip next page exchange during auto-negotiation. Auto-negotiation uses next page to negotiate EEE. To disable EEE auto-negotiation on port 2, clear this bit to zero. Restarting auto-negotiation may then be required..
1	0	RW	**Port 1 Next Page Enable** 1 = Enable next page exchange during auto-negotiation. 0 = Skip next page exchange during auto-negotiation. Auto-negotiation uses next page to negotiate EEE. To disable EEE auto-negotiation on port 1, clear this bit to zero. Restarting auto-negotiation may then be required.

Empty TXQ to LPI Wait Time Control Register (0x0F4 - 0x0F5): ETLWTC

This register contains the empty TXQ to LPI wait time control information.

TABLE 4-107: EMPTY TXQ TO LPI WAIT TIME CONTROL REGISTER (0X0F4 - 0X0F5): ETLWTC

Bit	Default	R/W	Description
15 - 0	0x03E8	RW	**Empty TXQ to LPI Wait Time Control** This register specifies the time that the LPI request will be generated after a TXQ has been empty exceeds this configured time. This is only valid when EEE 100BT is enabled. This setting will apply to all the three ports. The unit is 1.3 ms. The default value is 1.3 sec (in a range from 1.3 ms to 86 seconds).

Buffer Load to LPI Control 2 Register (0x0F6 - 0x0F7): BL2LPIC2

This register contains the buffer load to LPI control 2 information.

TABLE 4-108: BUFFER LOAD TO LPI CONTROL 2 REGISTER (0X0F6 - 0X0F7): BL2LPIC2

Bit	Default	R/W	Description
15 - 8	0x00	RO	**Reserved**
7 - 0	0x04	RW	**Buffer Load Threshold for All Ports LPI Termination** This value defines the maximum buffer usage allowed for a single port before it starts to trigger the LPI termination for every port (128 bytes per unit).

0x0F8 - 0x0FF: Reserved

4.17 Internal I/O Register Space Mapping for Interrupts, BIU, and Global Reset (0x100 - 0x1FF)

0x100 - 0x107: Reserved

Chip Configuration Register (0x108 - 0x109): CCR

This register indicates the chip configuration mode based on strapping and bonding options.

TABLE 4-109: CHIP CONFIGURATION REGISTER (0X108 - 0X109): CCR

Bit	Default	R/W	Description
15 - 11	—	RO	**Reserved**
10	—	RO	**Bus Endian Mode** The P2LED0/LEBE pin value is latched into this bit during power-up/reset. 0 = Bus in Big Endian mode 1 = Bus in Little Endian mode
9	—	RO	**EEPROM Presence** The PME/EEPROM pin value is latched into this bit during power-up/reset. 0 = No external EEPROM 1 = Use external EEPROM
8	0	RO	**Reserved**
7	—	RO	**8-Bit Data Bus Width** This bit value is loaded from P1LED0/H816 (pin 60) to indicate the data bus mode. 0 = Not in 8-bit bus mode operation 1 = In 8-bit bus mode operation

TABLE 4-109: CHIP CONFIGURATION REGISTER (0X108 - 0X109): CCR (CONTINUED)

Bit	Default	R/W	Description
6	—	RO	**16-Bit Data Bus Width** This bit value is loaded from P1LED0/H816 (pin 60) to indicate the data bus mode. 0 = Not in 16-bit bus mode operation 1 = In 16-bit bus mode operation
5	0	RO	**Reserved**
4	1	RO	**Shared Data Bus Mode for Data and Address** 0 = Not valid 1 = Data and address bus are shared.
3 - 0	0x2	RO	**Reserved**

0x10A - 0x10F: Reserved

4.18 Host MAC Address Registers: MARL, MARM, and MARH

These Host MAC address registers are loaded starting at word location 0x1 of the EEPROM upon hardware reset. The software driver can read or write these registers value, but it will not modify the original Host MAC address value in the EEPROM. These six bytes of Host MAC address in external EEPROM are loaded to these three registers as mapping below:

- MARL[15:0] = EEPROM 0x1(MAC Byte 2 and 1)
- MARM[15:0] = EEPROM 0x2(MAC Byte 4 and 3)
- MARH[15:0] = EEPROM 0x3(MAC Byte 6 and 5)

The Host MAC address is used to define the individual destination address that the KSZ8852 responds to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received from right to left (LSB to MSB). For example, the actual transmitted and received bits are on the order of 10000000 11000100 10100010 11100110 10010001 11010101. These three registers value for Host MAC address 01:23:45:67:89:AB will be held as below:

- MARL[15:0] = 0x89AB
- MARM[15:0] = 0x4567
- MARH[15:0] = 0x0123

Host MAC Address Register Low (0x110 – 0x111): MARL

The following table shows the register bit fields for low word of Host MAC address.

TABLE 4-110: HOST MAC ADDRESS REGISTER LOW (0X10 – 0X11): MARL

Bit	Default	R/W	Description
15 - 0	—	RW	**MARL MAC Address Low** The least significant word of the MAC address.

Host MAC Address Register Middle (0x112 – 0x113): MARM

The following table shows the register bit fields for middle word of Host MAC address.

TABLE 4-111: HOST MAC ADDRESS REGISTER MIDDLE (0X112 – 0X113): MARM

Bit	Default	R/W	Description
15 - 0	—	RW	**MARM MAC Address Middle** The middle word of the MAC address.

Host MAC Address Register High (0x114 – 0x115): MARH

The following table shows the register bit fields for high word of Host MAC address.

TABLE 4-112: HOST MAC ADDRESS REGISTER HIGH (0X114 – 0X115): MARH

Bit	Default	R/W	Description
15 - 0	—	RW	**MARH MAC Address High** The Most significant word of the MAC address.

0x116 - 0x121: Reserved

EEPROM Control Register (0x122 – 0x123): EEPCR

To support an external EEPROM, the PME/EEPROM pin should be pulled-up to high; otherwise, it should be pulled-down to low. If an external EEPROM is not used, the software should program the host MAC address. If an EEPROM is used in the design, the chip host MAC address can be loaded from the EEPROM immediately after reset. The KSZ8852 allows the software to access (read or write) the EEPROM directly; that is, the EEPROM access timing can be fully controlled by the software if the EEPROM software access bit is set.

TABLE 4-113: EEPROM CONTROL REGISTER (0X122 – 0X123): EEPCR

Bit	Default	R/W	Description
15 - 6	—	RO	**Reserved**
5	0	WO	**EESRWA EEPROM Software Read or Write Access** 0 = S/W read enable to access EEPROM when software access enabled (bit[4] = “1”) 1 = S/W write enable to access EEPROM when software access enabled (bit[4] = “1”).
4	0	RW	**EESA EEPROM Software Access** 1 = Enable software to access EEPROM through bits [3:0]. 0 = Disable software to access EEPROM.
3	—	RO	**EESB EEPROM Status Bit** Data Receive from EEPROM. This bit directly reads the EEDIO pin.
2	0	RW	**EECB_EEPROM_WR_DATA** Write Data to EEPROM. This bit directly controls the device’s EEDIO pin.
1	0	RW	**EECB_EEPROM_Clock** Serial EEPROM Clock. This bit directly controls the device’s EESK pin.
0	0	RW	**EECB_EEPROM_CS** Chip Select for the EEPROM. This bit directly controls the device’s EECS pin.

Memory BIST Info Register (0x124 – 0x125): MBIR

This register indicates the built-in self-test results for both TX and RX memories after power-up/reset. The device should be reset after the BIST procedure to ensure proper subsequent operation.

TABLE 4-114: MEMORY BIST INFO REGISTER (0X124 – 0X125): MBIR

Bit	Default	R/W	Description
15	0	RO	**Memory BIST Done** 0 = BIST In progress 1 = BIST Done
14 - 13	00	RO	**Reserved**
12	—	RO	**TXMBF TX Memory BIST Completed** 0 = TX Memory built-in self-test has not completed. 1 = TX Memory built-in self-test has completed.

TABLE 4-114: MEMORY BIST INFO REGISTER (0X124 – 0X125): MBIR (CONTINUED)

Bit	Default	R/W	Description
11	—	RO	**TXMBFA TX Memory BIST Failed** 0 = TX Memory built-in self-test has completed without failure. 1 = TX Memory built-in self-test has completed with failure.
10 - 8	—	RO	**TXMBFC TX Memory BIST Fail Count** 0 = TX Memory built-in self-test completed with no count failure. 1 = TX Memory built-in self-test encountered a failed count condition.
7 - 5	—	RO	**Reserved**
4	—	RO	**RXMBF RX Memory BIST Completed** 0 = Completion has not occurred for the Memory built-in self-test 1 = Indicates completion of the RX Memory built-in self-test.
3	—	RO	**RXMBFA RX Memory BIST Failed** 0 = No failure with the RX Memory built-in self-test. 1 = Indicates the RX Memory built-in self-test has failed.
2 - 0	—	RO	**RXMBFC RX Memory BIST Test Fail Count** 0 = No count failure for the RX Memory BIST 1 = Indicates the RX Memory built-in self-test failed count.

Global Reset Register (0x126 – 0x127): GRR

This register controls the global functions with information programmed by the CPU.

TABLE 4-115: GLOBAL RESET REGISTER (0X126 – 0X127): GRR

Bit	Default	R0/W	Description
15 - 4	0x000	RW	**Reserved**
3	0	RW	**Memory BIST Start** 1 = Setting this bit will start the Memory BIST. 0 = Setting this bit will stop the Memory BIST.
2	0	RW	**Reserved**
1	0	RW	**QMU Module Soft Reset** 1 = Software reset is active to clear both the TXQ and RXQ memories. 0 = QMU reset is inactive. QMU software reset will flush out all TX/RX packet data inside the TXQ and RXQ memories and reset all the QMU registers to their default value.
0	0	RW	**Global Soft Reset** 1 = Software reset is active. 0 = Software reset is inactive. Global software reset will reset all registers to their default value. The strap-in values are not affected. This bit is not self-clearing. After writing a “1” to this bit, wait for 10ms to elapse then write a “0” for normal operation.

0x128 - 0x129: Reserved

Wakeup Frame Control Register (0x12A – 0x12B): WFCR

This register holds control information programmed by the CPU to control the Wake-Up frame function.

TABLE 4-116: WAKEUP FRAME CONTROL REGISTER (0X12A – 0X12B): WFCR

Bit	Default	R/W	Description
15 - 8	0x00	RO	**Reserved**

TABLE 4-116: WAKEUP FRAME CONTROL REGISTER (0X12A – 0X12B): WFCR (CONTINUED)

Bit	Default	R/W	Description
7	0	RW	**MPRXE** Magic Packet RX Enable When set, it enables the magic packet pattern detection. When reset, the magic packet pattern detection is disabled.
6 - 4	000	RO	**Reserved**
3	0	RW	**WF3E** Wake up Frame 3 Enable When set, it enables the Wake up frame 3 pattern detection. When reset, the Wake up frame 3 pattern detection is disabled.
2	0	RW	**WF2E** Wake up Frame 2 Enable When set, it enables the Wake up frame 2 pattern detection. When reset, the Wake up frame 2 pattern detection is disabled.
1	0	RW	**WF1E** Wake up Frame 1 Enable When set, it enables the Wake up frame 1 pattern detection. When reset, the Wake up frame 1 pattern detection is disabled.
0	0	RW	**WF0E** Wake up Frame 0 Enable When set, it enables the Wake up frame 0 pattern detection. When reset, the Wake up frame 0 pattern detection is disabled.

0x12C - 0x12F: Reserved

Wakeup Frame 0 CRC0 Register (0x130 – 0x131): WF0CRC0

This register contains the expected CRC values of the Wake up frame 0 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-117: WAKEUP FRAME 0 CRC0 REGISTER (0X130 – 0X131): WF0CRC0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0CRC0** Wake up Frame 0 CRC (lower 16 bits) The expected CRC value of a Wake up frame 0 pattern.

Wakeup Frame 0 CRC1 Register (0x132 – 0x133): WF0CRC1

This register contains the expected CRC values of the Wake up frame 0 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-118: WAKEUP FRAME 0 CRC1 REGISTER (0X132 – 0X133): WF0CRC1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0CRC1** Wake up Frame 0 CRC (upper 16 bits). The expected CRC value of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 0 Register (0x134 – 0x135): WF0BM0

This register contains the first 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the first byte of the Wake up frame 0, setting bit 15 selects the 16th byte of the Wake up frame 0.

TABLE 4-119: WAKEUP FRAME 0 BYTE MASK 0 REGISTER (0X134 – 0X135): WF0BM0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0BM0** Wake up Frame 0 Byte Mask 0 The first 16 bytes mask of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 1 Register (0x136 – 0x137): WF0BM1

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 0. Setting bit 15 selects the 32nd byte of the Wake up frame 0.

TABLE 4-120: WAKEUP FRAME 0 BYTE MASK 1 REGISTER (0X136 – 0X137): WF0BM1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0BM1** Wake up Frame 0 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 0 pattern.

Wakeup Frame 0 Byte Mask 2 Register (0x138 – 0x139): WF0BM2

This register contains the next 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 0. Setting bit 15 selects the 48th byte of the Wake up frame 0.

TABLE 4-121: WAKEUP FRAME 0 BYTE MASK 2 REGISTER (0X138 – 0X139): WF0BM2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0BM2** Wake-up Frame 0 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 0 pattern.

Wakeup Frame 0 Byte Mask 3 Register (0x13A – 0x13B): WF0BM3

This register contains the last 16 bytes mask values of the Wake up frame 0 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 0. Setting bit 15 selects the 64th byte of the Wake up frame 0.

TABLE 4-122: WAKEUP FRAME 0 BYTE MASK 3 REGISTER (0X13A – 0X13B): WF0BM3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF0BM3** Wake-up Frame 0 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 0 pattern.

0x13C – 0x13F: Reserved

Wakeup Frame 1 CRC0 Register (0x140 – 0x141): WF1CRC0

This register contains the expected CRC values of the Wake up frame 1 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard; it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-123: WAKEUP FRAME 1 CRC0 REGISTER (0X140 – 0X141): WF1CRC0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1CRC0** Wake-up frame 1 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Wakeup Frame 1 CRC1 Register (0x142 – 0x143): WF1CRC1

This register contains the expected CRC values of the Wake up frame 1 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-124: WAKEUP FRAME 1 CRC1 REGISTER (0X142 – 0X143): WF1CRC1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1CRC1** Wake-up frame 1 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 0 Register (0x144 – 0x145): WF1BM0

This register contains the first 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the first byte of the Wake up frame 1, setting bit 15 selects the 16th byte of the Wake up frame 1.

TABLE 4-125: WAKEUP FRAME 1 BYTE MASK 0 REGISTER (0X144 – 0X145): WF1BM0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1BM0** Wake-up frame 1 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 1 Register (0x146 – 0x147): WF1BM1

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 1. Setting bit 15 selects the 32nd byte of the Wake up frame 1.

TABLE 4-126: WAKEUP FRAME 1 BYTE MASK 1 REGISTER (0X146 – 0X147): WF1BM1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1BM1** Wake-up frame 1 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 2 Register (0x148 – 0x149): WF1BM2

This register contains the next 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 1. Setting bit 15 selects the 48th byte of the Wake up frame 1.

TABLE 4-127: WAKEUP FRAME 1 BYTE MASK 2 REGISTER (0X148 – 0X149): WF1BM2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1BM2** Wake-up frame 1 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 1 pattern.

Wakeup Frame 1 Byte Mask 3 Register (0x14A – 0x14B): WF1BM3

This register contains the last 16 bytes mask values of the Wake up frame 1 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 1. Setting bit 15 selects the 64th byte of the Wake up frame 1.

TABLE 4-128: WAKEUP FRAME 1 BYTE MASK 3 REGISTER (0X4A – 0X4B): WF1BM3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF1BM3** Wake-up frame 1 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 1 pattern.

0x14C – 0x14F: Reserved

Wakeup Frame 2 CRC0 Register (0x150 – 0x151): WF2CRC0

This register contains the expected CRC values of the Wake up frame 2 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-129: WAKEUP FRAME 2 CRC0 REGISTER (0X150 – 0X151): WF2CRC0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2CRC0** Wake-up frame 2 CRC (lower 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Wakeup Frame 2 CRC1 Register (0x152 – 0x153): WF2CRC1

This register contains the expected CRC values of the wake-up frame 2 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake up byte mask registers.

TABLE 4-130: WAKEUP FRAME 2 CRC1 REGISTER (0X152 – 0X153): WF2CRC1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2CRC1** Wake-up frame 2 CRC (upper 16 bits). The expected CRC value of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 0 Register (0x154 – 0x155): WF2BM0

This register contains the first 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the first byte of the Wake up frame 2, setting bit 15 selects the 16th byte of the Wake up frame 2.

TABLE 4-131: WAKEUP FRAME 2 BYTE MASK 0 REGISTER (0X154 – 0X155): WF2BM0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2BM0** Wake-up frame 2 Byte Mask 0. The first 16 bytes mask of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 1 Register (0x156 – 0x157): WF2BM1

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 2. Setting bit 15 selects the 32nd byte of the Wake up frame 2.

TABLE 4-132: WAKEUP FRAME 2 BYTE MASK 1 REGISTER (0X156 – 0X157): WF2BM1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2BM1** Wake-up frame 2 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 2 Register (0x158 – 0x159): WF2BM2

This register contains the next 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 2. Setting bit 15 selects the 48th byte of the Wake up frame 2.

TABLE 4-133: WAKEUP FRAME 2 BYTE MASK 2 REGISTER (0X158 – 0X159): WF2BM2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2BM2** Wake-up frame 2 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake-up frame 2 pattern.

Wakeup Frame 2 Byte Mask 3 Register (0x15A – 0x15B): WF2BM3

This register contains the last 16 bytes mask values of the Wake up frame 2 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 2. Setting bit 15 selects the 64th byte of the Wake up frame 2.

TABLE 4-134: WAKEUP FRAME 2 BYTE MASK 3 REGISTER (0X5A – 0X5B): WF2BM3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF2BM3** Wake-up frame 2 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake-up frame 2 pattern.

0x15C – 0x15F: Reserved

Wakeup Frame 3 CRC0 Register (0x160 – 0x161): WF3CRC0

This register contains the expected CRC values of the Wake up frame 3 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake-up byte mask registers.

TABLE 4-135: WAKEUP FRAME 3 CRC0 REGISTER (0X160 – 0X161): WF3CRC0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3CRC0** Wake-up frame 3 CRC (lower 16 bits). The expected CRC value of a Wake up frame 3 pattern.

Wakeup Frame 3 CRC1 Register (0x162 – 0x163): WF3CRC1

This register contains the expected CRC values of the Wake up frame 3 pattern. The value of the CRC calculated is based on the IEEE 802.3 Ethernet standard, it is taken over the bytes specified in the wake-up byte mask registers.

TABLE 4-136: WAKEUP FRAME 3 CRC1 REGISTER (0X162 – 0X163): WF3CRC1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3CRC1** Wake-up frame 3 CRC (upper 16 bits). The expected CRC value of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 0 Register (0x164 – 0x165): WF3BM0

This register contains the first 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the first byte of the Wake up frame 3, setting bit 15 selects the 16th byte of the Wake up frame 3.

TABLE 4-137: WAKEUP FRAME 3 BYTE MASK 0 REGISTER (0X164 – 0X165): WF3BM0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3BM0** Wake up Frame 3 Byte Mask 0. The first 16 byte mask of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 1 Register (0x166 – 0x167): WF3BM1

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 17th byte of the Wake up frame 3. Setting bit 15 selects the 32nd byte of the Wake up frame 3.

TABLE 4-138: WAKEUP FRAME 3 BYTE MASK 1 REGISTER (0X166 – 0X167): WF3BM1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3BM1** Wake up Frame 3 Byte Mask 1. The next 16 bytes mask covering bytes 17 to 32 of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 2 Register (0x168 – 0x169): WF3BM2

This register contains the next 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 33rd byte of the Wake up frame 3. Setting bit 15 selects the 48th byte of the Wake up frame 3.

TABLE 4-139: WAKEUP FRAME 3 BYTE MASK 2 REGISTER (0X168 – 0X169): WF3BM2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3BM2** Wake up Frame 3 Byte Mask 2. The next 16 bytes mask covering bytes 33 to 48 of a Wake up frame 3 pattern.

Wakeup Frame 3 Byte Mask 3 Register (0x16A – 0x16B): WF3BM3

This register contains the last 16 bytes mask values of the Wake up frame 3 pattern. Setting bit 0 selects the 49th byte of the Wake up frame 3. Setting bit 15 selects the 64th byte of the Wake up frame 3.

TABLE 4-140: WAKEUP FRAME 3 BYTE MASK 3 REGISTER (0X16A – 0X16B): WF3BM3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**WF3BM3** Wake up Frame 3 Byte Mask 3. The last 16 bytes mask covering bytes 49 to 64 of a Wake up frame 3 pattern.

0x16C – 0x16F: Reserved

4.19 Internal I/O Register Space Mapping for the Queue Management Unit (QMU) (0x170 - 0x1FF)

Transmit Control Register (0x170 - 0x171): TXCR

This register holds control information programmed by the CPU to control the QMU transmit module function.

TABLE 4-141: TRANSMIT CONTROL REGISTER (0X170 - 0X171): TXCR

Bit	Default	R/W	Description
15 - 9	—	RO	**Reserved**
8	0	RW	**TCGICMP Transmit Checksum Generation for ICMP** When this bit is set, the device hardware is enabled to generate an ICMP frame checksum in a non-fragmented ICMP frame.
7	0	RW	**TCGUDP Transmit Checksum Generation for UDP** When this bit is set, the device hardware is enabled to generate a UPD frame checksum in a non-fragmented UDP frame.
6	0	RW	**TCGTCP Transmit Checksum Generation for TCP** When this bit is set, the device hardware is enabled to generate a TCP frame checksum in a non-fragmented TCP frame.

TABLE 4-141: TRANSMIT CONTROL REGISTER (0X170 - 0X171): TXCR (CONTINUED)

Bit	Default	R/W	Description
5	0	RW	**FTXQ Flush Transmit Queue** When this bit is set, the transmit queue memory is cleared and TX frame pointer is reset. Note: Disable the TXE transmit enable bit[0] first before setting this bit, then clear this bit to normal operation.
4	0	RW	**TXFCE Transmit Flow Control Enable** When this bit is set and the device is in full-duplex mode, flow control is enabled. The device transmits a PAUSE frame when the receive buffer capacity reaches a threshold level that will cause the buffer to overflow. When this bit is set and the device is in half-duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
3	0	RW	**TXPE Transmit Padding Enable** When this bit is set, the device automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit requires enabling the add CRC feature (bit[1] = “1”) to avoid CRC errors for the transmit packet.
2	0	RW	**TXCE Transmit CRC Enable** When this bit is set, the device automatically adds a 32−bit CRC checksum field to the end of a transmit frame.
0	0	RW	**TXE Transmit Enable** When this bit is set, the transmit module is enabled and placed in a running state. When reset, the transmit process is placed in the stopped state after the transmission of the current frame is completed.

Transmit Status Register (0x172 – 0x173): TXSR

This register keeps the status of the last transmitted frame in the QMU transmit module.

TABLE 4-142: TRANSMIT STATUS REGISTER (0X172 – 0X173): TXSR

Bit	Default	R/W	Description
15 - 14	0x0	RO	**Reserved**
13	0	RO	**TXLC Transmit Late Collision** This bit is set when a transmit Late Collision occurs.
12	0	RO	**TXMC Transmit Maximum Collision** This bit is set when a transmit Maximum Collision is reached.
11 - 6	—	RO	Reserved
5 - 0	—	RO	**TXFID Transmit Frame ID** This field identifies the transmitted frame. All of the transmit status information in this register belongs to the frame with this ID.

Receive Control Register 1 (0x174 – 0x175): RXCR1

This register holds control information programmed by the host to control the receive function in the QMU module.

TABLE 4-143: RECEIVE CONTROL REGISTER 1 (0X174 – 0X175): RXCR1

Bit	Default	R/W	Description
15	0	RW	**FRXQ Flush Receive Queue** When this bit is set, The receive queue memory is cleared and RX frame pointer is reset. Note: Disable the RXE receive enable bit[0] first before set this bit, then clear this bit to normal operation.

TABLE 4-143: RECEIVE CONTROL REGISTER 1 (0X174 – 0X175): RXCR1 (CONTINUED)

Bit	Default	R/W	Description
14	0	RW	**RXUDPFCC Receive UDP Frame Checksum Check Enable** When this bit is set, the KSZ8852 will check for correct UDP checksum for incoming UDP frames. Any received UDP frames with incorrect checksum will be discarded.
13	0	RW	**RXTCPFCC Receive TCP Frame Checksum Check Enable** When this bit is set, the KSZ8852 will check for correct TCP checksum for incoming TCP frames. Any received TCP frames with incorrect checksum will be discarded.
12	0	RW	**RXIPFCC Receive IP Frame Checksum Check Enable** When this bit is set, the KSZ8852 will check for correct IP header checksum for incoming IP frames. Any received IP header with incorrect checksum will be discarded.
11	1	RW	**RXPAFMA Receive Physical Address Filtering with MAC Address Enable** When this bit is set, this bit enables the RX function to receive physical address that pass the MAC address filtering mechanism (see MAC Address Filtering Scheme in Table 3-2 for detail).
10	0	RW	**RXFCE Receive Flow Control Enable** When this bit is set and the KSZ8852 is in full-duplex mode, flow control is enabled, and the KSZ8852 will acknowledge a PAUSE frame from the receive interface; i.e., the outgoing packets are pending in the transmit buffer until the PAUSE frame control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, flow control is not enabled.
9	0	RW	**RXEFE Receive Error Frame Enable** When this bit is set, CRC error frames are allowed to be received into the RX queue. When this bit is cleared, all CRC error frames are discarded.
8	0	RW	**RXMAFMA Receive Multicast Address Filtering with MAC Address Enable** When this bit is set, this bit enables the RX function to receive multicast address that pass the MAC address filtering mechanism (see MAC Address Filtering Scheme in Table 3-2 for detail).
7	0	RW	**RXBE Receive Broadcast Enable** When this bit is set, the RX module receives all the broadcast frames.
6	0	RW	**RXME Receive Multicast Enable** When this bit is set, the RX module receives all the multicast frames (including broadcast frames).
5	0	RW	**RXUE Receive Unicast Enable** When this bit is set, the RX module receives unicast frames that match the 48-bit Station MAC address of the module.
4	0	RW	**RXAE Receive All Enable** When this bit is set, the KSZ8852 receives all incoming frames, regardless of the frame's destination address (see MAC Address Filtering Scheme in Table 3-2 for detail).
3 - 2	0x0	RW	**Reserved**
1	0	RW	**RXINVF Receive Inverse Filtering** When this bit is set, the KSZ8852 receives function with address check operation in inverse filtering mode (see MAC Address Filtering Scheme in Table 3-2 for detail).

TABLE 4-143: RECEIVE CONTROL REGISTER 1 (0X174 – 0X175): RXCR1 (CONTINUED)

Bit	Default	R/W	Description
0	0x0	RW	**RXE Receive Enable** When this bit is set, the RX block is enabled and placed in a running state. When this bit is cleared, the receive process is placed in the stopped state upon completing reception of the current frame.

Receive Control Register 2 (0x176 – 0x177): RXCR2

This register holds control information programmed by the host to control the receive function in the QMU module.

TABLE 4-144: RECEIVE CONTROL REGISTER 2 (0X176 – 0X177): RXCR2

Bit	Default	R/W	Description
15 - 9	—	RO	**Reserved**
8	1	RW	**EQFCPT Enable QMU Flow Control Pause Timer** While this bit is set, another pause frame will be sent out if the pause timer is expired and RXQ (12 KB) is still above the low water mark. The pause timer will reset itself when it expires and RXQ is still above the low water mark and it will be disabled or stop counting when RXQ is below the low water mark. The pause frame is sent out before RXQ is above the high water mark.
7 - 5	0x00	RW	**Reserved**
4	1	RW	**IUFFP IPv4/IPv6/UDP Fragment Frame Pass** While this bit is set, the device will pass the frame without checking the UDP checksum at the received side for IPv6 UDP frames with a fragmented extension header. Operating with this bit cleared is not a valid mode since the hardware cannot calculate a correct UDP checksum without all of the IP fragments.
3	0	RW	**Reserved**
2	1	RW	**UDPLFE UDP Lite Frame Enable** While this bit is set, the KSZ8852 will check the checksum at receive side and generate the checksum at transmit side for UDP lite frame. While this bit is cleared, the KSZ8852 will pass the checksum check at receive side and skip the checksum generation at transmit side for UDP lite frame.
1	0	RW	**RXICMPFCC Receive ICMP Frame Checksum Check Enable** While this bit is set, any received ICMP frame (only a non-fragmented frame) with an incorrect checksum will be discarded. If this bit is not set, the frame will not be discarded even though there is an ICMP checksum error.
0	0	RW	**RXSAF Receive Source Address Filtering** While this bit is set, the device will drop the frame if the source address is the same as the MAC Address in the MARL, MARM, MARH registers.

TXQ Memory Information Register (0x178 – 0x179): TXMIR

This register indicates the amount of free memory available in the TXQ of the QMU module.

TABLE 4-145: TXQ MEMORY INFORMATION REGISTER (0X178 – 0X179): TXMIR

Bit	Default	R/W	Description
15 - 13	—	RO	Reserved
12 - 0	0x1800	RO	**TXMA Transmit Memory Available** The amount of memory available is represented in units of byte. The TXQ memory is used for both frame payload, control word. Note: Software must be written to ensure that there is enough memory for the next transmit frame including control information before transmit data is written to the TXQ.

0x17A - 0x17B: Reserved

Receive Frame Header Status Register (0x17C – 0x17D): RXFHSR

This register indicates the received frame header status information. The received frames are reported in the RXFC register. This register contains the status information for the frame received, and the host processor can read as many times as the frame count value in the RXFC register.

TABLE 4-146: RECEIVE FRAME HEADER STATUS REGISTER (0X17C – 0X17D): RXFHSR

Bit	Default	R/W	Description
15	—	RO	**RXFV Receive Frame Valid** When this bit is set, it indicates that the present frame in the receive packet memory is valid. The status information currently in this location is also valid. When clear, it indicates that there is either no pending receive frame or that the current frame is still in the process of receiving.
14	—	RO	Reserved
13	—	RO	**RXICMPFCS Receive ICMP Frame Checksum Status** When this bit is set, the KSZ8852 received ICMP frame checksum field is incorrect.
12	—	RO	**RXIPFCS Receive IP Frame Checksum Status** When this bit is set, the KSZ8852 received IP header checksum field is incorrect.
11	—	RO	**RXTCPFCS Receive TCP Frame Checksum Status** When this bit is set, the KSZ8852 received TCP frame checksum field is incorrect.
10	—	RO	**RXUDPFCS Receive UDP Frame Checksum Status** When this bit is set, the KSZ8852 received UDP frame checksum field is incorrect.
9 - 8	—	RO	Reserved
7	—	RO	**RXBF Receive Broadcast Frame** When this bit is set, it indicates that this frame has a broadcast address.
6	—	RO	**RXMF Receive Multicast Frame** When this bit is set, it indicates that this frame has a multicast address (including the broadcast address).
5	—	RO	**RXUF Receive Unicast Frame** When this bit is set, it indicates that this frame has a unicast address.
4	—	RO	**Reserved**

TABLE 4-146: RECEIVE FRAME HEADER STATUS REGISTER (0X17C – 0X17D): RXFHSR

Bit	Default	R/W	Description
3	—	RO	**RXFT Receive Frame Type** When this bit is set, it indicates that the frame is an Ethernet-type frame (frame length is greater than 1500 bytes). When clear, it indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames.
2	—	RO	**Reserved**
1	—	RO	**RXRF Receive Runt Frame** When this bit is set, it indicates that a frame was damaged by a collision or had a premature termination before the collision window passed. Runt frames are passed to the host only if the pass bad frame bit is set.
0	—	RO	**RXCE Receive CRC Error** When this bit is set, it indicates that a CRC error has occurred on the current received frame. CRC error frames are passed to the host only if the pass bad frame bit is set.

Receive Frame Header Byte Count Register (0x17E – 0x17F): RXFHBCR

This register indicates the received frame header byte count information. The received frames are reported in the RXFC register. This register contains the total number of bytes information for the frame received, and the host processor can read as many times as the frame count value in the RXFC register.

TABLE 4-147: RECEIVE FRAME HEADER BYTE COUNT REGISTER (0X17E – 0X17F): RXFHBCR

Bit	Default	R/W	Description
15 - 12	—	RO	Reserved
11 - 0	—	RO	**RXBC Receive Byte Count** This field indicates the present received frame byte size. Note: Always read low byte first for 8−bit mode operation.

TXQ Command Register (0x180 – 0x181): TXQCR

This register is programmed by the Host CPU to issue a transmit command to the TXQ. The present transmit frame in the TXQ memory is queued for transmit.

TABLE 4-148: TXQ COMMAND REGISTER (0X180 – 0X181): TXQCR

Bit	Default	R/W	Description
15 - 3	—	RW	Reserved
2	0	RW	Reserved
1	0	RW	**TXQMAM TXQ Memory Available Monitor** When this bit is written as a “1”, the KSZ8852 will generate interrupt (bit [6] in the ISR register) to the CPU when TXQ memory is available based upon the total amount of TXQ space requested by CPU at TXNTFSR (0x19E) register. Note: This bit is self-clearing after the frame is finished transmitting. The software should wait for the bit to be cleared before setting to “1” again.
0	0	RW	**METFE Manual Enqueue TXQ Frame Enable** When this bit is written as “1”, the KSZ8852 will enable the current TX frame in the TX buffer to be queued for transmit one frame at a time. Note: This bit is self-cleared after the frame transmission is complete. The software should wait for the bit to be cleared before setting up another new TX frame.

RXQ Command Register (0x182 – 0x183): RXQCR

This register is programmed by the Host CPU to issue DMA read or write command to the RXQ and TXQ. This register also is used to control all RX thresholds enable and status.

TABLE 4-149: RXQ COMMAND REGISTER (0X82 – 0X83): RXQCR

Bit	Default	R/W	Description
15 - 13	—	RW	**Reserved**
12	—	RO	**RXDTTS RX Duration Timer Threshold Status** When this bit is set, it indicates that RX interrupt is due to the time start at first received frame in RXQ buffer exceeds the threshold set in RX Duration Timer Threshold Register (0x18C, RXDTTR). This bit will be updated when write 1 to bit 13 in ISR register.
11	—	RO	**RXDBCTS RX Data Byte Count Threshold Status** When this bit is set, it indicates that RX interrupt is due to the number of received bytes in RXQ buffer exceeds the threshold set in RX Data Byte Count Threshold Register (0x18E, RXDBCTR). This bit will be updated when write 1 to bit 13 in ISR register.
10	—	RO	**RXFCTS RX Frame Count Threshold Status** When this bit is set, it indicates that RX interrupt is due to the number of received frames in RXQ buffer exceeds the threshold set in RX Frame Count Threshold Register (0x19C, RXFCTR). This bit will be updated when write 1 to bit 13 in ISR register.
9	0	RW	**RXIPHTOE RX IP Header Two-Byte Offset Enable** When this bit is written as 1, the device will enable to add two bytes before frame header in order for IP header inside the frame contents to be aligned with double word boundary to speed up software operation.
8	—	RW	**Reserved**
7	0x0	RW	**RXDTTE RX Duration Timer Threshold Enable** When this bit is written as 1, the KSZ8852 will enable RX interrupt (bit 13 in ISR) when the time start at first received frame in RXQ buffer exceeds the threshold set in RX Duration Timer Threshold Register (0x18C, RXDTTR).
6	0x0	RW	**RXDBCTE RX Data Byte Count Threshold Enable** When this bit is written as 1, the device will enable RX interrupt (bit 13 in ISR) when the number of received bytes in RXQ buffer exceeds the threshold set in RX Data Byte Count Threshold Register (0x18E, RXDBCTR).
5	0x0	RW	**RXFCTE RX Frame Count Threshold Enable** When this bit is written as 1, the device will enable RX interrupt (bit 13 in ISR) when the number of received frames in RXQ buffer exceeds the threshold set in RX Frame Count Threshold Register (0x19C, RXFCTR).
4	0x0	RW	**ADRFE Auto-Dequeue RXQ Frame Enable** When this bit is written as 1, the device will automatically enable RXQ frame buffer dequeue. The read pointer in RXQ frame buffer will be automatically adjusted to next received frame location after current frame is completely read by the host.
3	0x0	WO	**SDA Start DMA Access** When this bit is written as 1, the device allows a DMA operation from the host CPU to access either read RXQ frame buffer or write TXQ frame buffer with AEN, RDN or WRN signals regardless of the address and byte enable signals. All registers access are disabled except this register during this DMA operation. This bit must be set to 0 when DMA operation is finished in order to access the rest of registers.
2 - 1	—	RW	**Reserved**

TABLE 4-149: RXQ COMMAND REGISTER (0X82 – 0X83): RXQCR (CONTINUED)

Bit	Default	R/W	Description
0	0x0	RW	**RRXEF Release RX Error Frame** When this bit is written as 1, the current RX error frame buffer is released. Note: This bit is self-clearing after the frame memory is released. The software should wait for the bit to be cleared before processing new RX frame.

TX Frame Data Pointer Register (0x184 – 0x185): TXFDPR

The value of this register determines the address to be accessed within the TXQ frame buffer. When the AUTO increment is set, It will automatically increment the pointer value on write accesses to the data register.

The counter is incremented by one for every byte access, by two for every word access, and by four for every double word access.

TABLE 4-150: TX FRAME DATA POINTER REGISTER (0X184 – 0X185): TXFDPR

Bit	Default	R/W	Description
15	—	RO	**Reserved**
14	0	RW	**TXFPAI TX Frame Data Pointer Auto Increment** 1: When this bit is set, the TX Frame Data Pointer register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every double word access. 0: When this bit is reset, the TX Frame Data Pointer is manually controlled by the user to access the TX frame location.
13 - 11	—	RO	**Reserved**
10 - 0	0x000	RO	**TXFP TX Frame Pointer** TX Frame Pointer index to the Frame Data register for access. This field reset to next available TX frame location when the TX Frame Data has been enqueued through the TXQ command register.

RX Frame Data Pointer Register (0x186 – 0x187): RXFDPR

The value of this register determines the address to be accessed within the RXQ frame buffer. When the Auto Increment is set, it will automatically increment the RXQ Pointer on read accesses to the data register.

The counter is incremented is by one for every byte access, by two for every word access, and by four for every double word access.

TABLE 4-151: RX FRAME DATA POINTER REGISTER (0X186 – 0X187): RXFDPR

Bit	Default	R/W	Description
15	—	RO	**Reserved**
14	0	RW	**RXFPAI RX Frame Pointer Auto Increment** 1 = When this bit is set, the RXQ Address register increments automatically on accesses to the data register. The increment is by one for every byte access, by two for every word access, and by four for every double word access. 0 = When this bit is reset, the RX frame data pointer is manually controlled by user to access the RX frame location.
13	—	RO	**Reserved**

TABLE 4-151: RX FRAME DATA POINTER REGISTER (0X186 – 0X187): RXFDPR (CONTINUED)

Bit	Default	R/W	Description
12	1	RW	**WST Write Sample Time** This bit is used to select the WRN active to write data valid time as shown in Table 7-1. 0: WRN active to write data valid sample time is range of 8 ns (min) to 16 ns (max). 1: WRN active to write data valid sample time is 4 ns (max).
11	—	WO	**EMS Endian Mode Selection** This bit indicates the mode of the 8/16-bit host interface – either big endian or little endian. The mode is determined at reset or power up by the strap-in function on pin 62, and should not be changed when writing to this register. 0 = Set to little endian mode 1 = Set to big endian mode
10 - 0	0x000	WO	**RXFP RX Frame Pointer** RX Frame data pointer index to the Data register for access. This pointer value must reset to 0x000 before each DMA operation from the host CPU to read RXQ frame buffer.

0x188 - 0x18B: Reserved1

RX Duration Timer Threshold Register (0x18C – 0x18D): RXDTTR

This register is used to program the received frame duration timer threshold.

TABLE 4-152: RX DURATION TIMER THRESHOLD REGISTER (0X18C – 0X18D): RXDTTR

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**RXDTT Receive Duration Timer Threshold** To program received frame duration timer threshold value in 1 µs interval. The maximum value is 0xCFFF. When bit 7 set to 1 in RXQCR register, the KSZ8852 will set RX interrupt (bit 13 in ISR) after the time starts at first received frame in RXQ buffer and exceeds the threshold set in this register.

RX Data Byte Count Threshold Register (0x18E – 0x18F): RXDBCTR

This register is used to program the received data byte count threshold.

TABLE 4-153: RX DATA BYTE COUNT THRESHOLD REGISTER (0X18E – 0X18F): RXDBCTR

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**RXDBCT Receive Data Byte Count Threshold** To program received data byte threshold value in byte count. When bit 6 set to 1 in RXQCR register, the KSZ8852 will set RX interrupt (bit 13 in ISR) when the number of received bytes in RXQ buffer exceeds the threshold set in this register.

4.20 Internal I/O Register Space Mapping for Interrupt Registers (0x190 - 0x193)

Interrupt Enable Register (0x190 – 0x191): IER

This register enables the interrupts from the QMU and other sources.

TABLE 4-154: INTERRUPT ENABLE REGISTER (0X190 – 0X191): IER

Bit	Default	R/W	Description
15	0	RW	**LCIE Link Change Interrupt Enable** 1 = When this bit is set, the link change interrupt is enabled. 0 = When this bit is reset, the link change interrupt is disabled.
14	0	RW	**TXIE Transmit Interrupt Enable** 1 = When this bit is set, the transmit interrupt is enabled. 0 = When this bit is reset, the transmit interrupt is disabled.
13	0	RW	**RXIE Receive Interrupt Enable** 1 = When this bit is set, the receive interrupt is enabled. 0 = When this bit is reset, the receive interrupt is disabled.
12	0	RW	**Reserved**
11	0	RW	**RXOIE Receive Overrun Interrupt Enable** 1 = When this bit is set, the Receive Overrun interrupt is enabled. 0 = When this bit is reset, the Receive Overrun interrupt is disabled.
10	0	RW	Reserved
9	0	RW	**TXPSIE Transmit Process Stopped Interrupt Enable** 1 = When this bit is set, the Transmit Process Stopped interrupt is enabled. 0 = When this bit is reset, the Transmit Process Stopped interrupt is disabled.
8	0	RW	**RXPSIE Receive Process Stopped Interrupt Enable** 1 = When this bit is set, the Receive Process Stopped interrupt is enabled. 2 = When this bit is reset, the Receive Process Stopped interrupt is disabled.
7	0	RW	**Reserved**
6	0	RW	**TXSAIE Transmit Space Available Interrupt Enable** 1 = When this bit is set, the Transmit memory space available interrupt is enabled. 0 = When this bit is reset, the Transmit memory space available interrupt is disabled.
5	0	RW	**RXWFDIE Receive Wake-up Frame Detect Interrupt Enable** 1 = When this bit is set, the Receive wakeup frame detect interrupt is enabled. 0 = When this bit is reset, the Receive wakeup frame detect interrupt is disabled.
4	0	RW	**RXMPDIE Receive Magic Packet Detect Interrupt Enable** 1 = When this bit is set, the Receive magic packet detect interrupt is 0 enabled. 0 = When this bit is reset, the Receive magic packet detect interrupt is disabled.
3	0	RW	**LDIE Linkup Detect Interrupt Enable** 1 = When this bit is set, the wake-up from linkup detect interrupt is enabled. 0 = When this bit is reset, the linkup detect interrupt is disabled.

TABLE 4-154: INTERRUPT ENABLE REGISTER (0X190 – 0X191): IER (CONTINUED)

Bit	Default	R/W	Description
2	0	RW	**EDIE Energy Detect Interrupt Enable** 1 = When this bit is set, the wake-up from energy detect interrupt is enabled. 0 = When this bit is reset, the energy detect interrupt is disabled.
1 - 0	0x0	RO	**Reserved**

Interrupt Status Register (0x192 – 0x193): ISR

This register contains the status bits for all QMU and other interrupt sources. When the corresponding enable bit is set, it causes the interrupt pin to be asserted. This register is usually read by the host CPU and device drivers during interrupt service routine or polling. The register bits are not cleared when read. The user has to write “1” to clear.

TABLE 4-155: INTERRUPT STATUS REGISTER (0X192 – 0X193): ISR

Bit	Default	R/W	Description
15	0	RO (W1C)	**LCIS Link Change Interrupt Status** When this bit is set, it indicates that the link status has changed from link up to link down, or link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
14	0	RO (W1C)	**TXIS Transmit Interrupt Status** When this bit is set, it indicates that the TXQ MAC has transmitted at least a frame on the MAC interface and the QMU TXQ is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
13	0	RO (W1C)	**RXIS Receive Interrupt Status** When this bit is set, it indicates that the QMU RXQ has received at least a frame from the MAC interface and the frame is ready for the host CPU to process. This edge-triggered interrupt status is cleared by writing 1 to this bit.
12	0	RO (W1C)	**Reserved**
11	0	RO (W1C)	**RXOIS Receive Overrun Interrupt Status** When this bit is set, it indicates that the Receive Overrun status has occurred. This edge-triggered interrupt status is cleared by writing 1 to this bit.
10	0	RO (W1C)	**Reserved**
9	0	RO (W1C)	**TXPSIS Transmit Process Stopped Interrupt Status** When this bit is set, it indicates that the Transmit Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
8	0	RO (W1C)	**RXPSIS Receive Process Stopped Interrupt Status** When this bit is set, it indicates that the Receive Process has stopped. This edge-triggered interrupt status is cleared by writing 1 to this bit.
7	0	RO	**Reserved**
6	0	RO (W1C)	**TXSAIS Transmit Space Available Interrupt Status** When this bit is set, it indicates that Transmit memory space available status has occurred. When this bit is reset, the Transmit memory space available interrupt is disabled.
5	0	RO	**RXWFDIS Receive Wakeup Frame Detect Interrupt Status** When this bit is set, it indicates that Receive wakeup frame detect status has occurred. Write “1000” to PMCTRL[5:2] to clear this bit
4	0	RO	**RXMPDIS Receive Magic Packet Detect Interrupt Status** When this bit is set, it indicates that Receive magic packet detect status has occurred. Write “0100” to PMCTRL[5:2] to clear this bit.

TABLE 4-155: INTERRUPT STATUS REGISTER (0X192 – 0X193): ISR (CONTINUED)

Bit	Default	R/W	Description
3	0	RO	**LDIS Linkup Detect Interrupt Status** When this bit is set, it indicates that wake-up from linkup detect status has occurred. Write “0010” to PMCTRL[5:2] to clear this bit.
2	0	RO	**EDIS Energy Detect Interrupt Status** When this bit is set and bit 2=1, bit 0=0 in IER register, it indicates that wake-up from energy detect status has occurred. When this bit is set and bit 2, 0=1 in IER register, it indicates that wake-up from delay energy detect status has occurred. Write “0001” to PMCTRL[5:2] to clear this bit.
1 - 0	0x0	RO	**Reserved**

0x194 - 0x19B: Reserved

4.21 Internal I/O Register Space Mapping for the Queue Management Unit (QMU) (0x19C - 0x1B9)

RX Frame Count & Threshold Register (0x19C -0x19D): RXFCTR

This register is used to program the received frame count threshold.

TABLE 4-156: RX FRAME COUNT & THRESHOLD REGISTER (0X19C -0X19D): RXFCTR

Bit	Default	R/W	Description
15 - 8	0x00	RW	**Reserved**
7 - 0	0x00	RW	**RXFCT Receive Frame Count Threshold** This register is used to program the received frame count threshold value. When bit [5] set to “1” in the RXQCR register, the device will set interrupt bit [13] in the ISR when the number of received frames in RXQ buffer exceeds the threshold set in this register. The count has to be at least equal to or greater than “1” to enable correct functioning of the hardware. A write of “1” to this register while the receive is enabled will result in erratic hardware operation.

TX Next Total Frames Size Register (0x19E – 0x19F): TXNTFSR

This register is used by the host CPU to program the total amount of TXQ buffer space requested for the next transmit.

TABLE 4-157: TX NEXT TOTAL FRAMES SIZE REGISTER (0X19E – 0X19F): TXNTFSR

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**TXNTFSR TX Next TXQ Buffer Frame Space Required** The Host CPU programs the contents of this register to indicate the total amount of TXQ buffer space which is required for the next “one-frame” transmission. It contains the frame size in double-word count (multiples of four bytes). When bit [1] (TXQ memory available monitor) is set to “1” in the TXQCR register, the device will generate interrupt (bit [6] in the ISR register) to the CPU when TXQ memory is available based upon the total amount of TXQ space requested by the CPU in this register.

MAC Address Hash Table Register 0 (0x1A0 – 0x1A1): MAHTR0

The 64-bit MAC address table is used for group address filtering and it is enabled by selecting item 5 “Hash perfect” mode in Table 3-2 (Address Filtering Scheme table).

This value is defined as the six most significant bits from CRC circuit calculation result that is based on 48-bit of DA input. The two most significant bits select one of the four registers to be used, while the others determine which bit within the register.

Multicast table register 0.

TABLE 4-158: MAC ADDRESS HASH TABLE REGISTER 0 (0X1A0 – 0X1A1): MAHTR0

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**HT0 Hash Table 0** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will be dropped. Note: When ”Receive All” (RXCR1, bit[4]) and the “Receive Multicast Addr. Filtering with the MAC Address” (RXCR1, bit [8]) bit is set, all multicast addresses are received regardless of the multicast table value.

MAC Address Hash Table Register 1 (0x1A2 – 0x1A3): MAHTR1

Multicast table register 1.

TABLE 4-159: MAC ADDRESS HASH TABLE REGISTER 1 (0X1A2 – 0X1A3): MAHTR1

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**HT1 Hash Table 1** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will be dropped. Note: When ”Receive All” (RXCR1, bit[4]) and the “Receive Multicast Addr. Filtering with the MAC Address” (RXCR1, bit [8]) bit is set, all multicast addresses are received regardless of the multicast table value.

MAC Address Hash Table Register 2 (0x1A4 – 0x1A5): MAHTR2

Multicast table register 2.

TABLE 4-160: MAC ADDRESS HASH TABLE REGISTER 2 (0X1A4 – 0X1A5): MAHTR2

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**HT2 Hash Table 2** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will be dropped. Note: When ”Receive All” (RXCR1, bit[4]) and the “Receive Multicast Addr. Filtering with the MAC Address” (RXCR1, bit [8]) bit is set, all multicast addresses are received regardless of the multicast table value.

MAC Address Hash Table Register 3 (0x1A6 – 0x1A7): MAHTR3

Multicast table register 3.

TABLE 4-161: MAC ADDRESS HASH TABLE REGISTER 3 (0X1A6 – 0X1A7): MAHTR3

Bit	Default	R/W	Description
15 - 0	0x0000	RW	**HT3 Hash Table 3** When the appropriate bit is set, if the packet received with DA matches the CRC, the hashing function is received without being filtered. When the appropriate bit is cleared, the packet will drop. Note: When “Receive All” (RXCR1, bit[4]) and the “Receive Multicast Addr. Filtering with the MAC Address” (RXCR1, bit [8]) bit is set, all multicast addresses are received regardless of the multicast table value.

0x1A8 - 0x1AF: Reserved

Flow Control Low Watermark Register (0x1B0 – 0x1B1): FCLWR

This register is used to control the flow control for low watermark in QMU RX queue.

TABLE 4-162: FLOW CONTROL LOW WATERMARK REGISTER (0X1B0 – 0X1B1): FCLWR

Bit	Default	R/W	Description
15 - 12	—	RW	Reserved
11 - 0	0x600	RW	**FCLWC Flow Control Low Watermark Configuration** These bits are used to define the QMU RX queue low watermark configuration. It is in double words count and default is 6 KByte available buffer space out of 12 KByte.

Flow Control High Watermark Register (0x1B2 – 0x1B3): FCHWR

This register is used to control the flow control for high watermark in QMU RX queue.

TABLE 4-163: FLOW CONTROL HIGH WATERMARK REGISTER (0X1B2 – 0X1B3): FCHWR

Bit	Default	R/W	Description
15 - 12	—	RW	Reserved
11 - 0	0x0400	RW	**FCHWC Flow Control High Watermark Configuration** These bits are used to define the QMU RX queue high watermark configuration. It is in double words count and default is 4 KByte available buffer space out of 12 KByte.

Flow Control Overrun Watermark Register (0x1B4 – 0x1B5): FCOWR

This register is used to control the flow control for overrun watermark in QMU RX queue.

TABLE 4-164: FLOW CONTROL OVERRUN WATERMARK REGISTER (0X1B4 – 0X1B5): FCOWR

Bit	Default	R/W	Description
15 - 12	—	RW	Reserved
11 - 0	0x0040	RW	**FCLWC Flow Control Overrun Watermark Configuration** These bits are used to define the QMU RX queue overrun watermark configuration. It is in double words count and default is 256 Bytes available buffer space out of 12 Kbyte.

0x1B6 - 0x1B7: Reserved

RX Frame Count Register (0x1B8 - 0x1B9): RXFC

This register indicates the current total amount of received frame count in RXQ frame buffer.

TABLE 4-165: RX FRAME COUNT REGISTER (0X1B8 - 0X1B9): RXFC

Bit	Default	R/W	Description
15 - 8	0x00	RO	**RXFC RX Frame Count** Indicates the total received frames in RXQ frame buffer when the receive interrupt (bit [13] = “1” in the ISR) occurred and a '1' is written to clear this bit [13] in the ISR. The host CPU can start to read the updated receive frame header information in RXFHSR/RXFHBCR registers after reading the RX frame count register.
7 - 0	0x00	RW	**Reserved**

0x1BA - 0x747: Reserved

Analog Control 1 Register (0x748 - 0x749): ANA_CNTRL_1

This register contains control bits for the Analog Block.

TABLE 4-166: ANALOG CONTROL 1 REGISTER (0X748 - 0X749): ANA_CNTRL_1

Bit	Default	R/W	Description
15 - 8	0x00	RW	**Reserved**
7	0	RW	LDO Off This bit is used to control the on/off state of the internal Low Voltage regulator. 0 = LDO on (default) 1 = Turn LDO off
6 - 0	0x00	RW	**Reserved**

0x74A - 0x74B: Reserved

Analog Control 1 Register (0x74C - 0x74D): ANA_CNTRL_3

This register contains control bits for the Analog Block.

TABLE 4-167: ANALOG CONTROL 1 REGISTER (0X74C - 0X74D): ANA_CNTRL_3

Bit	Default	R/W	Description
15	0	RW	**HIPLS3 Mask** This bit must be set prior to initiating the LINK MD function.
14 - 4	0x00	RW	**Reserved**
3	0	RW	**BTRX Reduce** This bit must be set prior to initiating the LINK MD function.
2 - 0	0x00	RW	**Reserved**

0x74E - 0x7FF: Reserved

4.22 Management Information Base (MIB) Counters

The KSZ8852 provides 34 MIB counters for each port. These counters are used to monitor the port activity for network management. The MIB counters are formatted “per port” and “all ports dropped packet” as shown in Table 4-168.

Format of Per-Port MIB Counters

This register contains control bits for the Analog Block.

TABLE 4-168: FORMAT OF PER-PORT MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = Counter overflow. 0 = No counter overflow.	0
30	Count Valid	RO	1 = Counter value is valid. 0 = Counter value is not valid.	0
29 - 0	Counter Values	RO	Counter value (read clear)	0x00000000

“Per-port” MIB counters are read using indirect memory access. The base address offsets and address ranges for all three ports are:

- Port 1 base address is 0x00 and range is from 0x00 to 0x1F.
- Port 2 base address is 0x20 and range is from 0x20 to 0x3F.
- Port 3 base address is 0x40 and range is from 0x40 to 0x5F.

Per-port MIB counters are read using indirect access control in the IACR register and the indirect access data registers in IADR4[15:0], IADR5[31:16] (0x02C - 0x02F). The Port 1 MIB counters address memory offset as shown in Table 4-169.

TABLE 4-169: PORT 1 MIB COUNTERS – INDIRECT MEMORY OFFSET

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets.
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets.
0x2	RxUndersizePkt	Rx undersize packets with good CRC.
0x3	RxFragments	Rx fragment packets with bad CRC, symbol errors or alignment errors.
0x4	RxOversize	Rx oversize packets with good CRC (maximum: 2000 bytes).
0x5	RxJabbers	Rx packets longer than 1522 bytes with either CRC errors, alignment errors, or symbol errors (depends on max packet size setting).
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size.
0x7	RxCRCError	Rx packets within (64,1522) bytes w/ an integral number of bytes and a bad CRC (upper limit depends on maximum packet size setting).
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/ a non-integral number of bytes and a bad CRC (upper limit depends on maximum packet size setting).
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in Ether-Type field.
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B minimum), and a valid CRC.
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets).
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets).
0xD	RxUnicast	Rx good unicast packets.
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length.
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.

TABLE 4-169: PORT 1 MIB COUNTERS – INDIRECT MEMORY OFFSET (CONTINUED)

Offset	Counter Name	Description
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
0x13	Rx1024to2000Octets	Total Rx packets (bad packets included) that are between 1024 and 2000 octets in length (upper limit depends on max packet size setting).
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets.
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port.
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multi-cast packets).
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets).
0x1A	TxUnicastPkts	Tx good unicast packets.
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.
0x1C	TxTotalCollision	Tx total collision, half duplex only.
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions.
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.

TABLE 4-170: "ALL PORTS DROPPED PACKET" MIB COUNTER FORMAT

Bit	Default	R/W	Description
30 - 16	—	N/A	Reserved
15 - 0	0x0000	RO	Counter Value

Note: "All ports dropped packet" MIB Counters do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

All ports dropped packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 4-174.

TABLE 4-171: "ALL PORTS DROPPED PACKET" MIB COUNTERS− INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port 1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port 2 TX Drop Packets	TX packets dropped due to lack of resources
0x102	Port 3 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port 1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port 2 RX Drop Packets	RX packets dropped due to lack of resources
0x105	Port 3 RX Drop Packets	RX packets dropped due to lack of resources

MIB Counter Examples:

1. MIB Counter Read (read port 1 "Rx64Octets" counter at indirect address offset 0x0E)

Write to Reg. IACR (0xC8) with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR5 (MIB counter value [31:16]) // If bit [31] = 1, there was a counter overflow, // If bit [30] = 0, restart (re-read) from this register

Read Reg. IADR4 (MIB counter value 15-0)

2. MIB Counter Read (read Port 2 “Rx64Octets” counter at indirect address offset 0x2E)

Write to Reg. IACR with 0x1c2e (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR5 (MIB counter value [31:16]) // If bit [31] = 1, there was a counter overflow, // If bit [30] = 0, restart (re-read) from this register

Read Reg. IADR4 (MIB counter value [15:0])

3. MIB Counter Read (read “Port 1 TX Drop Packets” counter at indirect address offset 0x100)

Write to Reg. IACR with 0x1D00 (set indirect address and trigger a read MIB counters operation)

Then:

Read Reg. IADR4 (MIB counter value [15:0])

4.22.1 ADDITIONAL MIB INFORMATION

Per port MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.

All ports dropped packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

4.23 Static MAC Address Table

The KSZ8852 supports both a static and a dynamic MAC address table. In response to a destination address (DA) look up, the KSZ8852 searches both tables to make a packet forwarding decision. In response to a source address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. These entries in Table 7-1 will not be aged out by the KSZ8852.

TABLE 4-172: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Name	R/W	Description
57 - 54	0000	RW	**FID** Filter VLAN ID − identifies one of the 16 active VLANs.
53	0	R/W	**Use FID** 1 = Specifies the use of FID+MAC for static table look up. 0 = Specifies only the use of MAC for static table look up.
52	0	R/W	**Override** 1 = Overrides the port setting transmit enable = “0” or receive enable = “0” setting. 0 = Specifies no override. Note: The Override bit also allows usage (turns on the entry) even if the Valid bit = “0”.
51	0	R/W	**Valid** 1 = Specifies that this entry is valid, and the look up result will be used. 0 = Specifies that this entry is not valid.

TABLE 4-172: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Name	R/W	Description
50 - 48	000	R/W	**Forwarding Ports** These 3 bits control the forwarding port(s): 000 = No forward. 001 = Forward to Port 1. 010 = Forward to Port 2. 100 = Forward to Port 3. 011 = Forward to Port 1 and Port 2. 110 = Forward to Port 2 and Port 3. 101 = Forward to Port 1 and Port 3. 111 = Broadcasting (excluding the ingress port).
47 - 0	0	R/W	**MAC Address** 48−bit MAC Address

Static MAC Table Lookup Examples:

1. Static Address Table Read (read the second entry at indirect address offset 0x01)

Write to Reg. IACR with 0x1001 (set indirect address and trigger a read static MAC table operation)

Then:

Read Reg. IADR3 (static MAC table bits [57:48])

Read Reg. IADR2 (static MAC table bits [47:32])

Read Reg. IADR5 (static MAC table bits [31:16])

Read Reg. IADR4 (static MAC table bits [15:0])

2. Static Address Table Write (write the eighth entry at indirect address offset 0x07)

Write to Reg. IADR3 (static MAC table bits [57:48])

Write to Reg. IADR2 (static MAC table bits[47:32])

Write to Reg. IADR5 (static MAC table bits [31:16])

Write to Reg. IADR4 (static MAC table bits [15:0])

Write to Reg. IACR with 0x0007 (set indirect address and trigger a write static MAC table operation)

4.24 Dynamic MAC Address Table

The Dynamic MAC Address (Table 4-173) is a read-only table.

TABLE 4-173: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES)

Bit	Default	R/W	Description
71	—	RO	**Data Not Ready** 1 = Specifies that the entry is not ready, continue retrying until bit is set to “0”. 0 = Specifies that the entry is ready.
70 - 67	—	RO	**Reserved**
66	1	RO	**MAC Empty** 1 = Specifies that there is no valid entry in the table 0 = Specifies that there are valid entries in the table
65 - 56	0x000	RO	**Number of Valid Entries** Indicates how many valid entries in the table. 0x3ff means 1K entries. 0x001 means 2 entries. 0x000 and bit [66] = “0” means 1 entry. 0x000 and bit [66] = “1” means 0 entry.
55 - 54	—	RO	**Timestamp** Specifies the 2−bit counter for internal aging.

TABLE 4-173: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES) (CONTINUED)

Bit	Default	R/W	Description
53 - 52	00	RO	**Source Port** Identifies the source port where FID+MAC is learned: 00 = Port 1 01 = Port 2 10 = Port 3 (host port)
51 - 48	0x0	RO	**FID** Specifies the filter ID.
47 - 0	0x0000_0000_0000	RO	**MAC Address** Specifies the 48−bit MAC Address.

Dynamic MAC Address Lookup Example:

1. Dynamic MAC Address Table Read (read the first entry at indirect address offset 0 and retrieve the MAC table size)

Write to Reg. IACR with 0x1800 (set indirect address and trigger a read dynamic MAC table operation)

Then:

Read Reg. IADR1 (dynamic MAC table bits [71:64]) // If bit [71] = “1”, restart (re-read) from this register

Read Reg. IADR3 (dynamic MAC table bits [63:48])

Read Reg. IADR2 (dynamic MAC table bits [47:32])

Read Reg. IADR5 (dynamic MAC table bits [31:16])

Read Reg. IADR4 (dynamic MAC table bits [15:0])

4.25 VLAN Table

The KSZ8852 uses the VLAN table to perform look-ups. If 802.1Q VLAN mode is enabled (SGCR2[15]), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (Filter ID), VID (VLAN ID), and VLAN membership as described in Table 4-174:

TABLE 4-174: VLAN TABLE FORMAT (16 ENTRIES)

Bit	Default	R/W	Description
19	1	RW	**Valid** 1 = Specifies that this entry is valid, the look up result will be used. 0 = Specifies that this entry is not valid.
18 - 16	111	R/W	**Membership** Specifies which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example: “101” means Port 3 and Port 1 are in this VLAN.
15 - 12	0x0	R/W	**FID** Specifies the Filter ID. The KSZ8852 supports 16 active VLANs represented by these four bit fields. The FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.
11 - 0	0x001	R/W	**VID** Specifies the IEEE 802.1Q 12 bits VLAN ID.

If 802.1Q VLAN mode is enabled, then KSZ8852 will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, then the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, then VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, then packet will be dropped and no address learning will take place. If the VID is valid, then FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, then the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, then the FID+SA will be learned.

VLAN Table Lookup Examples:

1. VLAN Table Read (read the third entry, at the indirect address offset 0x02)

Write to Reg. IACR with 0x1402 (set indirect address and trigger a read VLAN table operation)

Then:

Read Reg. IADR5 (VLAN table bits [19:16])

Read Reg. IADR4 (VLAN table bits [15:0])

2. VLAN Table Write (write the seventh entry, at the indirect address offset 0x06)

Write to Reg. IADR5 (VLAN table bits [19:16])

Write to Reg. IADR4 (VLAN table bits [15:0])

Write to Reg. IACR with 0x1406 (set indirect address and trigger a read VLAN table operation)

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage ($V_{DD\_A3.3}$, V_{DD_IO}) ..... –0.5V to +5.0V

Supply Voltage (V_{DD_AL}, V_{DD_L}) ..... –0.5V to +1.8V

Input Voltage (All Inputs) ..... –0.5V to +5.0V

Output Voltage (All Outputs) ..... –0.5V to +5.0V

Lead Temperature (soldering, 20s) ..... +260°C

Storage Temperature (T_S) ..... –65°C to +150°C

Maximum Junction Temperature (T_J) ..... +125°C

HBM ESD Rating ..... 2 kV

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

5.2 Operating Ratings**

Supply Voltage

V_{DD_A} (3.3V) ..... +3.135V to +3.465V

V_{DD_L}, V_{DD_AL}, V_{DD_COL} ..... +1.25V to +1.4V

V_{DD_IO} (3.3V) ..... +3.135V to +3.465V

V_{DD_IO} (2.5V) ..... +2.375 to +2.625V

V_{DD_IO} (1.8V) ..... +1.71V to +1.89V

Ambient Operating Temperature (T_A) ..... –40°C to +70°C

Extended Industrial (HLEW) ..... –40°C to +105°C

Extended Industrial (HLEY) ..... –40°C to +115°C

Thermal Resistance (Note 5-1)

Junction-to-Ambient (θ_{JA}) ..... +426°C/W

Junction-to-Case (θ_{JC}) ..... +10.6°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (GROUND to V_{DD_IO}).

Note:	Do not drive input signals without power supplied to the device.

Note 5-1 The θ_{JC}/θ_{JA} is under air velocity 0m/s.

6.0 ELECTRICAL CHARACTERISTICS

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current for 100BASE-TX Operation (Internal Low-Voltage Regulator On, $V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = 3.3V)						
—	$I_{VDD\_A3.3}$	—	42	—	mA	100% Traffic on Both Ports
—	I_{VDD_IO}	—	87	—		
—	$PDISS_{DEVICE}$	—	428	—	mW	
—	$I_{VDD\_A3.3}$	—	41	—	mA	Link, no Traffic on Both Ports, EEE Feature is off.
—	I_{VDD_IO}	—	86	—		
—	$PDISS_{DEVICE}$	—	421	—	mW	
—	$I_{VDD\_A3.3}$	—	4.6	—	mA	Ports 1 and 2 Powered Down (P1CR4, P2CR4 bit[11] = “1”)
—	I_{VDD_IO}	—	70	—		
—	$PDISS_{DEVICE}$	—	246	—	mW	
—	$I_{VDD\_A3.3}$	—	5.5	—	mA	Ports 1 and 2 Not Connected, Using EDPD Feature (PMCTRL bits[1:0] = “01”)
—	I_{VDD_IO}	—	70	—		
—	$PDISS_{DEVICE}$	—	249	—	mW	
—	$I_{VDD\_A3.3}$	—	5.3	—	mA	Ports 1 and 2 Powered Down Using EEE Feature
—	I_{VDD_IO}	—	71	—		
—	$PDISS_{DEVICE}$	—	251	—	mW	
—	$I_{VDD\_A3.3}$	—	0.98	—	mA	Soft Power-Down Mode (PMCTRL bits[1:0] = “10”)
—	I_{VDD_IO}	—	2.0	—		
—	$PDISS_{DEVICE}$	—	10	—	mW	
—	$I_{VDD\_A3.3}$	—	0.18	—	mA	Hardware Power-Down Mode While the PWDRN pin (Pin 17) is held low.
—	I_{VDD_IO}	—	0	—		
—	$PDISS_{DEVICE}$	—	0.6	—	mW	
Supply Current for 100BASE-TX Operation (Internal Low Voltage Regulator Off; $V_{DD\_A3.3}$ and V_{DD_IO} = 3.3V; V_{DD_L}, V_{DD_AL} and V_{DD_COL} = 1.4V) (Note 6-2)						
—	$I_{VDD\_A3.3}$	—	40	—	—	100% Traffic on both ports
—	I_{VDD_IO}	—	0.6	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	88	—	—	
—	$PDISS_{Device}$	—	258	—	—	
—	$I_{VDD\_A3.3}$	—	40	—	—	Link, no traffic on both ports. EEE Feature is off.
—	I_{VDD_IO}	—	0.7	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	87	—	—	
—	$PDISS_{Device}$	—	256	—	—	
—	$I_{VDD\_A3.3}$	—	3.8	—	—	Ports 1 & 2 Powered Down (P1CR4, P2CR4 bit[11] = “1”)
—	I_{VDD_IO}	—	0.5	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	71	—	—	
—	$PDISS_{Device}$	—	114	—	—	

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
—	$I_{VDD\_A3.3}$	—	4.5	—	—	Ports 1 & 2 Not Connected. Using EDPD Feature (PMCTRL bits[1:0] = “01”)
—	I_{VDD_IO}	—	0.6	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	72	—	—	
—	$PDISS_{Device}$	—	117	—	—	
—	$I_{VDD\_A3.3}$	—	5.2	—	—	Ports 1 and 2 Linked, no traffic. Using EEE Feature
—	I_{VDD_IO}	—	0.7	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	74	—	—	
—	$PDISS_{Device}$	—	123	—	—	
—	$I_{VDD\_A3.3}$	—	0.2	—	—	Soft Powerdown Mode (PMCTRL bits[1:0] = “10”)
—	I_{VDD_IO}	—	0.7	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	1.1	—	—	
—	$PDISS_{Device}$	—	4.3	—	—	
—	$I_{VDD\_A3.3}$	—	0.2	—	—	Hardware Powerdown Mode. While the PWDRN pin (Pin 17) is held low.
—	I_{VDD_IO}	—	0.7	—	—	
—	I_{VDD_AL} + I_{VDD_DL}	—	0.1	—	—	
—	$PDISS_{Device}$	—	4.1	—	—	
Supply Current for 10BASE-T Operation (Internal Low Voltage Regulator On; $V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = 3.3V) (Note 6-3)						
—	$I_{VDD\_A3.3}$	—	53	—	mA	100% traffic on both ports
—	I_{VDD_IO}	—	74	—		
—	$PDISS_{DEVICE}$	—	417	—	mV	
—	$I_{VDD\_A3.3}$	—	17	—	mA	Link, no traffic on both ports
—	I_{VDD_IO}	—	71	—		
—	$PDISS_{DEVICE}$	—	290	—	mV	
Supply Current for 10BASE-T Operation (Internal Low Voltage Regulator Off; $V_{DD\_A3.3}$ and V_{DD_IO} = 3.3V; V_{DD_L}, V_{DD_AL} and V_{DD_COL} = 1.4V) (Note 6-3)						
—	$I_{VDD\_A3.3}$	—	51	—	mA	100% traffic on both ports
—	I_{VDD_IO}	—	0.5	—		
—	I_{VDD_AL} + I_{VDD_DL}	—	76	—		
—	$PDISS_{Device}$	—	277	—	mW	
—	$I_{VDD\_A3.3}$	—	16	—	mA	Link, no traffic on both ports
—	I_{VDD_IO}	—	0.6	—		
—	I_{VDD_AL} + I_{VDD_DL}	—	74	—		
—	$PDISS_{Device}$	—	158	—	mW	
Output Voltage at V_{DD_L}	V_{LDO}	—	1.32	—	V	V_{DD_IO} = 2.5V or 3.3V; internal regulator enabled; measured at pins 40 and 51
CMOS Inputs (V_{DD_IO} = 3.3V/2.5V/1.8V)						
Input High Voltage	V_{IH}	2.1/1.7/ 1.3	—	—	V	—

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	V_{IL}	—	—	0.9/0.9/0.6	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DD_IO}
X1 Crystal/Osc Input Pin						
Input High Voltage	V_{IH}	2.1	—	—	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Low Voltage	V_{IL}	—	—	0.9	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Current	I_{IN}	—	—	10	µA	—
PWRDN Input (Note 6-4)						
Input High Voltage	V_{IH}	1.1	—	—	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
Input Low Voltage	V_{IL}	—	—	0.3	V	$V_{DD\_A3.3}$ = 3.3V, V_{DD_IO} = any
CMOS Outputs (V_{DD_IO} = 3.3V/2.5V/1.8V)						
Output High Voltage	V_{OH}	2.4/1.9/1.5	—	—	V	I_{OH} = –8mA
Output Low Voltage	V_{OL}	—	—	0.4/0.4/0.2	V	I_{OL} = 8mA
Output Tri-State Leakage	$\|I_{OZ}\|$	—	—	10	µA	—
100BASE-TX Transmit (Measured Differentially After 1:1 Transformer)						
Peak Differential Output Voltage	V_O	±0.95	—	±1.05	V	100Ω termination on the differential output
Output Voltage Imbalance	V_{imb}	—	—	2	%	100Ω termination on the differential output
Rise/Fall Time	t_r, t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty-Cycle Distortion	—	—	—	±0.25	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.65	—	V	—
Output Jotter	—	—	0.7	1.4	ns	Peak-to-Peak
10BASE-T Receive						
Squelch Threshold	V_{sq}	—	400	—	mV	5 MHz square wave
10BASE-T Transmit (Measured Differentially After 1:1 Transformer)						
Peak Differential Output Voltage	V_P	2.2	2.5	2.8	V	100Ω termination on the differential output
Jitter Added	—	—	1.8	3.5	ns	100Ω termination on the differential output (peak-to-peak)
Rise/Fall Time	t_r, t_f	—	25	—	ns	—
LED Outputs						
Output Drive Current	I_{LED}	—	8	—	mA	Each LED pin (P1/2LED0, P1/2LED1)
I/O Pin Internal Pull-Up and Pull-Down Effective Resistance						
I/O Pin Effective Pull-Up Resistance	R1.8PU	57	100	187	kΩ	V_{DD_IO} = 1.8V
I/O Pin Effective Pull-Down Resistance	R1.8PD	55	100	190		

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
I/O Pin Effective Pull-Up Resistance	R2.5PU	37	59	102	kΩ	V_{DD_IO} = 2.5V
I/O Pin Effective Pull-Down Resistance	R2.5PD	35	60	11		
I/O Pin Effective Pull-Up Resistance	R3.3PU	29	43	70	kΩ	V_{DD_IO} = 3.3V
I/O Pin Effective Pull-Down Resistance	R3.3PD	27	43	76		

Note 6-1 $IV_{DD\_A3.3}$ measured at pin 9. I_{VDD_IO} measured at pins 21, 30, and 56. I_{VDD_AL} measured at pins 6 and 16. I_{VDD_DL} measured at pins 40 and 51.

Note 6-2 T_A = 25°C. Specification for packaged product only.

Note 6-3 The θ_{JC}/θ_{JA} is under air velocity 0m/s.

Note 6-4 For PWRDN pin, pin 17, the operating value of VIH is lower than the other CMOS input pins. It is not dependent on VDD_IO.

7.0 TIMING SPECIFICATIONS

7.1 Host Interface Read / Write Timing

FIGURE 7-1: HOST INTERFACE READ/WRITE TIMING

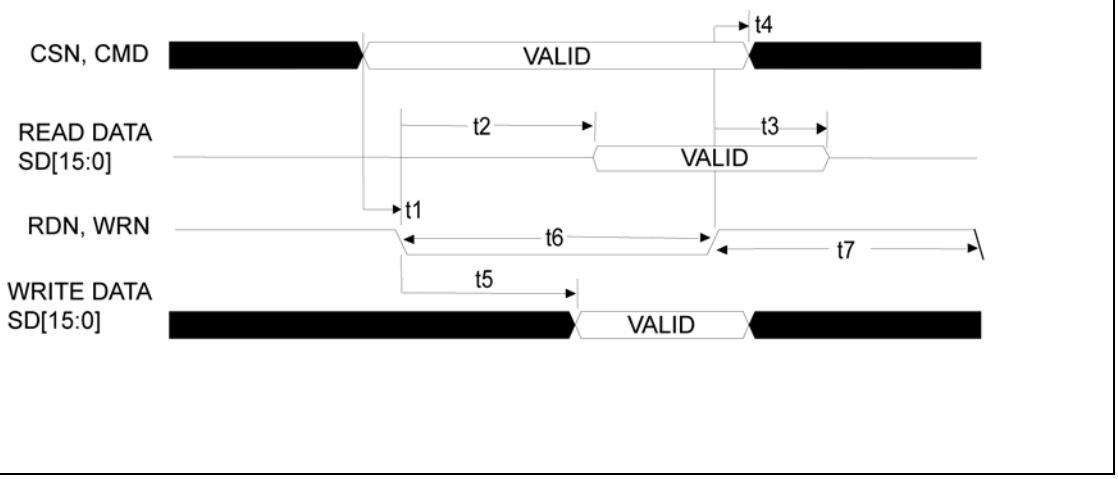


TABLE 7-1: HOST INTERFACE READ/WRITE TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t1	CSN, CMD valid to RDN, WRN active	0	—	—	ns
t2	RDN active to Read Data SD[15:0] valid Note: This is the SD output delay after RDN becomes active until valid read data is available.	24	—	32	ns
t3	RDN inactive to Read data invalid Note: The processor latches valid read data at the rising edge of RDN.	1	—	2	ns
t4	CSN, CMD hold time after RDN, WRN inactive	0	—	—	ns
t5	WRN active to write data valid (bit12=0 in RXFDPR)	8	—	16	ns
	WRN active to write data valid (bit [12] = 1 in RXFDPR) Note: It is better if the processor can provide data in less than 4 ns after WRN is active. If the processor provides data more than 4 ns after WRN is active, make sure that RXFDPR bit [12] = 0.	—	—	4	ns
t6	RDN Read active time (low)	40	—	—	ns
	WRN Write active time (low)	40	—	—	ns
t7	RDN Read Inactive time (high)	10	—	—	ns
	WRN Write inactive time (high)	10	—	—	ns

7.2 Auto-Negotiation Timing

FIGURE 7-2: AUTO-NEGOTIATION TIMING

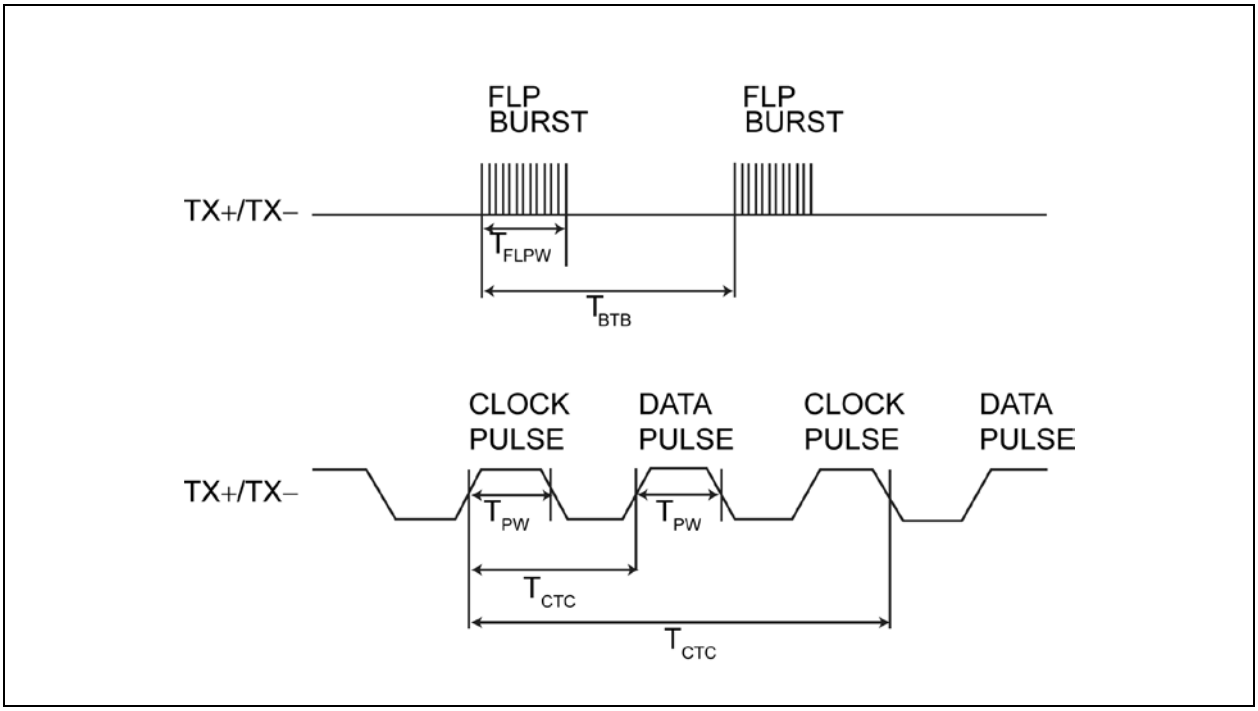


TABLE 7-2: AUTO-NEGOTIATION TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	—	2	—	ms
t_{PW}	Clock/Data pulse width	—	100	—	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
—	Number of Clock/Data pulses per burst	17	—	33	—

7.3 Serial EEPROM Interface Timing

FIGURE 7-3: SERIAL EEPROM TIMING

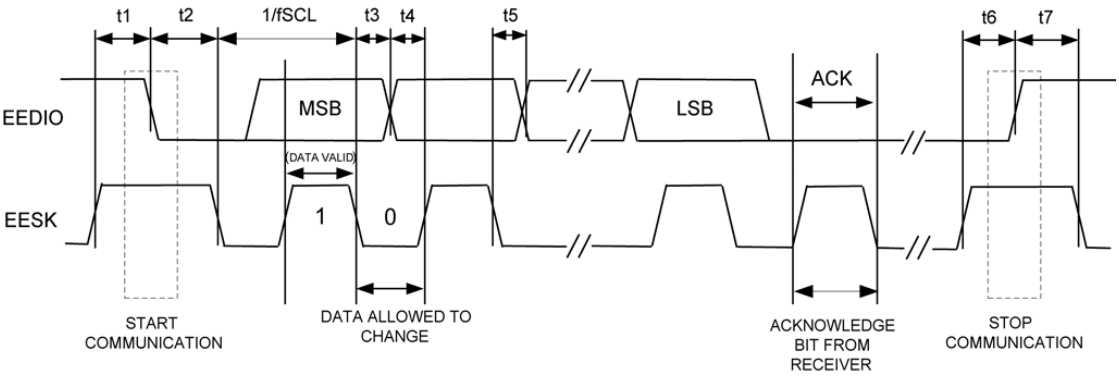


TABLE 7-3: SERIAL EEPROM TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
f_{SCL}	EESK Clock Frequency	—	—	2.5	MHz
t1	Setup Time for Start Bit	33	—	—	ns
t2	Hold Time for Start Bit	33	—	—	ns
t3	Hold Time for Data	20	—	—	ns
t4	Setup Time for Data	33	—	—	ns
t5	Output Valid Time for Data	60	—	—	ns
t6	Setup Time for Stop Bit	33	—	—	ns
t7	Hold Time for Stop Bit	33	—	—	ns

7.4 Reset Timing and Power Sequencing

The KSZ8852 reset timing requirement is summarized in Figure 7-4 and Table 7-4.

FIGURE 7-4: KSZ8852 RESET AND POWER SEQUENCE TIMING

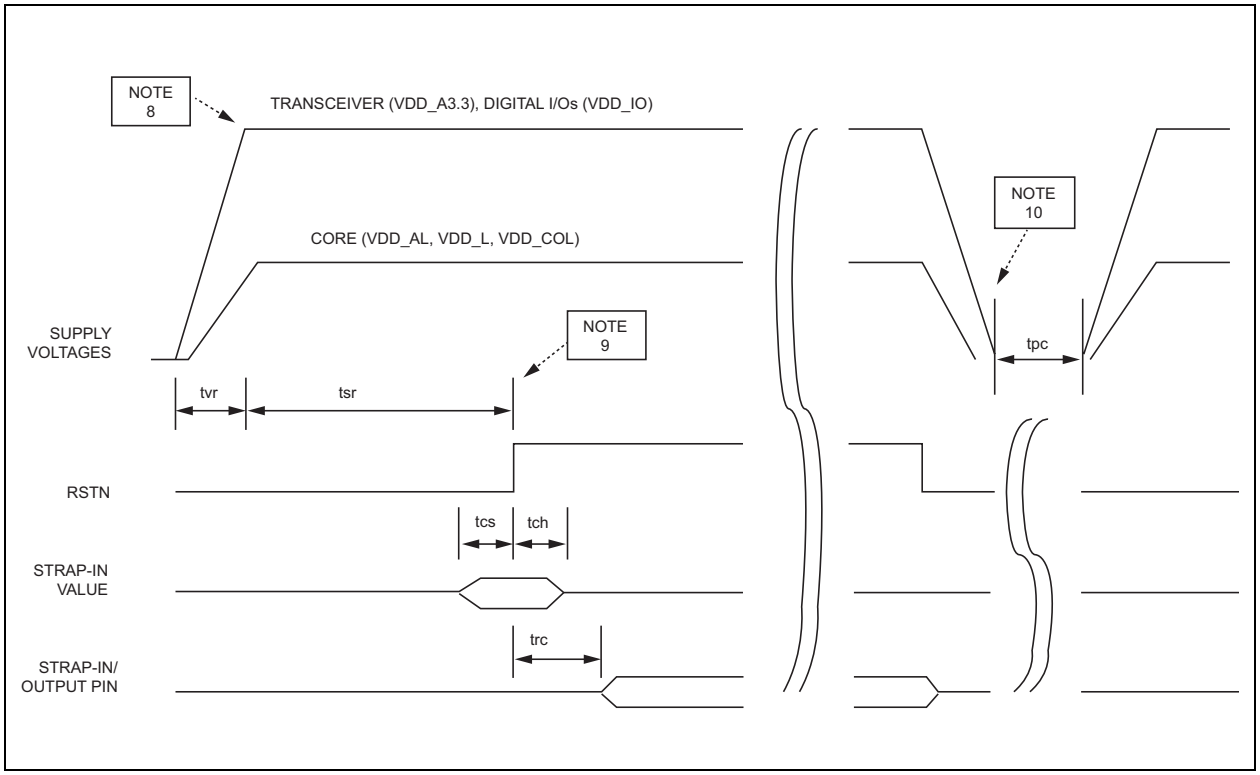


TABLE 7-4: RESET TIMING PARAMETERS

Parameter	Description	Min.	Max.	Units
tvr	Supply voltages rise time (must be monotonic)	0	—	—
tsr	Stable supply voltages to de-assertion of reset	10	—	—
tcs	Strap-in pin configuration setup time	5	—	—
tch	Strap-in pin configuration hold time	5	—	—
trc	De-assertion of reset to strap-in pin output	6	—	—

Note 1: The recommended powering sequence is to bring up all voltages at the same time. However, if that cannot be attained, then a recommended power-up sequence is to have the transceiver ($V_{DD\_A3.3}$) and digital I/Os (V_{DD_IO}) voltages power up before the low-voltage core (V_{DD_AL}, V_{DD_L}, and V_{DD_COL}) voltage, if an external low voltage core supply is used. There is no power sequence requirement between transceiver ($V_{DD\_A3.3}$) and digital I/Os (V_{DD_IO}) power rails. The power-up waveforms should be monotonic for all supply voltages to the KSZ8852.

2: After the de-assertion of reset, it is recommended to wait a minimum of 100 µs before starting programming of the device through any interface.

3: The recommended power-down sequence is to have the low-voltage core voltage power-down first before powering down the transceiver and digital I/O voltages.

7.5 Reset Circuit Guidelines

Figure 7-5 is the recommended reset circuit for powering up the KSZ8852 device if reset is triggered by the power supply.

FIGURE 7-5: SAMPLE RESET CIRCUIT

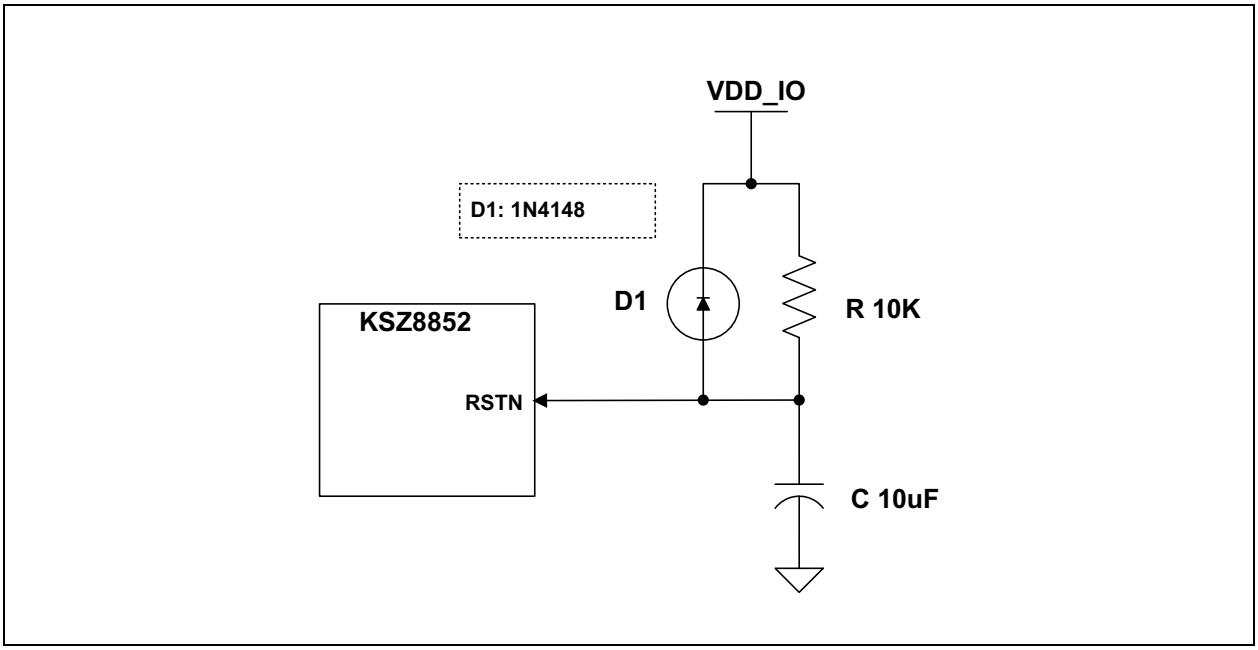
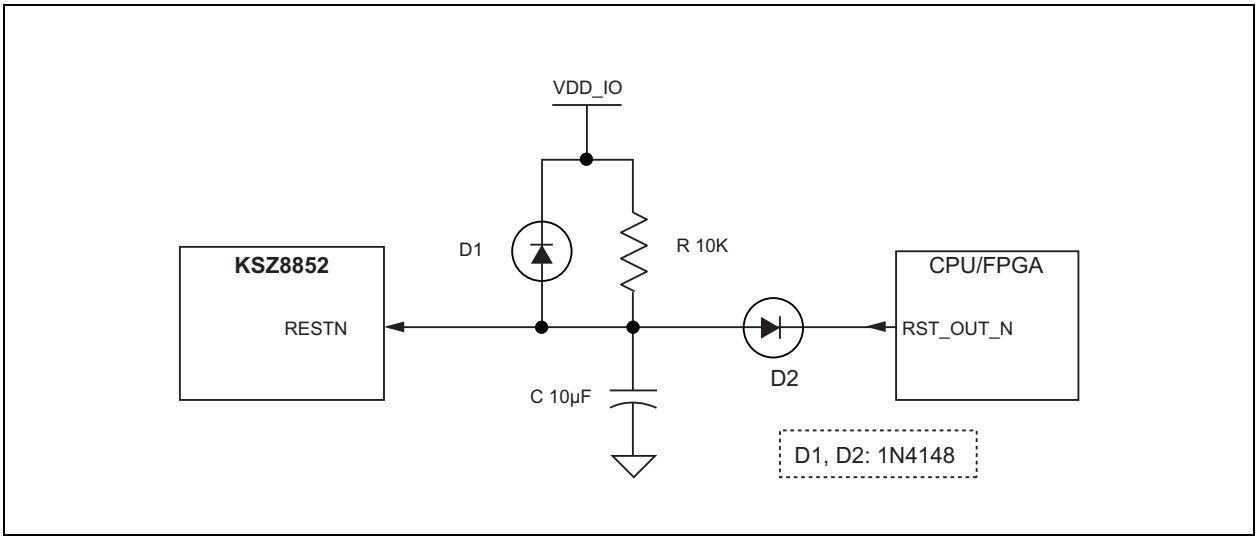


Figure 7-6 is the recommended reset circuit for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ8852 device. The RST_OUT_N from CPU/FPGA provides the warm reset after power up.

FIGURE 7-6: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH A CPU/FPGA RESET OUTPUT

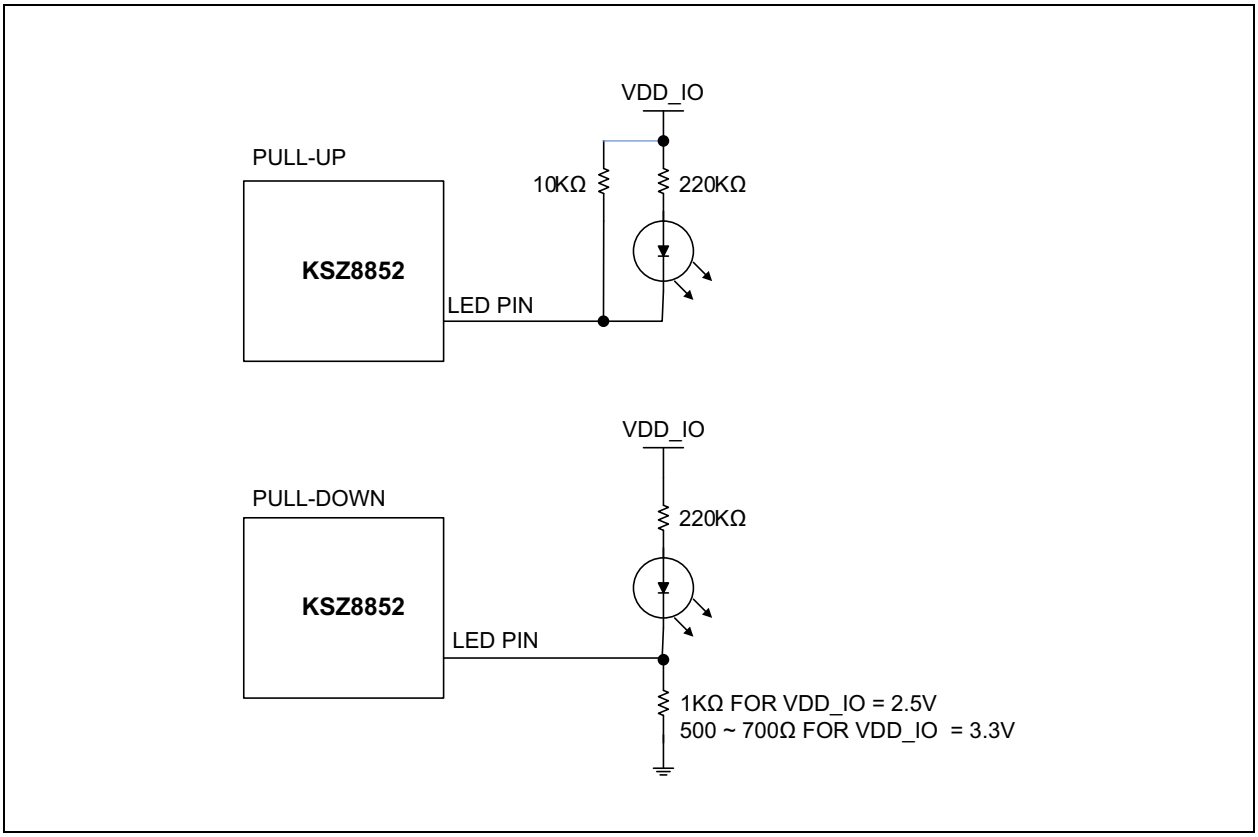


7.6 Reference Circuits – LED Strap-In Pins

The pull-up and pull-down reference circuits for the P1LED0/H816 and P2LED0/LEBE strapping pins are shown in Figure 7-7.

The supply voltage for the LEDs must be at least ~2.2V, depending on the particular LED and the load resistor used. If V_{DD_IO} is 1.8V, then a different (higher voltage) supply must be used for the LEDs.

FIGURE 7-7: TYPICAL LED STRAP- IN CIRCUIT

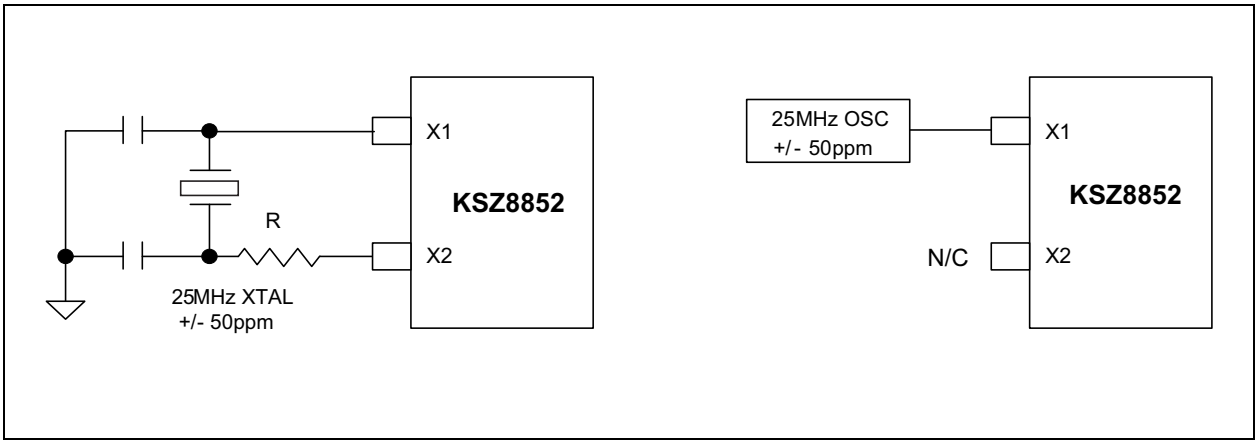


7.7 Reference Clock – Connection and Selection

Figure 7-8 shows a crystal or external clock source, such as an oscillator, as the reference clock for the KSZ8852. The reference clock is 25 MHz for all operating modes of the KSZ8852. If an oscillator is used, connect it to X1, and leave X2 unconnected.

The resistor shown on X2 is optional and can be used to reduce the current to the crystal if needed, depending on the specific crystal that is used. The maximum recommended resistor value is 30Ω.

FIGURE 7-8: 25 MHZ CRYSTAL AND OSCILLATOR CLOCK CONNECTIONS



Selection of Reference Crystal

TABLE 7-5: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristics	Value
Frequency	25 MHz
Frequency tolerance (max)	±50 ppm
Series resistance (max)	50Ω

8.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 8-1 lists recommended transformer characteristics.

TABLE 8-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT:1 CT	—
Open-Circuit Inductance (max.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	100 kHz to 100 MHz
HIPOT (max.)	1500 V_{RMS}	—

TABLE 8-2: QUALIFIED SINGLE-PORT MAGNETIC

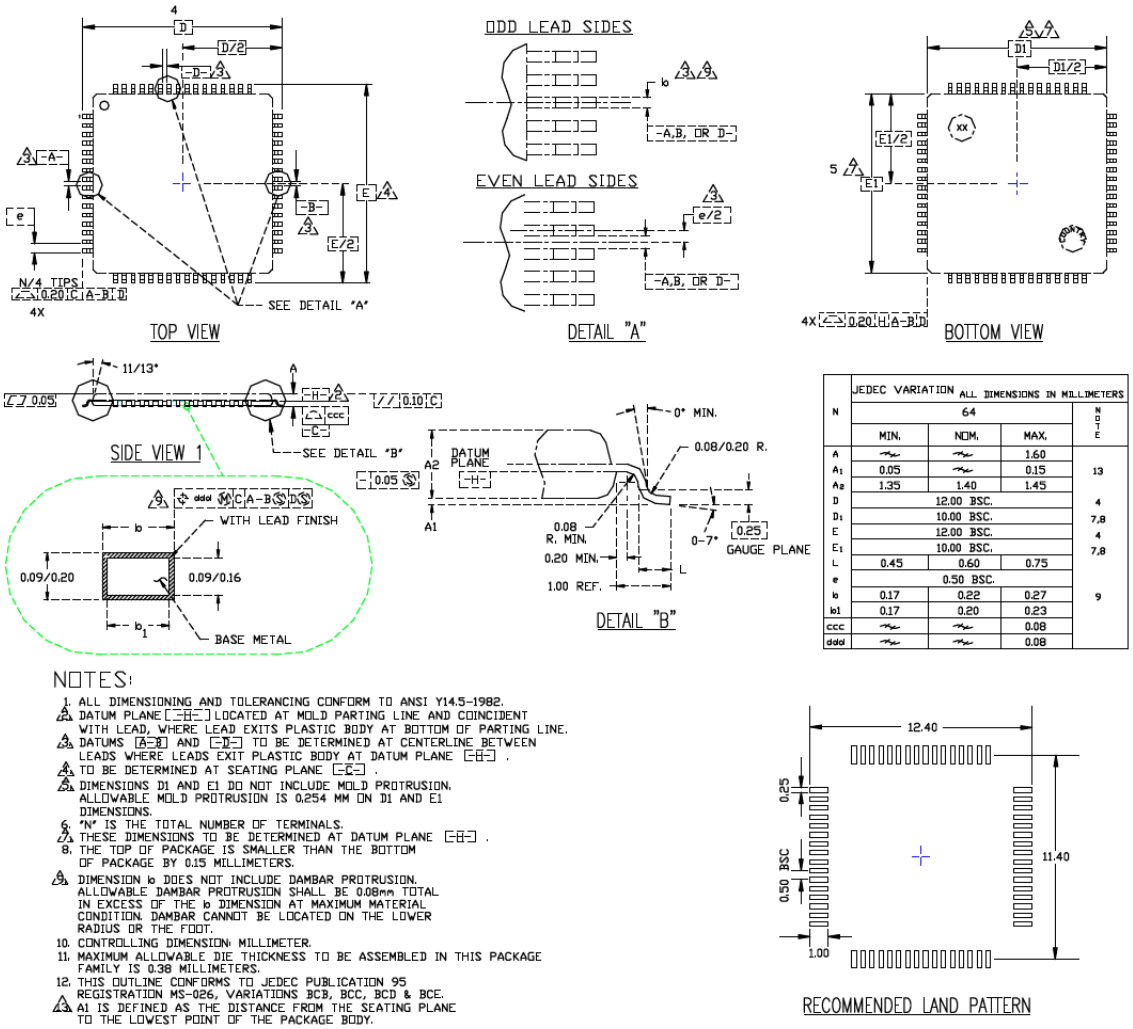
Manufacturer	Part Number	Auto MDI-X
Pulse	H1102NL	Yes
Pulse (low cost)	H1260	Yes
Transpower	HB726	Yes
Bel Fuse	S558-5999-U7	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
TDK (Mag Jack)	TLA-6T718	Yes

9.0 PACKAGE OUTLINE

FIGURE 9-1: 64-LEAD LQFP 10 MM X 10 MM PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

TITLE
64 LEAD LQFP 10x10mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	LQFP10x10-64LD-PL-1	UNIT	MM



N	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
	64			NOTE
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05		0.15	13
A_2	1.35	1.40	1.45	
D		12.00 BSC.		4
D_1		10.00 BSC.		7,8
E		12.00 BSC.		4
E_1		10.00 BSC.		7,8
L	0.45	0.60	0.75	
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b_1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS -A-B- AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS BCB, BCC, BCD & BCE.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002761A (09-13-18)	—	Converted Micrel data sheet KSZ8852HLE to Microchip DS00002761A. Minor text changes throughout.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	X	X	X	X	-XX
Device	Interface	Package	Generic Interface	Temperature	Bond Wire	Media Type

Device:	KSZ8852
Interface:	H = Generic Host Bus Interface
Package:	L = 64-Lead LQFP
Generic Interface:	E = 16-Bit Generic Interface
Temperature:	W = –40°C to +105°C (Ext.Industrial) Y = –40°C to +115°C (Ext.Industrial)
Bond Wire:	A = Gold Bond Wire
Media Type:	<blank> = 160/Tray TR = 1000/Reel

Examples:

a) KSZ8852-HLEWA:	Two-Port 10/100 Ethernet Switch with 8-/16-Bit Generic Host Bus Interface, 64 Lead LQFP, 16-Bit Generic Interface,–40°C to +105°C (Ext. Industrial Temp.), Gold Bond Wire,160/Tray
b) KSZ8852-HLEWA-TR:	Two-Port 10/100 Ethernet Switch with 8-/16-Bit Generic Host Bus Interface, 64 Lead LQFP, 16-Bit Generic Interface,–40°C to +105°C (Ext. Industrial Temp.), Gold Bond Wire,1000/Reel
c) KSZ8852-HLEYA:	Two-Port 10/100 Ethernet Switch with 8-/16-Bit Generic Host Bus Interface, 64 Lead LQFP, 16-Bit Generic Interface,–40°C to +115°C (Ext. Industrial Temp.), Gold Bond Wire, 160/Tray
d) KSZ8852-HLEYA-TR:	Two-Port 10/100 Ethernet Switch with 8-/16-Bit Generic Host Bus Interface, 64 Lead LQFP, 16-Bit Generic Interface,–40°C to +115°C (Ext. Industrial Temp.), Gold Bond Wire, 1000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

ISBN: 978-1-5224-3529-7

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820