STANDARD MICROSYSTEMS CORPORATION

CRT 7004
μPC FAMILY

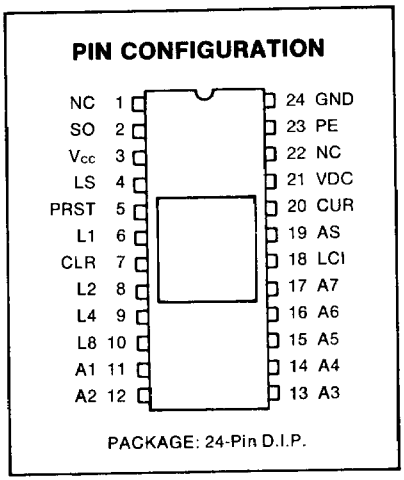
Dot Matrix Character Generator

128 Characters of 7 × 11 Bits

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 7004A 20MHz
    - CRT 7004B 15MHz
    - CRT 7004C 10MHz
    - Access time 400ns
- ☐ No descender circuitry required
- ☐ On chip cursor
- ☐ On chip character address buffer
- ☐ On chip line address buffer
- ☐ Single +5 volt power supply
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM
- ☐ Compatible with CRT 5027 VTAC®
- ☐ Enhanced version of CG5004L-1

PIN CONFIGURATION



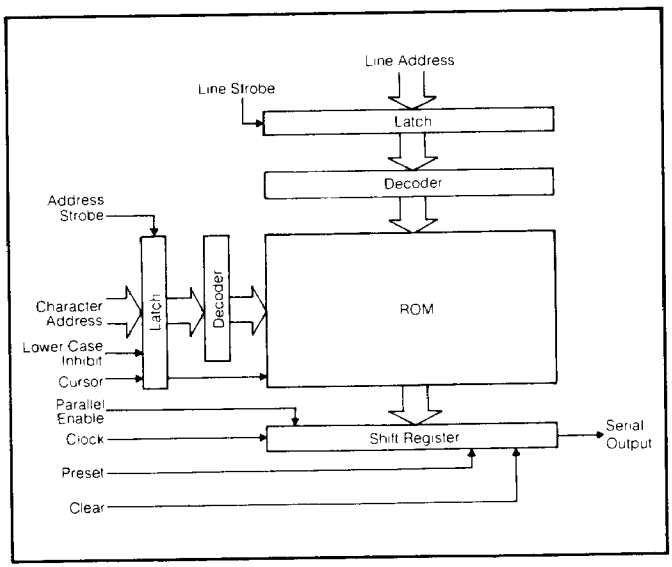
PACKAGE: 24-Pin D.I.P.

GENERAL DESCRIPTION

SMC's CRT 7004 is a high speed character generator with a high speed video shift register designed to display 128 characters in a 7 x 11 dot matrix. The CRT 7004 is an enhanced, pin for pin compatible, version of SMC's CG5004L-1. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply. This process permits reduction of turn-around time for ROM patterns.

The CRT 7004 is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

FUNCTIONAL BLOCK DIAGRAM



SECTION V

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

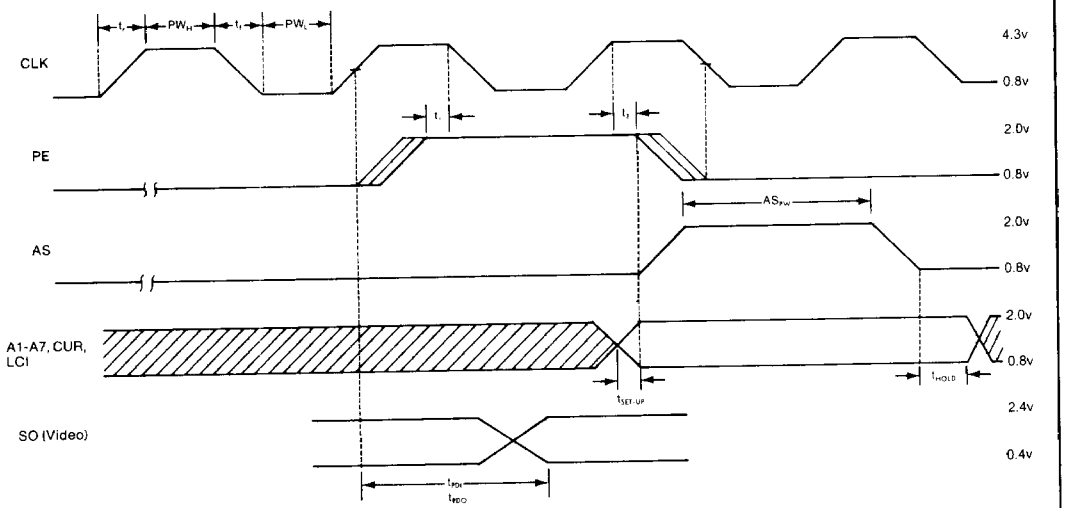
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See AC Timing Diagram
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L			100	μA	V_{IN} = O, LS, AS, A1-A7, Cursor LCI
			10	μA	$O \leq V_{IN} \leq V_{CC}$, All others
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
PE		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

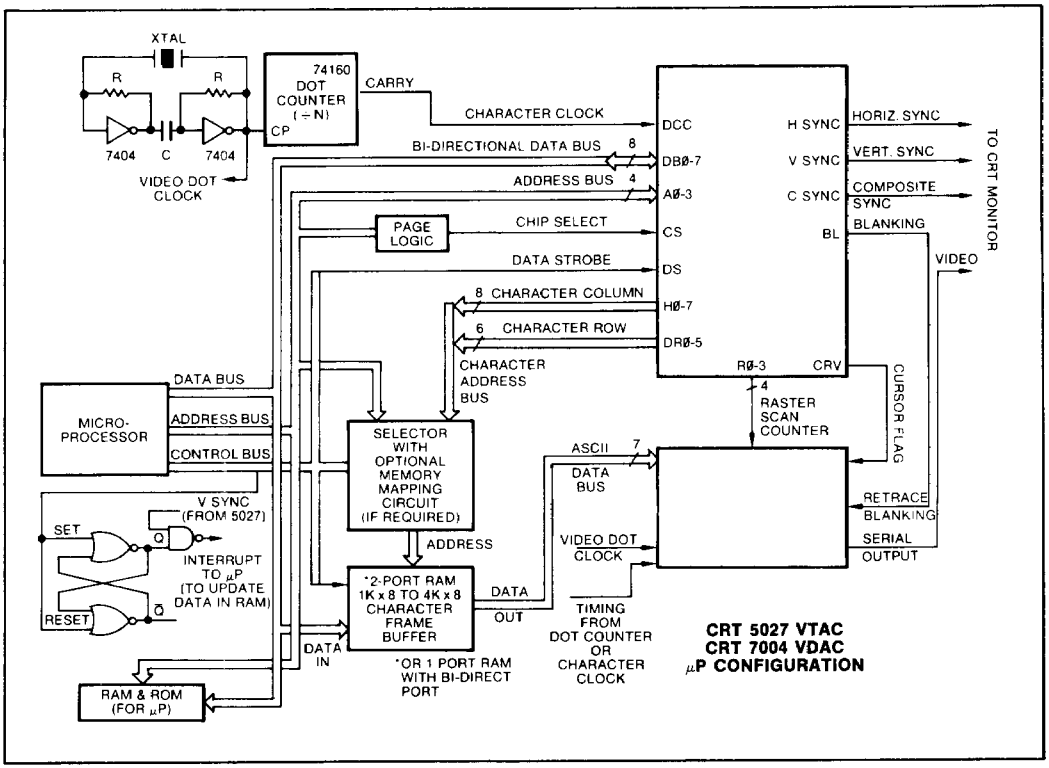
SYMBOL	PARAMETER	CRT 7004A		CRT 7004B		CRT 7004C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC — High Time	13.5		21		36		ns
PW_L	VDC — Low Time	13.5		21		36		ns
$t_{CY}AS$	Address strobe to PE high	400		533		800		ns
$t_{CY}LS$	Line strobe to PE high	1.0		1.0		1.0		μs
t_r, t_f	Rise, fall time		10		10		10	ns
t_1	PE set-up time	5		20		20		ns
t_2	PE hold time	15		15		15		ns
AS_{PW}	Address strobe pulse width	50		50		50		ns
LS_{PW}	Line strobe pulse width	50		50		50		ns
t_{SET-UP}	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{Pd1}, t_{Pd0}	Output propagation delay		45		60		90	ns

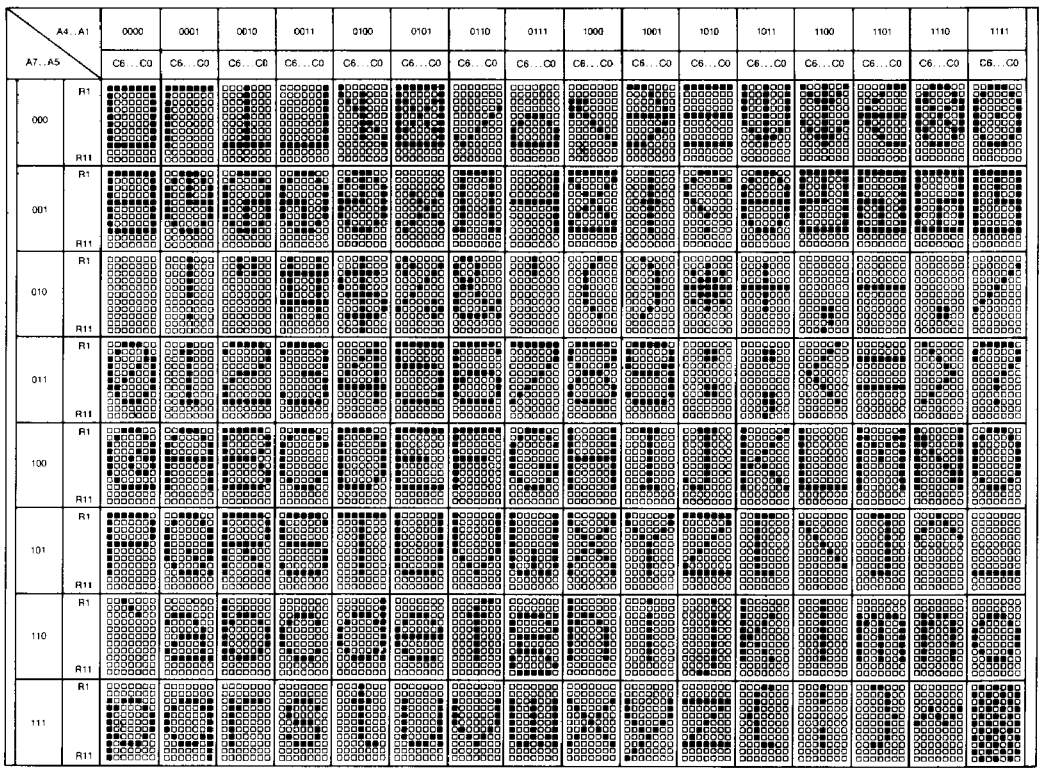
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	NC	No Connection	
2	SO	Serial Output	The output of the dynamic shift register is clocked out on this pin. The serial input to this shift register is internally grounded; thus zeros are shifted in while data is shifted out.
3	V_{CC}	Power Supply	+5 volt supply
4	LS	Line Strobe	A positive pulse on this input enters data from the L1, L2, L4, L8 lines into the line address holding register. The LS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. Data on the L1 to L8 inputs is then entered directly into the register without any latching action.
5	PRST	Preset	A high level on this input forces the last stage of the shift register and the serial output to a logic high.
6,8,9,10	L1, L2, L4, L8	Line Address	A binary number N, on these four inputs address the Nth line of the character font for N = 1—11. If lines 0, 12, 13, 14 or 15 are addressed, the parallel inputs to the shift register are all forced low.
7	CLR	Clear	A high level on this input forces the last stage of the shift register and the serial output to a logic low and will be latched (for a character time) by PE. Clear overrides preset.
11-17	A1-A7	Character Address	The seven-bit word on these inputs is decoded internally to address one of the 128 available characters.
18	LCI	Lower Case Inhibit	A high level on this input transforms the address of a lower case character into that of the equivalent upper case character. This is internally achieved by forcing A6 low whenever A7 and LCI are high.
19	AS	Address Strobe	A positive pulse on this input enters data from the A1-A7, LCI and CUR inputs into the holding register. The AS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. The data on the A1-A7, LCI and CUR inputs is then entered directly into the register without any latching action.
20	CUR	Cursor*	A high level on this input causes the cursor pattern to be superimposed on the pattern of the character addressed, i.e., the two patterns are OR-ed to generate the parallel inputs to the shift register. The standard cursor is presented as a double underscore on rows 10 and 11.
21	CLK	Clock	Frequency at which video (SO) is shifted.
22	NC	No Connection	
23	PE	Parallel Enable	A high level on this input loads the word at the output of the ROM into the shift register. The PE input must then be brought low again to allow the shift register to clock out this word.
24	GND	Ground	Ground

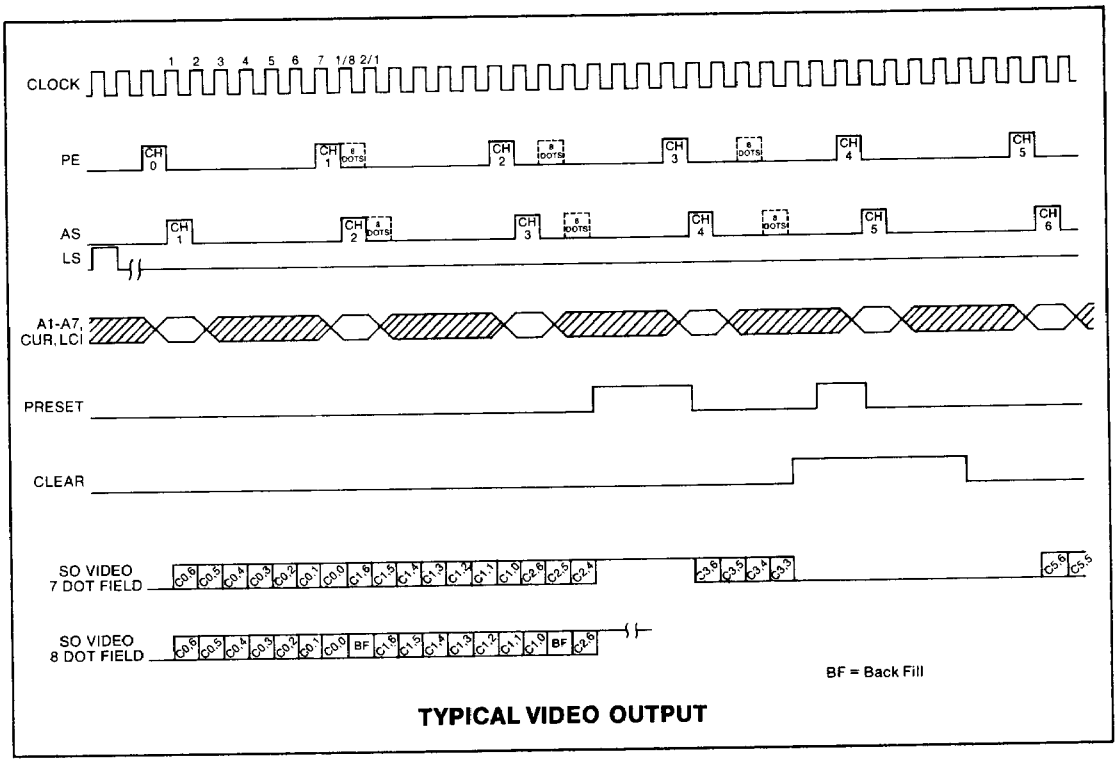


AC TIMING DIAGRAM

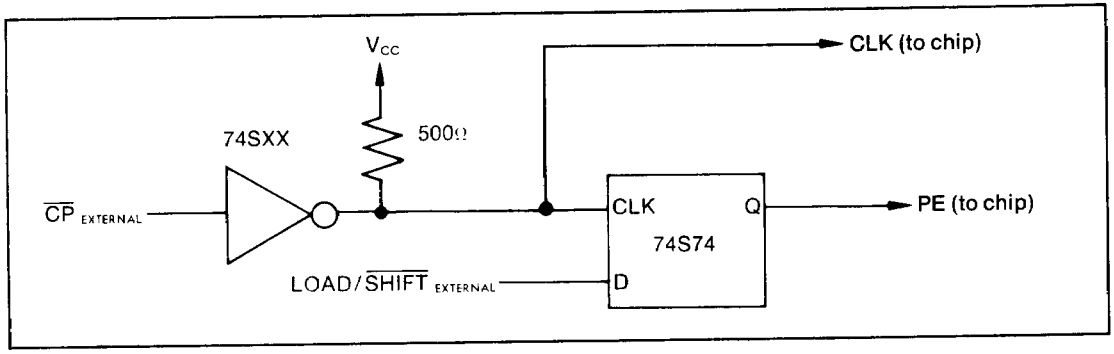




*CONSULT FACTORY FOR CUSTOM FONT AND CURSOR OPTION.



TYPICAL VIDEO OUTPUT



NOTE

The differences between the CRT 7004 and CG5004L-1 are detailed below:

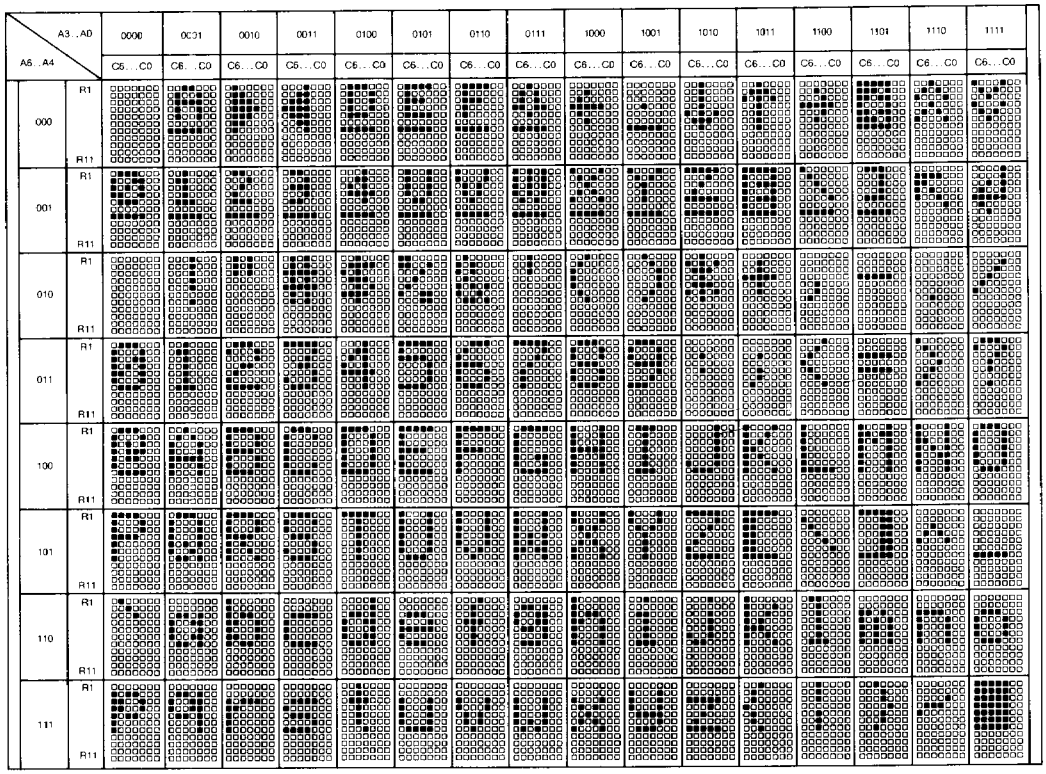
CG5004L-1

1. If both the Preset and Clear inputs are brought high simultaneously the Serial Output is disabled and may be wire-ORed.
2. All Inputs $V_{IH} = V_{CC} - 1.5v$
3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.2mA$
4. Shift Register is static
5. Clear—directly forces the output low; when released, the output is determined by the state of the shift register output.
6. General Timing Differences—See Timing Diagram

CRT 7004

1. Clear overrides Preset, no output disable is possible.
2. All inputs (except CLK) $V_{IH} = 2.0v$, min. CLK $V_{IH} = 4.3v$, min.
3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.4mA$ 74LSXX load
4. Shift Register is dynamic
5. Clear directly forces the output low and will be latched (for a character time) by PE.
6. General Timing Differences—See Timing Diagram

Dot Matrix Character Generator



The Cursor for the CRT 7004-003 is presented as a double underscore on Rows 8 and 9.