STANDARD MICROSYSTEMS CORPORATION

FDC72C65/66

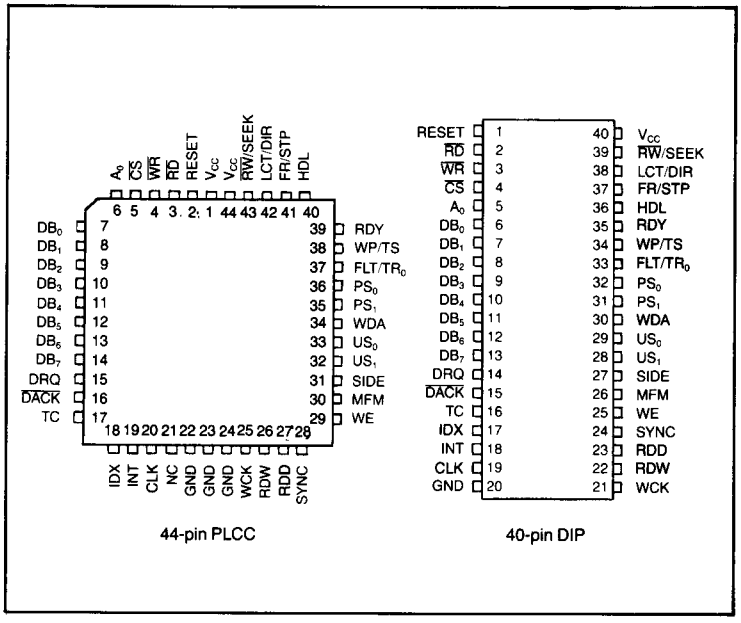
PRELIMINARY

Single/Double Density Floppy Disk Controller

FEATURES

- ☐ IBM-compatible format (single, double and quad density) (FDC72C65)
- ☐ Sony (EMCA)-compatible recording format (FDC72C66)
- ☐ Multi-sector and multi-track transfer capability
- ☐ Drive Up to 4 floppy or micro floppydisk drives
- ☐ Data scan capability–will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Programmable stepping rate, head load and head unload times
- ☐ Parallel seek operations on up to four drives
- ☐ Compatible with μPD8080/85, μPD8086/88, μPD80186/286/386 and Z80' microprocessors
- ☐ Single-phase clock 8 MHz (standard floppy) or 4 MHz (minifloppy)
- ☐ CMOS technology
- ☐ Single +5V ±10% power supply.

PIN CONFIGURATION



44-pin PLCC

40-pin DIP

SECTION VI

GENERAL DESCRIPTION

The FDC72C65 is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The FDC 72C65 provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The FDC72C66 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppy-disk* drive. The FDC72C66 is pin-compatible and electrically equivalent to the 72C65 but utilizes the Sony recording format. The FDC72C66 can read a diskette that has been formatted by the FDC72C65.

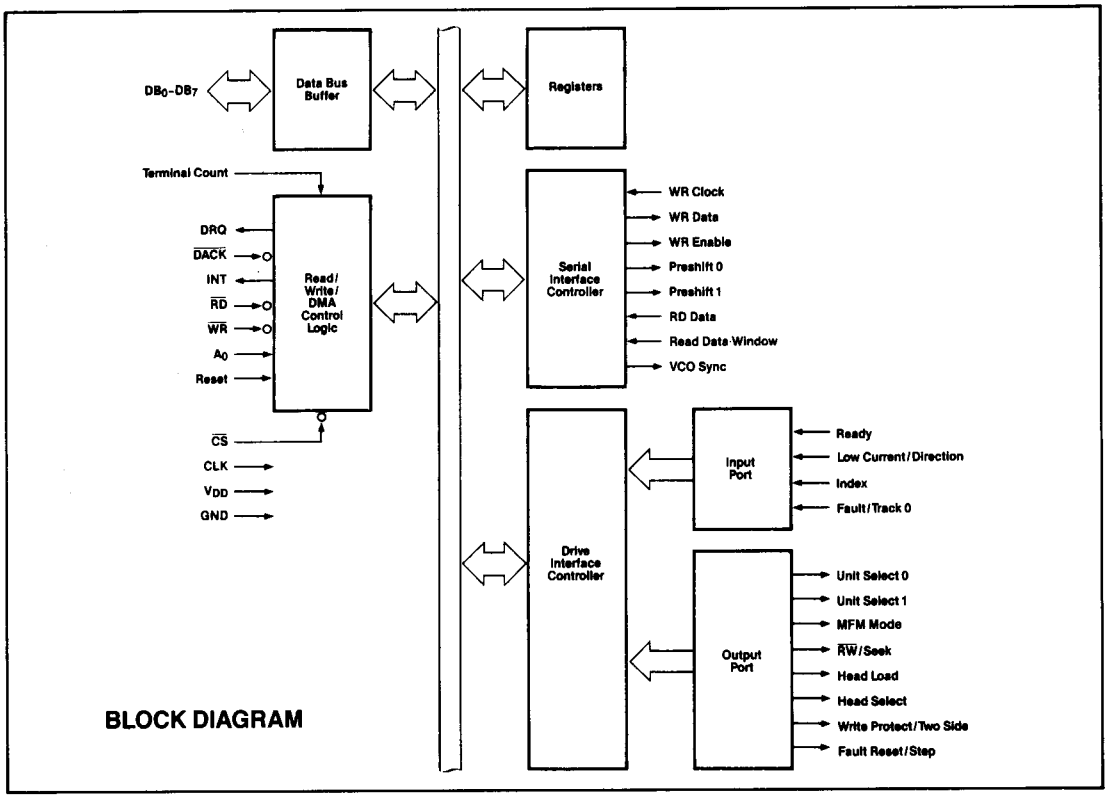
Hand-shaking signals are provided in the FDC72C65/FDC72C66 which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

The FDC is designed using CMOS technology. In addition to a low normal operating current, a standby mode can be software-enabled to provide minimal current drain when the FDC is not in use.

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The FDC72C65/FDC72C66 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

There are 18 commands which the FDC72C65/FDC72C66 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Format Track
Read Track	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
Set Standby	Sense Drive Status
Reset Standby	Software Reset



BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
1	RESET	Reset	Input	Processor	A high input places the FDC72C65/72C66 in standby mode and sets drive interface outputs to low level (except PS_0, PS_1, and WDATA). In the main system, INT and DRQ are set to low level, and DB_0-DB_7 are set as inputs.
2	$\overline{RD}$	Read control	Input	Processor	The $\overline{RD}$ input allows the transfer of data from the FDC to the data bus when low. Disabled when $\overline{CS}$ is high.
3	$\overline{WR}$	Write control	Input	Processor	The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.
4	$\overline{CS}$	Chip select	Input	Processor	The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$, $\overline{WR}$, and A_0.
5	A_0	Data or status select	Input	Processor	The A_0 input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be sent to the data bus.
6-13	DB_0-DB_7	Bidirectional data bus	Input Output	Processor	DB_0-DB_7 are a bidirectional three-state 8-bit data bus. Disabled when $\overline{CS}$ is high.
14	DRQ	DMA request	Output	DMA	The FDC asserts the DRQ output high to request a DMA transfer.
15	$\overline{DACK}$	DMA acknowledge	Input	DMA	When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.
16	TC	Terminal count	Input	DMA	When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

DESCRIPTION OF PIN FUNCTIONS

PIN			INPUT/ OUTPUT	CONNECTION TO	FUNCTION
NO.	SYMBOL	NAME			
17	IDX	Index	Input	FDD	The IDX input goes high at the beginning of a disk track.
18	INT	Interrupt request	Output	Processor	The INT output is FDC's interrupt request.
19	CLK	Clock	Input	Clock	CLK is the input for the FDC's single-phase, 8 MHz (standard floppy) or 4 MHz (mini floppy) clock.
20	GND	Ground			Ground.
21	WCK	Write clock	Input	Data Separator or Clock Generator	The WCK input sets the data read and write rate. Synchronize the rising edge of WCK with the rising edge of CLK. FM = 16 CLK cycles; MFM = 8 CLK cycles.
22	RDW	Read data window	Input	Phase Lock Loop	The RDW input is generated by the VFO circuit. It is used to sample clock and data bits of RDD.
23	RDD	Read data	Input	FDD	The RDD input is the read data from the FDD, containing clock and data bits. Input RDD and RDW during a data read, or the FDC will enter a deadlock state.
24	SYNC	VCO sync	Output	Phase Lock Loop	SYNC outputs the functional mode of the FDC. A high output indicates read and a low output inhibits read.
25	WE	Write enable	Output	FDD	The WE output enables write data into the FDD.
26	MFM	MFM	Output	Phase Lock Loop	The MFM output shows the FDC's mode. It is high for MFM, low for FM.
27	SIDE	Side select	Output	FDD	Head 1 is selected when the SIDE output is 1 (high), head 0 is selected when SIDE is 0 (low).
28, 29	US_0, US_1	FDD unit select	Output	FDD	The US_0 and US_1 outputs select the floppy disk drive unit.
30	WDA	Write data	Output	FDD	WDA is the serial clock and data output to the FDD.
31, 32	PS_0, PS_1	Preshift	Output	FDD	The PS_0 and PS_1 outputs are the write precompensation status for MFM mode. They determine early, late, and normal times.
33	FLT/TR_0	Fault/track zero	Input	FDD	In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TR_0 detects track 0.
34	WP/TS	Write protect/two side	Input	FDD	In the read/write mode, the WP input senses write protected status. In the seek mode, TS senses two-sided media.
35	RDY	Ready	Input	FDD	The RDY input indicates that the FDD is ready to receive.
36	HDL	Head load	Output	FDD	The HDL output is the command which causes the read/write head in the FDD to contact the diskette.
37	FR/STP	Fault reset/step	Output	FDD	In the read/write mode, the FR output resets the fault flip-flop in the FDD. In the seek mode, STP outputs step pulses to move the head to another cylinder. A fault reset pulse (FR) is issued at the beginning or each Read or Write command prior to the HDL signal.
38	LCT/DIR	Low current/direction	Output	FDD	When RW/SEEK specifies RW, this output becomes LCT, indicating the read/write head of the drive is selecting a cylinder beyond the 43rd cylinder. When RW/SEEK specifies SEEK, this pin becomes DIR, specifying the direction of the seek operation. A low signal indicates output and a high signal indicates input.
39	$\overline{RW}$/ SEEK	Read/write/seek	Output	FDD	The $\overline{RW}$/SEEK output specifies the read/write mode when low, and the seek mode when high.
40	V_{CC}	DC power		Power Supply	+5V power supply.

Internal Registers

The FDC72C65/FDC72C66 contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0-ST3, in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and FDC72C65/FDC72C66.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in table 1.

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the main status register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC busy) goes low is 12 μs. See figure 1.

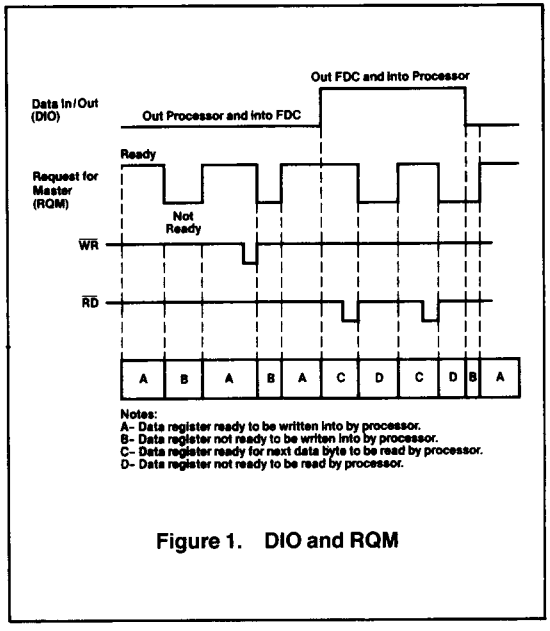


Figure 1. DIO and RQM

Table 1. Status/Data Register Addressing

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read main status register
0	1	0	Reset commands
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from data register
1	1	0	Write into data register

The bits in the main status register are defined in table 2.

Table 2. Main Status Register

Pin No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_4	CB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB_6	DIO (Data Input/ Output)	Indicates direction of data transfer between the processor and data register. If DIO = 1, then transfer is from data register to the processor. If DIO = 0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

Table 3. Status Register Identification

Pin No.	Pin Name	Symbol	Function
			Status Register 0
D_7, D_6	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal termination of command, (NT). Command was completed and properly executed.
			$D_7 = 0$ and $D_6 = 1$ Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at interrupt.
D_1	Unit Select 1	US_1	This flag is used to indicate a drive unit number at interrupt.
D_0	Unit Select 0	US_0	This flag is used to indicate a drive unit number at interrupt.
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit is always 0 (low).
D_2	No Data	ND	During execution of Read Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
			During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the Read A Cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the data address mark or deleted data address mark, this flag is set. Also at the same time, the MD (missing address mark in data field) of status register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Status Register 3			
D_7	Fault	FT	This bit is used to indicate the status of the fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	Two-Side	TS	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the side select signal to the FDD.
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Note:

(1) CRC = Cyclic Redundancy Check

(2) IDR = Internal Data Register

(3) Cylinder (C) is described more fully in the Command Symbol Description.

Standby Mode

The FDC72C65/FDC72C66 can be placed in a low-power standby mode by issuing the SET STANDBY command. During standby mode, the main status register will contain all zeros. After standby mode is disabled, RQM (Request for Master) in the main status register will be set to 1, indicating that the FDC72C65/72C66 is available for use. During standby mode, it is only necessary to maintain clock on pin 19. All disk control signals will be inactive.

To further reduce system power dissipation, it is possible to stop the clock on pin 19 as well by the following procedure.

(1) Issue SET STANDBY command.

(2) Wait for 32 clock periods, minimum.

(3) The clock may then be stopped.

To resume normal operation, the clock must be re-started. After 24 clock periods, the RESET STANDBY command may be issued.

All internal registers and I/O ports are held constant. V_{DD} must be maintained at normal levels.

Command Sequence

The FDC72C65/FDC72C66 is capable of performing 18 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the FDC72C65/FDC72C66 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbreviations used in table are given in the Command Symbol Description table.

NOTES:

Command Symbol Description

Pin		Function
Name	**Symbol**	
Address Line 0	A_0	A_0 controls selection of main status register (A_0 = 0) or data register (A_0 = 1).
Cylinder Number	C	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
Data	D	D stands for the data pattern which is going to be written into a sector.
Data Bus	D_7-D_0	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
Data Length	DTL	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
End of Track	EOT	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
Gap Length	GPL	GPL stands for the length of gap 3. During Read/Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
Head Address	H	H stands for head number 0 or 1, as specified in ID field.
Head	HD	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
Head Load Time	HLT	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments.)
Head Unload Time	HUT	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments.)
FM or MFM Mode	MF	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
Multitrack	MT	If MT is high, a multitrack operation is performed. If MT = 1 after finishing read/write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
Number	N	N stands for the number of data bytes written in a sector.
New Cylinder Number	NCN	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
Non-DMA Mode	ND	ND stands for operation in the non-DMA mode.
Present Cylinder Number	PCN	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
Record	R	R stands for the sector number which will be read or written.
Read/Write	R/W	R/W stands for either Read (R) or Write (W) signal.
Sector	SC	SC indicates the number of sectors per cylinder.
Skip	SK	SK stands for skip deleted data address mark.
Step Rate Time	SRT	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
Status 0-3	ST0-ST3	ST0-ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contains information relevant to that particular command.
	STP	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
Unit Select	US_0, US_1	US stands for a selected drive number 0 or 1.

NOTES:

Table 4. Instruction Set

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the main system and FDD
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	← ST0 →								Status information about the FDC at the end of seek operation
	R	← PCN →								
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	← SRT →					← HUT →			
	W	← HLT →							ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	← ST3 →								Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	← NCN →								
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	← Invalid Codes →								Invalid Command codes (No op—FDC goes into standby state)
Result	R	← ST0 →								ST0 = 80H
Set Standby										
Command	W	0	0	1	1	0	1	0	1	Command codes
Execution										Enter standby mode
Reset Standby										
Command	W	0	0	1	1	0	1	0	0	Command codes
Execution										Disable standby mode
Software Reset										
Command	W	0	0	1	1	0	1	1	0	Command codes
Execution										Same as hardware reset
Read a Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	← ST0 →								Status information after command execution
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution
	R	← H →								
	R	← R →								
	R	← N →								

NOTES:

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information read during execution phase from floppy disk.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Format a Track										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			N				→	Bytes/sector
	W	←			SC				→	Sectors/track
	W	←			GPL				→	Gap 3
	W	←			D				→	Filler byte
Execution										FDC formats an entire track.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	In this case, the ID information has no meaning
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Note:

(1) In the Instruction Code, X = don't care (usually set to 0).

(2) A_0 should be 0 for SET STANDBY, RESET STANDBY, and SOFTWARE RESET commands and 1 for all other commands.

NOTES:

System Configuration

Figure 2 shows an example of a system using a FDC72C65/FDC72C66.

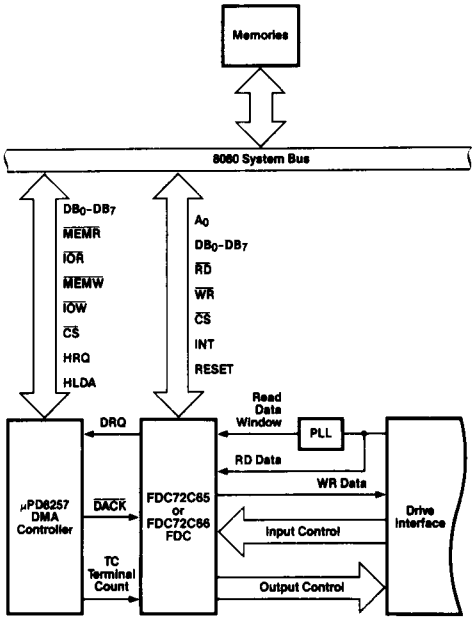


Figure 2. System Configuration

Processor Interface

During command or result phases the main status register (described earlier) must be read by the processor before each byte of information is written into or read from the data register. After each byte of data is read or written to the data register, the CPU should wait for 12μs before reading the main status register. Bits D_6 and D_7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the FDC72C65/FDC72C66. Many of the commands require multiple bytes and, as a result, the main status register must be read prior to each byte transfer to the FDC72C65/FDC72C66. On the other hand, during the result phase, D_6 and D_7 in the main status register must both be 1's ($D_6 = 1$ and $D_7 = 1$) before reading each byte from the data register. Note that this reading of the main status register before each byte transfer to the FDC72C65/FDC72C66 is required only in the command and result phases, and *not* during the execution phase.

During the execution phase, the main status register need not be read. If the FDC72C65/FDC72C66 is in the non-DMA mode, then the receipt of each data byte (if FDC72C65/FDC72C66 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a read signal ($\overline{RD} = 0$) or write signal ($\overline{WR} = 0$) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the main status register and bit D_7 (RQM) functions as the interrupt signal. If a write command is in the process then the $\overline{WR}$ signal negates the reset to the interrupt signal.

Note that in the non-DMA mode it is necessary to examine the main status register to determine the cause of the interrupt, since it could be a data interrupt of a command termination interrupt, either normal or abnormal.

If the FDC72C65/FDC72C66 is in the DMA mode, no interrupts are generated during the execution phase. The FDC72C65/FDC72C66 generates DRQs (DMA requests) when each byte of data is available. The DMA controller responds to this request with both a $\overline{DACK} = 0$ (DMA acknowledge) and an $\overline{RD} = 0$ (read signal). When the DMA acknowledge signal goes low ($\overline{DACK} = 0$), then the DMA request is cleared ($DRQ = 0$). If a write command has been issued, then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the execution phase has been completed (terminal count has occurred) or the EOT sector read/written, then an interrupt will occur (INT = 1). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

It is important to note that during the result phase all bytes shown in the instruction set (table 4) must be read. The read data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The FDC72C65/FDC72C66 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

The FDC72C65/FDC72C66 contains five status registers. The main status register mentioned above may be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the FDC72C65/FDC72C66 to form the command phase and are read out of the FDC72C65/FDC72C66 in the result phase must occur in the order shown in table 4. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the FDC72C65/FDC72C66, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the FDC72C65/FDC72C66 is ready for a new command.

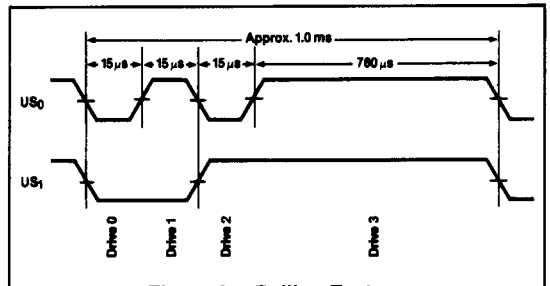


Figure 3. Polling Feature

Polling

After reset has been sent to the FDC72C65/FDC72C66, the unit select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the FDC72C65/FDC72C66 polls all four FDDs looking for a change in the ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the FDC72C65/FDC72C66 will generate an interrupt. When status register 0(ST0) is read (after Sense Interrupt Status is issued), not ready (NR) will be indicated. The polling of the ready line by the FDC72C65/FDC72C66 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms. See figure 3.

Read Data

A set of nine (9) byte words are required to place the FDC into the read data mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID address marks and ID fields. When the current sector number (R) stored in the ID register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the sector number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a multi-sector read operation. The Read Data command may be terminated by the receipt of a terminal count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (cyclic redundancy count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 5 shows the transfer capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTI defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus. The FDC reads (internally) the complete sector performing the CRC check and, depending upon the manner of command termination, may perform a multi-sector read operation. When N is non-zero, then DTL has no meaning and should be set to FFH.

At the completion of the Read Data command, the head is not unloaded until after head unload time interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head setting time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the index hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No data) flag in status register 1 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

After reading the ID and data fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (data error) flag in status register 1 to a 1 (high), and if a CRC error occurs in the data field, the FDC also sets the DD (data error in data field) flag in status register 2 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

If the FDC reads a deleted data address mark off the diskette, and the SK bit (bit D_5 in the first command word) is not set (SK = 0), then the FDC sets the CM (control mark) flag in status register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the deleted data address mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27μs in the FM mode, and every 13μs in the MFM mode, or the FDC sets the OR (Overrun) flag in status register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Table 6 shows the values for C, H, R, and N, when the processor terminates the command.

Functional Description of Commands

Write Data

A set of nine (9) bytes is required to set the FDC into the write data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head setting time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C,H,R,N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD. See table 6.

After writing data into the current sector, the sector number stored in R is incremented by one, and the next data field is written into. The FDC continues this multisector write operation until the issuance of a terminal count signal. If a terminal count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the terminal count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at side 0
0	1	01	(256) (26) = 6,656	or 26 at side 1
1	0	00	(128) (52) = 6,656	26 at side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at side 0
0	1	02	(512) (15) = 7,680	or 15 at side 1
1	0	01	(256) (30) = 7,680	15 at side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at side 0
0	1	03	(1024) (8) = 8,192	or 8 at side 1
1	0	02	(512) (16) = 8,192	8 at side 1
1	1	03	(1024) (16) = 16,384	

Table 6. Command Description

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=01	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=01	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=1	NC

Note: (1) NC (No Change): The same value as the one at the beginning of command execution.

(2) LSB (Least Significant Bit): The least significant bit of H is complemented.

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (end of cylinder) flag
- ND (no data) flag
- Head unload time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the write data mode, data transfers between the processor and FDC, via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the OR (overrun) flag in status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Write Deleted Data

This command is the same as the Write Data command except a deleted data address mark is written at the beginning of the data field instead of the normal data address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a data address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in status register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the data address mark and reads the next sector.

Read a Track

This command is similar to the Read Data command except that this is a continuous read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID address mark on the diskette after it senses the index hole for the second time, it sets the MA (missing address mark) flag in status register 1 to a 1 (high) and terminates the command. (Status register 0 has bits 7 and 6 set to 0 and 1, respectively).

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the

first ID field it is able to read. If no proper ID address mark is found in the diskette before the index hole is encountered for the second time, then the MA (missing address mark) flag in status register 1 is set to a 1 (high), and if no data is found then the ND (No data) flag is also set in status register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in status register 0 set to 0 and 1, respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format a Track command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; gaps, address marks, ID fields, and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format, are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number), and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C,H,R, and N to the FDC72C65/FDC72C66 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R reg-

Table 7. Sector Size

Format	Sector Size	N	SC	GPL (1)	GPL (2,3)
8" Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode (Note 4)	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode (Note 4)	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode (Note 4)	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Note:

(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.

(2) Suggested values of GPL in format command.

(3) All values except sector size are hexidecimal.

(4) In MFM mode FDC cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00).

ister are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a fault signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of status register 0 to 0 and 1, respectively. Also, the loss of a ready signal at the beginning of a command execution phase causes bits 7 and 6 of status register 0 to be set to 0 and 1, respectively.

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP→R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (scan hit) flag of status register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (scan not satisfied) flag of status register 2 to a 1 (high) and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 8 shows the status of bits SH and SN under various conditions of Scan.

Table 8. Scan Conditions

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a deleted data address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (control mark) flag of status register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the deleted address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (control mark) flag of status register 2 to a 1 (high) in order to show that a deleted sector has been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (overrun) flag set in status register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an overrun occurs, the FDC ends the command with bits 7 and 6 of status register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent present cylinder registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (present cylinder number) which is the current head position with the NCN (new cylinder number), and if there is a difference, performs the following operations:

PCN<NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step in)

PCN>NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step out)

The rate at which step pulses are issued is controlled by SRT (stepping rate time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (seek end) flag is set in status register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $D_0B - D_3B$ in the main status register are set during the seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the seek operation the FDC is in the FDC busy state, but during the execution phase it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the NR (not ready) flag is set in status register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

If the time to write three bytes of Seek command exceeds 150 μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the track 0 signal from the FDD. As long as the track 0 signal is low, the direction signal remains 0 (low) and step pulses are issued. When the track 0 signal goes high, the SE (seek end) flag in status register 0 is set to a 1 (high) and the command is terminated. If the track 0 signal is still low after 256 step pulses have been issued, the FDC sets the SE (seek end) and EC (equipment check) flags of status register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

The ability to do overlapping Recalibrate commands to multiple FDDs and the loss of the ready signal, as described in the Seek command, also applies to the Recalibrate command.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

(1) Upon entering the result phase of:
  (a) Read Data command
  (b) Read a Track command
  (c) Read ID command
  (d) Read Deleted Data command
  (e) Write Data command
  (f) Format a Cylinder command
  (g) Write Deleted Data command
  (h) Scan commands
(2) Ready line of FDD changes state
(3) End of Seek or Recalibrate command
(4) During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, DB_5 in the main status register is high. Upon entering the result phase this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by reading/writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and, via bits 5, 6, and 7 of status register 0, identifies the cause of the interrupt. See table 9.

Table 9. Interrupt Status

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready line changed state, either polarity
1	0	0	Normal termination of Seek or Recalibrate command
1	1	0	Abnormal termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the FDC72C65/FDC72C66 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be seek end or a change in ready status from one of the drives. A graphic example is shown in figure 4.

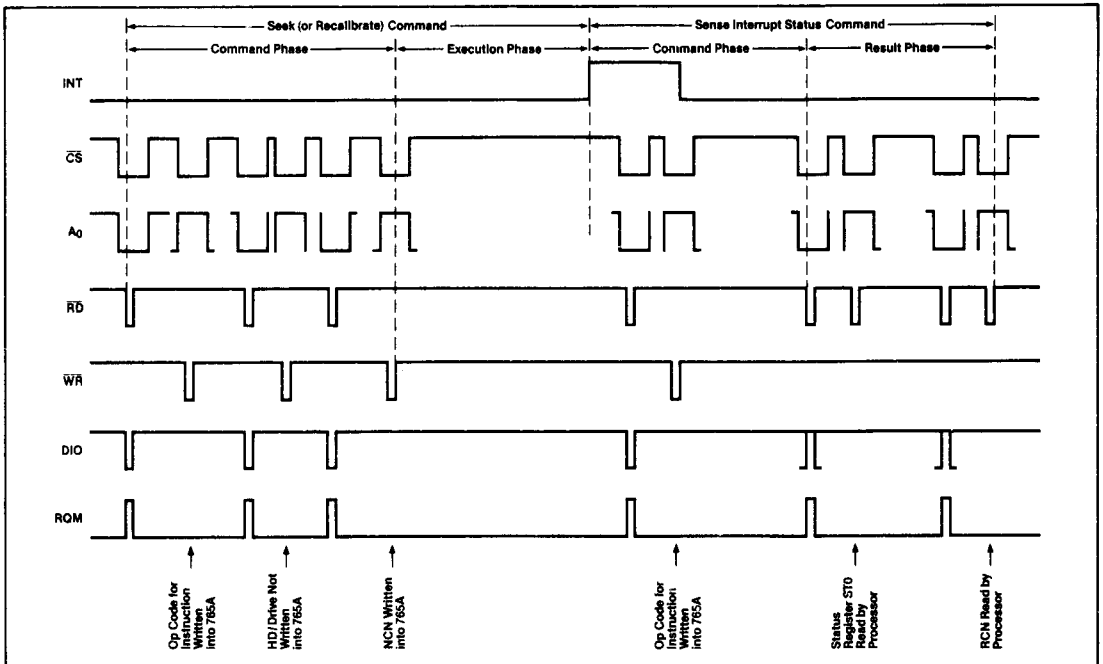


Figure 4. Seek, Recalibrate, and Sense Interrupt Status

Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (head unload time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OFH = 240 ms). The SRT (step rate time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (head load time) defines the time between when the head load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock was reduced to 4 MHz (minifloppy application), then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (non-DMA) bit. When this bit is high (ND = 1) the non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status register 3 contains the drive status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of status register 0 are set to 1 and 0, respectively. No interrupt is generated by the FDC72C65/FDC72C66 during this condition. Bits 6 and 7 (DIO and RQM) in the main status register are both 1 (high), indicating to the processor that the FDC72C65/FDC72C66 is in the result phase and the contents of status register 0 (ST0) must be read. When the processor reads status register 0 it will find an 80H, indicating an invalid command was received.

A Sense Interrupt Status command must be sent after a seek or recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid command. In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or no operation state.

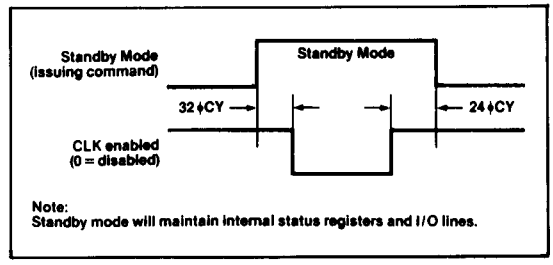
CMOS Reset Commands

Commands that are available in the FDC72C65/FDC72C66 which are enhancements over the FDC765A/FDC7265 are the CMOS reset commands. They are initiated as follows:

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Set standby	0	1	0	0	0	1	1	0	1	0	1
Reset standby	0	1	0	0	0	1	1	0	1	0	0
Software reset	0	1	0	0	0	1	1	0	1	1	0

The software reset command is identical to the hardware reset described previously.

The set standby command reduces power consumption (P_D) from 10mW to 10μW. Pin 19 (CLK) must be active when setting or resetting standby mode. All other clocks (i.e. WCK, etc.) can be inactive. The supply voltage must be maintained at 5 V during standby. The clock to pin 19 may be disabled during standby provided the following set-up and hold conditions are met:



Note:
Standby mode will maintain internal status registers and I/O lines.

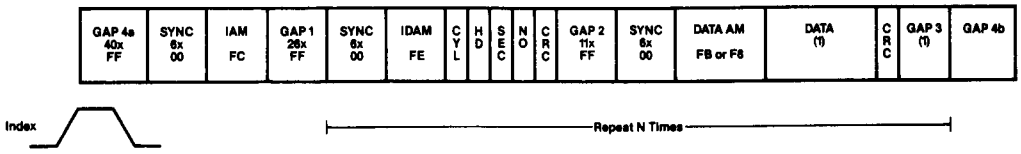
Differences Between the FDC72C65/72C66 and FDC765A/7265

Parameter	FDC72C65	FDC72C66	FDC765A	FDC7265
Track format	IBM	ECMA/ISO	IBM	EMCA/ISO
Tracks to be recalibrated	255		77	255
Skipping time after detection of index pulses	0.2ms (at 4 MHz)		about 1.2 ms (at 4 MHz)	about 0.2 ms (at 4 MHz)
DRQ ↑ $\overline{RD}$ ↓ TE response time	125 ns at 4MHz 250 ns at 8MHz		0.8 μs 1.6 μs	
FDD response latency after unit select signal output	2.5μs at 4MHz 5.0μs at 8MHz		0.5μs 1.0μs	
Multitrack write by tunnel erase head	Yes		No	
Standby function (standby command)	Yes		No	
Software reset command	Yes		No	

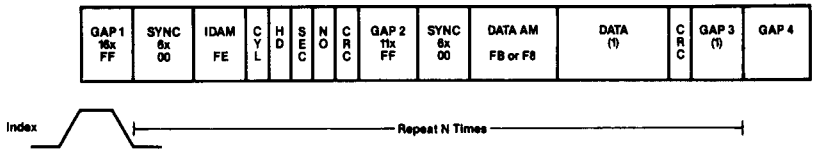
Data Format

Figure 5 shows the data transfer format for the FDC72C65 and FDC72C66 in various modes.

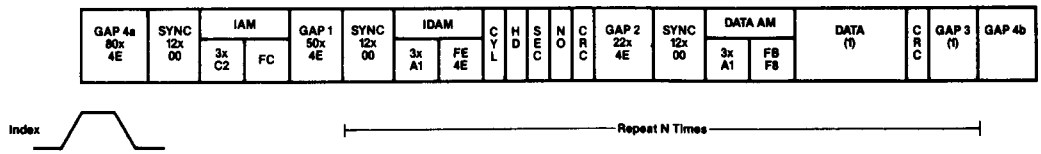
FDC72C65 (FM Mode)



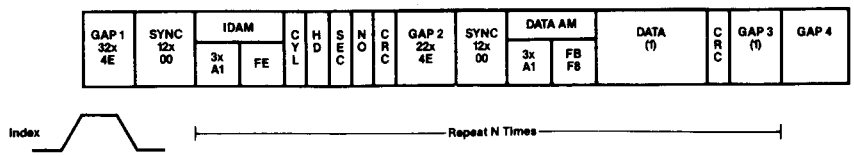
FDC72C66 (FM Mode)



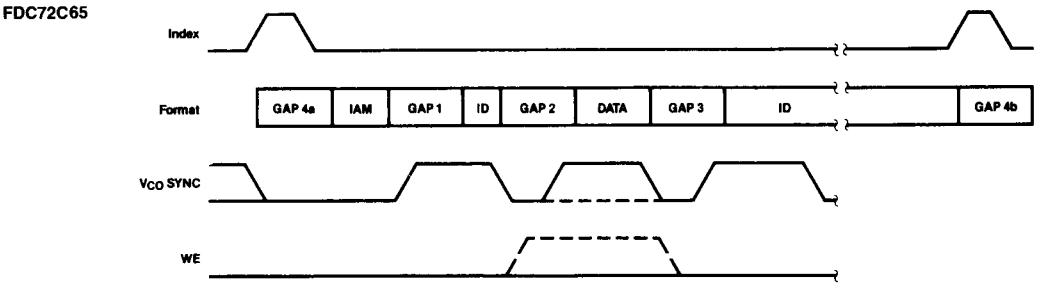
FDC72C65 (MFM Mode)



FDC72C66 (MFM Mode)



FDC72C65



FDC72C66

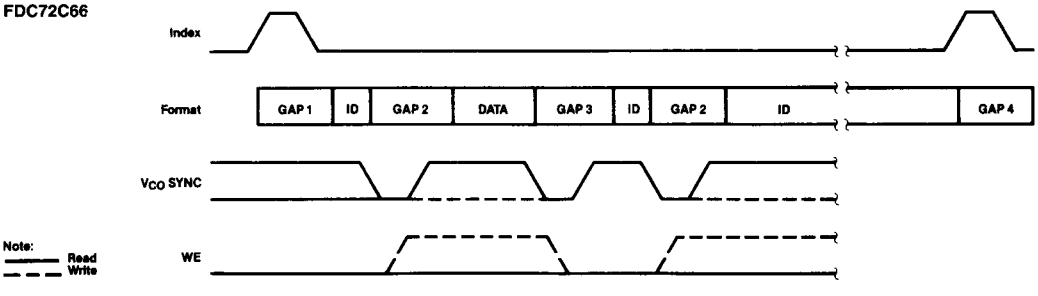


Figure 5. Data Format

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

Power supply voltage, V_{CC} ..... −0.3V to +7V
Input voltage, V_I ..... −0.3V to V_{CC} +0.3V
Output voltage, V_O ..... −0.3V to V_{CC} +0.3V
Operating temperature, T_{OPT} ..... 0°C to +70°C
Storage temperature, T_{STG} ..... −55°C to +125°C
Power dissipation, P_D 50mW

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE $T_A = 25°C$, $f_C = 1MHz$, $V_{CC} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input clock capacitance	$C_{IN}(\phi)$			20	pF	(Note 1)
Input capacitance	C_{IN}			10	pF	(Note 1)
Output capacitance	C_{OUT}			20	pF	(Note 1)

Note:
(1) All pins except pin under test tied to AC ground

DC CHARACTERISTICS

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2.2		V_{CC} +0.5	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200\ \mu A$
Supply current (V_{CC})	I_{DD} I_{DD1}		3 0.7	10 2	mA mA	
Input load current high	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input load current low	I_{LIL}			−10	μA	$V_{IN} = 0V$
Output leakage current high	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Output leakage current low	I_{LOL}			−10	μA	$V_{OUT} = +0.45$ V

AC CHARACTERISTICS

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock period	ϕ_{CY}	120	125 125 250 125	500	ns ns ns ns	(Note 4) 8" FDD 5¼" FDD 3½" Sony (Note 3)
Clock active (high, low)	ϕ_0	40			ns	
Clock rise time	ϕ_r			20	ns	
Clock fall time	ϕ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}\downarrow$	t_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}\uparrow$	t_{RA}	0			ns	
$\overline{RD}$ width	t_{RR}	200			ns	
Data access time from $\overline{RD}\downarrow$	t_{RD}			140	ns	$C_L = 100$ pF
DB to float delay time from $\overline{RD}\uparrow$	t_{DF}	10		85	ns	$C_L = 100$ pF
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}\downarrow$	t_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}\uparrow$	t_{WA}	0			ns	
$\overline{WR}$ width	t_{WW}	200			ns	
Data setup time to $\overline{WR}\uparrow$	t_{DW}	100			ns	
Data hold time from $\overline{WR}\uparrow$	t_{WD}	0			ns	
INT delay time from $\overline{RD}\uparrow$	t_{RI}			400	ns	

AC CHARACTERISTICS CONTINUED

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
INT delay time from $\overline{WR}\uparrow$	t_{WI}			400	ns	
DRQ cycle time	t_{MCY}	13			µs	ϕ_{CY} = 125 ns (Note 4)
$\overline{DACK}\downarrow \rightarrow DRQ\downarrow$ delay	t_{AM}			140	ns	
$DRQ\uparrow \rightarrow \overline{DACK}\downarrow$ delay	t_{MA}	200			ns	ϕ_{CY} = 125 ns (Note 4)
$\overline{DACK}$ width	t_{AA}	2			ϕ_{CY}	
TC width	t_{TC}	1			ϕ_{CY}	
Reset width	t_{RST}	14			ϕ_{CY}	
WCK cycle time	t_{CY}		16 8 8 4 8 4		ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY} ϕ_{CY}	MFM = 0, 5¼" MFM = 1, 5¼" MFM = 0, 8" MFM = 1, 8" MFM = 0, 3½" (Note 3) MFM = 1, 3½" (Note 3)
WCK active time (high)	t_0		2		ϕ_{CY}	
$CLK\uparrow \rightarrow WCK\uparrow$ delay	t_{CWH}	0		40	ns	
$CLK\uparrow \rightarrow WCK\downarrow$ delay	t_{CWL}	0		40	ns	
WCK rise time	t_R			20	ns	
WCK fall time	t_f			20	ns	
Preshift delay time from $WCK\uparrow$	t_{CP}	10		80	ns	
$WCK\uparrow \rightarrow WE\uparrow$ delay	t_{CWE}	10		80	ns	
WDA delay time from $WCK\uparrow$	t_{CD}	10		80	ns	
RDD active time (high)	t_{RDD}	40			ns	
Window cycle time	t_{WCY}		4 2 2 1 2 1		µs µs µs µs µs µs	MFM = 0, 5¼" MFM = 1, 5¼" MFM = 0, 8" MFM = 1, 8" MFM = 0, 3½" (Note 3) MFM = 1, 3½" (Note 3)
Window hold time to RDD	t_{RDW}	15			ns	
Window hold time from RDD	t_{WRD}	15			ns	
$US_{0,1}$ hold time to $\overline{RW}$ / seek$\uparrow$	t_{US}	12			µs	8 MHz clock period (Note 4)
$\overline{RW}$ / seek hold time to low current / direction$\uparrow$	t_{SD}	7			µs	8 MHz clock period (Note 4)
Low current / direction hold time to fault reset / step$\uparrow$	t_{DST}	1.0			µs	8 MHz clock period (Note 4)
$US_{0,1}$ hold time from fault reset / step 1	t_{STU}	5.0			µs	8 MHz clock period (Note 4)
Step active time (high)	t_{STP}	6	7	8	µs	(Note 4)
Step cycle time	t_{SC}	33	(2)	(2)	µs	(Note 4)
Fault reset active time (high)	t_{FR}	8.0		10	µs	(Note 4)
Write data width	t_{WDD}	t_0-50			ns	
$US_{0,1}$ hold time after seek	t_{SU}	15			µs	8 MHz clock period (Note 4)
Seek hold time from DIR	t_{DS}	30			µs	8 MHz clock period (Note 4)
DIR hold time after step	t_{STD}	24			µs	8 MHz clock period (Note 4)
Index pulse width	t_{IDX}	10			ϕ_{CY}	
$\overline{RD}\downarrow$ delay from DRQ	t_{MR}	1			ϕ_{CY}	8 MHz clock period (Note 4)
$\overline{WR}\downarrow$ delay from DRQ	t_{MW}	250			ns	8 MHz clock period (Note 4)
WE or $\overline{RD}$ response time from $DRQ\uparrow$	t_{MRW}			12	µs	8 MHz clock period (Note 4)

Note:

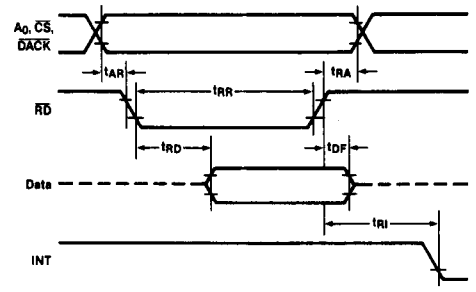
(1) Typical values for T_A = 25°C and nominal supply voltage.

(2) Under software control. The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 ms to 32 ms at 4 MHz clock period.

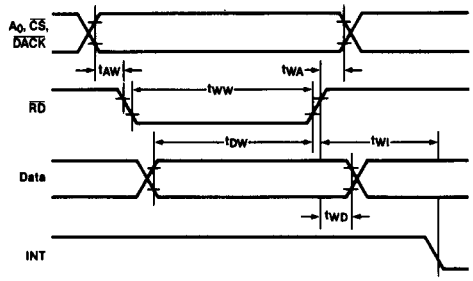
(3) Sony Micro Floppydisk 3½" drive.

(4) Double these values for a 4 MHz clock period.

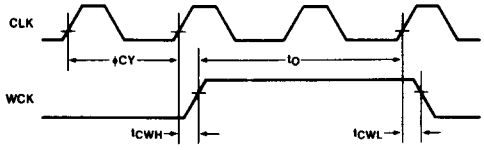
Timing Waveforms



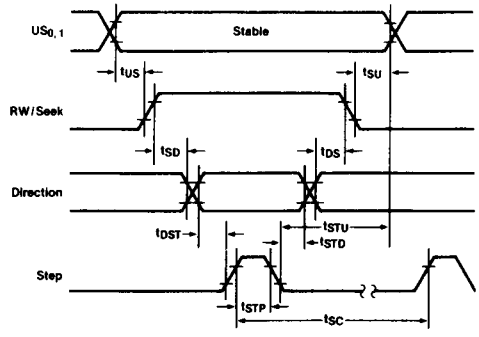
Processor Read Operation



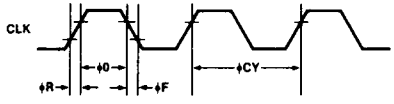
Processor Write Operation



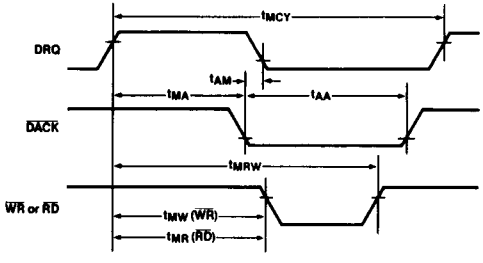
ϕ, WCK Timing



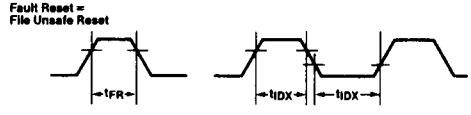
Seek Operation



Clock

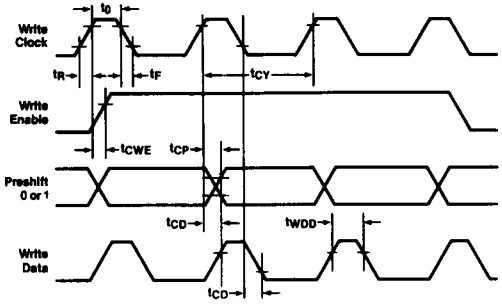


DMA Operation



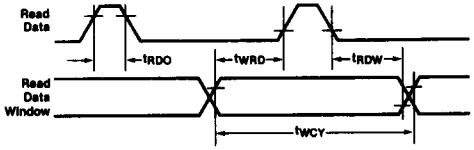
FLT Reset

Timing Waveforms



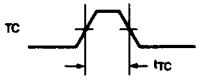
	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

FDD Write Operation

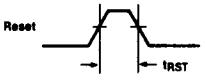


Note: Either polarity data window is valid.

FDD Read Operation



Terminal Count



Reset

SECTION VI

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
516 273 3100 TWX 510 227 8898