Data Sheet

BCM53154/BCM53156/BCM53158

Ultra-Low Power Layer2 GE Switch with 10G Uplinks

General Descriptions

Broadcom's BCM53154/BCM53156/BCM53158 is a family of highly integrated Ethernet switches that are optimally designed for cost-effective low-power applications in the SMB, Enterprise, Service-Provider, SOHO, and Industrial-Ethernet markets that rapidly transition to Gigabit-Ethernet connectivity and beyond. The BCM53154/BCM53156/BCM53158 is based on the industry-leading 28 nm RoboSwitch™ architecture, also known as Robo 2. The product line includes multiple models with 6 to 15 interfaces that support 100M/1GE/2.5GE and 10GE of bandwidth. The various models support Unmanaged, Web-Managed, and Managed modes of operation. The BCM53154/BCM53156/BCM53158 is designed for standalone low port-count configurations, high port-count configurations with support for cascading, and a Port-Extender configuration with support for IEEE 802.1BR.

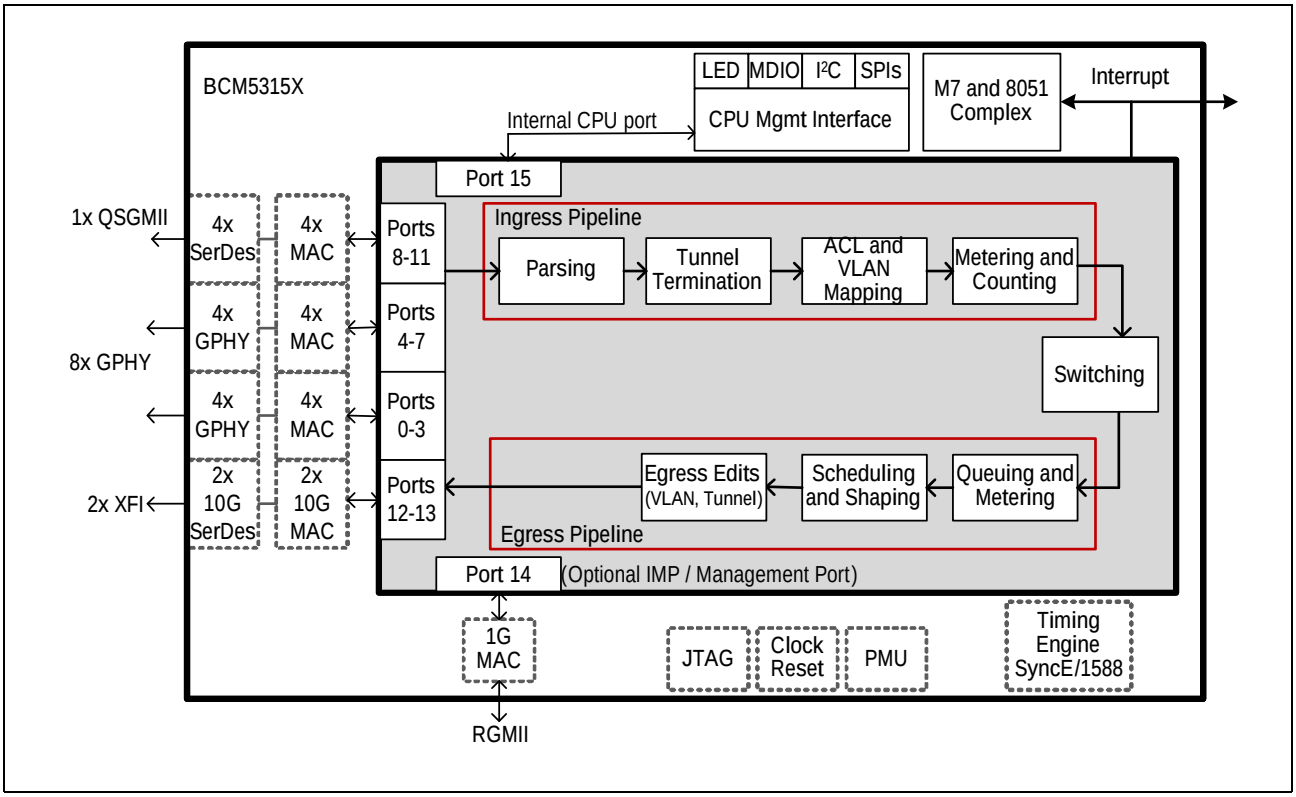
The BCM53154/BCM53156/BCM53158 allows customers to design complete product platforms that target new cost-effective low-power applications demanding 1GE/10GE connectivity. Among those, SMB switch with 10G uplinks, Enterprise switches, routers and security appliances, next generation Industrial Ethernet switches, and Service Provider access equipment.

The BCM53154/BCM53156/BCM53158 is also designed to support high-end applications that require advanced QoS, flexible classification of traffic, sophisticated VLAN manipulation, security features, packet synchronization for time-sensitive networks, and more. The product line takes advantage of a low-power integrated ARM Cortex-M7 CPU to offer on-chip support for certain protocols, including xSTP, LLDP, and IGMP as well as tools for monitoring and troubleshooting. The product line is offered in Commercial-grade as well as Industrial-grade temperature ranges.

Features

- ARM Cortex-M7 at up to 400 MHz.
- Operational modes: Unmanaged, Web-Managed, and Managed.
- Up to 8×10/100/1000BASE-T ports with integrated ultra-low-power GPHYs.
- Up to 1×QSGMII with integrated SerDes.
- Up to 2×10G XFI with KR support.
- Switch cascading.
- 16K entry MAC address table.
- 1K multicast group support.
- 1 MB packet buffer.
- srTCM and trTCM meters (support color aware and color blind modes).
- Eight CoS queues per port with priority flow-control.
- IEEE 802.1p, MAC, and DSCP packet classification.
- Per-queue and per-port shaper.
- 4K VLANs (IEEE 802.1Q) with Virtual Switching Instance (VSI) support.
- 1K CFP rules support (up to 192b key).
- Mirroring and sFlow sampling.
- Loop detection.
- 1K packets and bytes counters.
- 16 LAG trunks (32 supported across cascaded switches). Up to 32 ports in a LAG group.
- VLAN mapping and translation.
- Protection and security mechanisms: port authentication (IEEE 802.1x), isolation groups, BUM traffic metering, DOS filtering.
- IEEE 802.3az Energy Efficient Ethernet (EEE).
- IEEE 802.1BR standards-based port extender.
- 1588 and time-sensitive networking (IEEE 802.1Qbv, IEEE 802.1ASrev).
- Jumbo frame support: up to 9728 bytes.
- 311-pin, 13×13 mm^2 FBGA package (BCM53156/BCM53158).
- 425-pin, 19×19 mm^2 FBGA package (BCM53154).
- JTAG support.
- Includes one UART and MDIO interface, seven I^2C interfaces, and 9 GPIOs (via the MFIO).

Figure 1: Functional Block Diagram



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Chapter 1: Introduction

1.1 Overview

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM53154/BCM53156/BCM53158. This document is for designers interested in integrating the BCM53154/BCM53156/BCM53158 switches into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM53154/BCM53156/BCM53158 switches.

The BCM53154/BCM53156/BCM53158 is a family of highly integrated Ethernet switches that are optimally designed for cost-effective low-power applications in the SMB, Enterprise, Service-Provider, SOHO, and Industrial-Ethernet markets. The BCM53154/BCM53156/BCM53158 is the first family of products in the RoboSwitch® product line to introduce 10GE ports, which are relevant in markets that are rapidly transitioning to Gigabit-Ethernet connectivity anywhere.

The BCM53154/BCM53156/BCM53158 switch core supports full-duplex packet forwarding bandwidth of 33 Gb/s for all packet lengths (64-byte to 9720 jumbo frames). The platform supports oversubscription, with aggregate port speeds up to 39 Gb/s.

The family is based on a core technology that supports:

- Eight 10/100/1000BASE-TX ports with integrated Gigabit MACs (GMACs), and integrated PHYs (GPHYs).
- One QSGMII port (duplex mode only)
- Two 10GE/2.5GE/1GE XFI ports with integrated XMACs
- One RGMII port for PHY-less connection to the management agent (available only in full-duplex mode)
- An integrated Motorola SPI-compatible interface
- High-performance, integrated packet buffer memory
- An address resolution engine
- Virtual Switching Instances (VSI) support
- A high-end traffic-management system
- Support for multiple Synchronization mechanisms (1588v2/SyncE/TSN) for Audio-Video Bridging (AVB, IEEE 802.1Qav) and Time Sensitive Networks (IEEE 802.1bv) Industrial requirements

The GMACs support full-duplex and half-duplex modes for 10 Mb/s and 100 Mb/s, and full-duplex for 1000 Mb/s. Flow control is supported in half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is supported. The GMACs are IEEE 802.3-compliant and support a maximum frame size of 9720 bytes.

The BCM53154/BCM53156/BCM53158X supports advanced ContentAware™ processing using a compact field processor (CFP). Up to four intelligent ContentAware processes are performed in parallel for every packet. This flexible engine uses TCAM-based architecture which allows wildcard capabilities. Action examples include dropping, changing the forward port map, adding forward port, assigning the priority of a frame, and so on. These advanced ContentAware processes are well suited for access control lists (ACLs) and DoS prevention.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 16K unicast addresses. Addresses are added to the table after receiving an error-free packet.

The MIB statistics registers collect receive and transmit statistics for each port and provide direct hardware support for the EtherLike-MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface Port by an external microcontroller.

1.2 Target Markets

The BCM53154/BCM53156/BCM53158 series targets four main markets:

- SMB – Capacity requirement in this market is steadily growing. While 1GE is currently the prominent connectivity speed (about 55% of all links in the SMB), 2016 is the year in which 10GE connectivity is expected to reach the SMB market as well. The BCM53154/BCM53156/BCM53158 was designed to support this market segment by providing 1GE connectivity toward the SMB customers' end nodes and 2.5GE/10GE connectivity toward the WAN.
- Service Provider – The BCM53154/BCM53156/BCM53158 is focused on two sub-segments within the Service Provider market: 10G G/EPON MDU ONUs and 10GE small-cells. The first sub-segment mentioned is expected to drive the next cycle of growth in embedded connectivity. The BCM53154/BCM53156/BCM53158 is designed to complete G/EPON chip-sets in ONU and design and deliver a cost effective and high-speed solution. The series is also designed to be used as an embedded component within a small-cell design as they are upgraded to 2.5GE and 10GE connection.
- Port Extender – This market refers to a new design concept of chassis-based switches that is based on single or dual high-end controlling bridges and multiple lower-cost line cards that are termed *extenders*. The significant forwarding, traffic-management, VLAN resolution, and other high-end operations are done mainly by the controlling bridges while the line cards are nothing but front-end PHYs that enable an increase of port count with a minimal cost addition. To properly operate, chassis-based Port-Extenders are utilizing either of these two new technologies, IEEE 802.1BR and Channelization over Ethernet (CoE), both are supported by the BCM53154/BCM53156/BCM53158 series of switches.
- Industrial Ethernet – This market segment includes switches used for industrial purposes and associated niches like smart lighting and surveillance (also known as Closed-Circuit TV - CCTV). Applications used in this market require many times the transformation of Ethernet from asynchronous technology to synchronous technology in which all platforms in the network transmit and receive at known time slots and traffic has deterministic delay and delay-variation characteristics. To support this synchronization behavior of Ethernet, the BCM53154/BCM53156/BCM53158 has incorporated multiple high-end associated technologies such as SyncE, IEEE 1588v2, Audio-and Video Bridging per IEEE 802.1Qav, IEEE 802.1Qbv, and others.

1.3 Operational Mode

BCM53154/BCM53156/BCM53158 devices support three different operational modes: Unmanaged Mode (U), Web-Managed (W), and Fully-Managed (M). Each one of the devices in the series can be ordered in any of these modes. See Section 12: “Ordering Information,” on page 151 to find the exact part number that represents the operational-mode version of the desired switch.

- Unmanaged mode (U) – This mode should be used by customers who would like to build the most basic switching platform with a single bridging domain, no support for virtual LANs, that is, IEEE 802.1Q VLANS and no ability to rate limit incoming or outgoing traffic. This unmanaged mode does provide customers with 8 traffic classes per port, a default 1:1 mapping between incoming traffic VLAN priority bits and those queues (p-bits with value X will be mapped to queue X+1) and default WRR scheduling weights for improved scheduling of traffic from the queues (the weights are 1:1:2:2:4:4:8:8).

  In this mode, the device is shipped to customers with a basic out-of-the-box configuration that activates the switch in a single, no VLAN support, bridging domain. This basic configuration is available on the device’s internal ROM and no additional memory is required. However, customers can get additional functionality to that mentioned above by using an external flash and downloading Broadcom's Advanced Unmanaged software. This software supports, in addition to the basic functionality, Auto-Loopdetect, Auto-Dos, and Auto-VoIP functionality, autoQoS, and auto IGMP snooping that are further explained here. This mode is termed *Advanced Unmanaged*. Note that this mode is not offered separately from the regular Unmanaged mode (U) as it mainly requires that the end user deploy external flash for additional memory.
- Web-Managed (W) – This mode reflects the usage of the switch with a complete software package from BRCM that uses a web-based GUI to configure and present certain switch characteristics (see Table 1 on page 11). This Managed mode is utilizing the switch's embedded ARM-M7 CPU with the internal RAM memory. The software is running over a light-weight open-source operating system called Open RTOS that supports ~25 web windows to configure the various elements in the switch. Note that the advanced compact Filter processor (CFP) is not supported in Web-managed mode nor most of the advanced VLAN translation capabilities or the synchronization capabilities.
- Fully-Managed (M) – This mode reflects a higher-end environment in which BCM53154/BCM53156/BCM53158 devices are connected to an external CPU and have access to external RAM memory needed for advanced applications. In this mode, the entire feature-set of the BCM53154/BCM53156/BCM53158 devices are operational as seen in Table 1 on page 11.

Table 1: BCM53154/BCM53156/BCM53158 Operational Modes

Layer	Feature	Unmanaged (U) (* = Features Requires Flash)	Web-Managed (W)	Fully Managed (M)
System (CPU, Memory, Basic Software, Power)	Processor	Integrated M7 CPU	Integrated M7 CPU	External CPU
	ROM memory for image and config	Internal ROM + Flash Flash is necessary	Flash 8 MB is sufficient	Flash
	Operating System	Bare Metal	OpenRTOS	Linux
	Software Format Delivered to Customers	Binary Code	Source Code (ROBO-OS™)	Broadcom (XGS equivalent) SDK (API) + Robo 2-specific SDK (FSAL-API)
	SDK Support	✓ Initialization RSDK	✓ Web-Managed RSDK	✓ Full RSDK + Full XGS SDK
	Direct Register Access Support	✓	✓	✓
	Packet Memory	1 MB	768K	640K to 768K
	CPU Memory	8 KB	352 KB (256 KB from PB + 96 KB from TCM)	384K to 256K

Table 1: BCM53154/BCM53156/BCM53158 Operational Modes (Continued)

Layer	Feature	Unmanaged (U) (* = Features Requires Flash)	Web-Managed (W)	Fully Managed (M)
L1	Cable Diagnostic	✓*	✓	✓
	Cascading[a]	✓*	✓	✓
	EEE power saving (IEEE 802.3az)[b]	✓	✓	✓
	AVS[c]	✓*	✓	✓
	Link Aggregation (LAG)	×	✓ (16/16) hashing: da / da-sa / da-sa-vlan / da-sa-vlan-ip	✓ (16/16) hashing: flexible
L2 Forwarding	Jumbo Frames	✓ (9720)	✓ (9720)	✓ (9720)
	Switching/MAC Learning	✓ (16K)	✓ (16K)	✓ (16K)
	Broadcast Storm Control	✓*	✓	✓
	VLAN support (multiple bridging domains)	×	✓ (128)	✓ (4K – via VSI)
	VLAN translation	×	×	× Via N type interface (LIM Table) – 2K interfaces
	Isolation group (tree)	×	✓ (4)	✓ (4)
	Ingress Mirroring	×	×	✓
	Egress Mirroring	×	×	✓
	Traffic Sampling	×	×	✓
	CFP support (ACLs)	×	×	✓ (1K)
	AutoLoop	✓*	×	×
	AutoVOIP	✓* (256 SA)	✓ (256 SA)	×
	AutoDOS	✓*	✓	×

Table 1: BCM53154/BCM53156/BCM53158 Operational Modes (Continued)

Layer	Feature	Unmanaged (U) (* = Features Requires Flash)	Web-Managed (W)	Fully Managed (M)
L2 QoS	Queues per port	8	8	8
	IEEE 802.1p Priority mapping	✓* Through AutoQoS – mapping is fixed	✓	✓
	DSCP priority mapping	✓* Through AutoQoS – mapping is fixed	✓	✓
	Scheduling configurable SP	✓* Through AutoQoS	✓	✓
	Scheduling configurable WRR	✓* Through AutoQoS - Weights are configurable	✓	✓
	Metering Rate Limiting	×	✓ (128) CIR/CBS/EIR/EBS per port only Ingress QoS meters – 128	✓ (128, 512) CIR/CBS/EIR/EBS Ingress CoS meters – 128 Flow meters – 512
	Shaping queue/port	×	✓	✓
	Hierarchical Shaping	×	×	✓
	Flow Control – PAUSE IEEE 802.3x	✓*	✓	✓
	Flow Control – PFC IEEE 802.1QBB	✓*	✓	✓
Management	Debug CLI	✓	✓	✓
	RESTful API	×	✓	×
	Rx and Tx Counters	×	✓	✓
Multicast	IGMP Snooping	✓*	✓ (32)	✓ (1K)
Protocols and Advanced Features	LLDP	×	✓	✓
	Rapid Spanning Tree	×	✓ (128)	✓ (128)
	Cisco MAC-in-MAC	×	×	✓
	Port Extender/IEEE 802.1BR	×	✓ (available in the BCM53158XP)	✓

Table 1: BCM53154/BCM53156/BCM53158 Operational Modes (Continued)

Layer	Feature	Unmanaged (U) (* = Features Requires Flash)	Web-Managed (W)	Fully Managed (M)
Time-Sensitive Networking (TSN) Support	IEEE 802.1AS (subset of 1588) – One Step	×	✓	✓
	IEEE 802.1AS (subset of 1588) – Two Steps	×	✓	✓
	IEEE 802.1Qbv (enhancements ftraffic scheduling)	×	×	✓
	IEEE 802.1Qcc (Stream Reservation Protocol –SRP, HW support)	×	×	✓
	Cut-Through mode[d]	×	×	✓
	IEEE 802.1Qav (TSN Forwarding and Queuing)	×	×	✓
	AVB (class A and class B)	×	×	✓

a. The max support port is 30 in cascaded mode due to a PG2LPG table limitation (for ROBO-OS, the internal M7 be configured as port 15 used).

b. When EEE is enabled (EEE feature is for GPHY port only), the cut-through latency time is impacted causing very high latency (tens of microseconds). The selection of either EEE or cut-through does not impact performance since both are not available.

c. AVS is enabled by default in GA 1.4.5 or newer for UM only. ROBO-OS/RSDK and XGSDK must use the following procedure to enable AVS accordingly:

For ROBO-OS/RSDK, compile a new image with AVS enabled by adding the CONFIG_AVS=1 option.

For XGSDK, compile a new image with AVS enabled by adding the following statement on Make.local file as follows: CONFIG_AVS=1.

d. Cut-through is not supported on 10G ports and is only supported between ports running at the same speed.

1.4 BCM53154/BCM53156/BCM53158 Devices

The BCM53156X/BCM53158X series includes about 20 different part numbers that differ in their support for 10GE XFI interfaces, their package size, their ambient temperature support, and their operational mode support. See the full SKU list in Section 12: “Ordering Information,” on page 151.

The BCM53154/BCM53156/BCM53158 devices are offered in one 13×13 mm^2 package with 311 pins.

Table 2 provides a detailed list of the physical characteristics for each device in the BCM53154/BCM53156/BCM53158 family of switches.

Table 2: BCM53154/BCM53156/BCM53158 Family Features

Features	BCM53154	BCM53156	BCM53158
RGMII (port 14)	1	1	1
GPHY (ports 0 through 7) 10/100BASE-T	0	0	0
GPHY (ports 0 through 7) 10/100/1000BASE-T	4	8	8
SGMII (ports 8 through 11) 100/1000BASE-FX/2500BASE-FXF[a]	1	0	0
QSGMII (ports 8 through 11)[a]	0	0	1
XFI (ports 12 through 13) 2.5GE/1GE	0	0	0
XFI (ports 12 through 13) 10GE/2.5GE/1GE[b]	0	1	2
MDIO	1	1	1
SPI	3 (QSPI+2SP)	3 (QSPI+2SP)	3 (QSPI+2SP)
LED (28 pins)	Parallel	N/A	N/A
LED (2 pins)[c]	Serial	Serial	Serial
JTAG (w/ 2 JTCE)	1	1	1
1588	Yes	No	No
SyncE	Yes	Yes	Yes
I^2C	7[d]	7	7
MFIO	16	9	9
WB-FBGA	19 x 19 mm^2	13 x 13 mm^2	13 x 13 mm^2
Package	0.8 mm pitch	0.65 mm pitch	0.65 mm pitch
	425 balls	311 balls	311 balls
PCB Layers	4	4	4
Weight	1100 mg	511 mg	511 mg
Ambient Temp[e]	–40°C to +85°C	0°C to 70°C	0°C to 70°C

a. QSGMII/SGMII port supports full-duplex mode only.

b. Ports 12 to 13 10G mode supported as 10G-XFI ,10G-SFI (optical module), and 10G-SFI(DAC– direct attached cable).

c. Serial LED uses two bits from the 28-bit parallel LED. Both cannot be active at the same time.

d. The 19 × 19 mm^2 package has seven I^2C (six dedicated + one muxed on MFIO) and the 13 × 13 mm^2 package has 7× I^2C (all muxed on MFIO).

e. 0°C to 70°C for commercial SKUs; –40°C to +85°C for industrial SKUs.

1.5 System Functional Blocks

1.5.1 Overview

The BCM53154/BCM53156/BCM53158 includes the following blocks:

- Media Access Controller
- Integrated 10/100/1000 PHY
- Interdevice Interface
- MIB Engine
- Integrated High-Performance Memory
- Robo 2 Switch Core

Each of these blocks is discussed in additional detail in the following sections.

1.5.2 Media Access Controller

The BCM53154/BCM53156/BCM53158 contains eight 10/100/1000 MACs, and four 10/100/1000/2.5G MACs.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3, IEEE 802.3u, and IEEE 802.3x-compliant.

1.5.2.1 Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than standard max. frame size or 9,720 bytes for jumbo-enabled ports.

NOTE: Frames longer than standard max. frame size are considered oversized frames. When jumbo-frame mode is enabled, only the frames longer than 9,720 bytes are bad frames and dropped.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled using register settings.

1.5.2.2 Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision back-off, and inter-packet gap enforcement.

In 10/100 Mb/s half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the back-off algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the back-off algorithm starts over at the initial state, the collision counter is reset, and attempts to transmit the current frame continue. Following a late collision, the frame is aborted, and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96-bit times of IPG have been observed. Transmit functions can be disabled using register settings.

1.5.2.3 Flow Control

The BCM53154/BCM53156/BCM53158 implements an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53154/BCM53156/BCM53158 initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in full-duplex mode.

1.5.2.3.1 10/100 Mb/s Half-Duplex

In 10/100 half-duplex mode, the MAC back-pressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

1.5.2.3.2 10/100/1000 Mb/s Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

1.5.2.3.3 Priority Flow Control

Priority Flow Control (PFC) is a mechanism of conveying the per priority XON/XOFF information for 8 different classes using MAC control frames. UniMac provides the flexibility to program the DA, TYPE, and OPCODE fields for the PFC frames. The PFC feature can be independently enabled inside the MAC and pause should be disabled while PFC is operational to ensure IEEE compliance.

1.5.3 Integrated 10/100/1000 PHY

There are two integrated quad-PHY blocks in the BCM53154/BCM53156/BCM53158. For additional information see Copper Interface. The following sections describe the operations of the internal PHY block.

1.5.3.1 Encoder

The PHY is the Ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface, which performs the reverse process on data received at the MDI interface. The registers of the PHY are read using the Programming Interfaces. The following sections describe the operations of the internal PHY block. For additional information, see Copper Interface.

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs preequalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM53154/BCM53156/BCM53158 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/ K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in Stream Cipher. The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM53154/BCM53156/BCM53158 simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM-5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first two bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier-extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with the IEEE 802.3ab standard and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

1.5.3.2 Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn-to-zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM53154/BCM53156/BCM53158 asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails, or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. Decoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

1.5.3.3 Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch-detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled.

1.5.3.4 Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM53154/BCM53156/BCM53158 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

1.5.3.5 Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

1.5.3.6 Cross Talk Canceler

The BCM53154/BCM53156/BCM53158 transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

1.5.3.7 Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise rejection
- Fast settling time
- Low bit error rate

1.5.3.8 Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

1.5.3.9 Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM53154/BCM53156/BCM53158 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

1.5.3.10 Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM-5, MLT3, and Manchester coded symbols. The transmit DAC performs signal-wave shaping that decreases the unwanted high-frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and therefore, produces very low noise transmit signals.

1.5.3.11 Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53154/BCM53156/BCM53158 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM53154/BCM53156/BCM53158 detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM53154/BCM53156/BCM53158 is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

1.5.3.12 Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM53154/BCM53156/BCM53158 has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM53154/BCM53156/BCM53158) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable.
- Polarity errors caused by the swapping of wires within a pair.

The BCM53154/BCM53156/BCM53158 also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM53154/BCM53156/BCM53158 can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mb/s operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

1.5.3.13 Automatic MDI Crossover

During copper auto-negotiation, one end of the link must perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53154/BCM53156/BCM53158 can perform an automatic media-dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM53154/BCM53156/BCM53158 normally transmits and receives on the TRD pins.

When connecting to another device that does not perform MDI crossover, the BCM53154/BCM53156/BCM53158 automatically switches its TRD in pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM53154/BCM53156/BCM53158 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function cannot be disabled when in 1000BASE-T mode. During 10BASE-TX and 100BASE-T operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default works only when auto-negotiation is enabled. This function can be disabled during auto-negotiation using a register write.

NOTE: This function operates only when the copper auto-negotiation is enabled.

1.5.3.14 10/100BASE-TX Forced Mode Auto-MDIX

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for at least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100TX idles are detected. Once detected, the PHY returns to forced mode operation.

NOTE: This function operates only when the copper auto-negotiation is disabled.

1.5.3.15 PHY Address

The BCM53154/BCM53156/BCM53158 has eight unique PHY addresses for MII management of the internal PHYs. The PHY addresses for each port are as follows,

- PHY address for Port 0 is 1
- PHY address for Port 1 is 2
- PHY address for Port 2 is 3
- PHY address for Port 3 is 4
- PHY address for Port 4 is 5
- PHY address for Port 5 is 6
- PHY address for Port 6 is 7
- PHY address for Port 7 is 8

1.5.3.16 Super Isolate Mode

When in Super Isolate mode, the transmit and receive functions on the Copper Media Dependent Interface are disabled (no link is established with the PHY's copper link partner). Any data received from the switch is ignored by the BCM53154/BCM53156/BCM53158 and no data is sent from the BCM53154/BCM53156/BCM53158.

1.5.3.17 Standby Power-Down Mode

The BCM53154/BCM53156/BCM53158 can be placed into standby power-down mode using software commands. In this mode, all PHY functions except for the serial management interface are disabled. There are three ways to exit standby power-down mode:

- Clear MII Control register, bit 11 = 0.
- Set the software RESET bit 15.
- Assert the hardware $\overline{\text{RESET}}$ pin.

Read or write operations to any MII register, other than MII Control register, while the device is in the standby power-down mode returns unpredictable results. Upon exiting standby power-down mode, the BCM53154/BCM53156/BCM53158 remains in an internal reset state for 40 µs and then resumes normal operation.

1.5.3.18 Auto Power-Down Mode

The BCM53154/BCM53156/BCM53158 can be placed into auto power-down mode. Auto power-down mode reduces device power when the signal from the copper link partner is not present. The auto power-down mode works whether the device is in Auto-negotiation Enabled or Forced mode. This mode is enabled by setting bit 5 =1 of Auto Power-Down register. When auto power-down mode is enabled, the BCM53154/BCM53156/BCM53158 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. The energy-detect circuit is always enabled even when a port is in low-power mode. When the BCM53154/BCM53156/BCM53158 is in auto power-down mode, it wakes up after 2.7s or 5.4s, which determined by bit 4 of Auto Power-Down register, and sends link pulses to the link partner. The BCM53154/BCM53156/BCM53158 enters normal operation and establishes a link if energy is detected.

NOTE: Auto power-down mode is a Broadcom proprietary feature and is based on IEEE standard.

1.5.3.19 External Loopback Mode

The External Loopback mode allows in-circuit testing of the BCM53154/BCM53156/BCM53158 as well as the transmit path through the magnetics and the RJ-45 connector. External loopback can be performed with and without a jumper block. External loopback with a jumper block tests the path through the magnetics and RJ-45 connector. External loopback without the jumper block tests only the BCM53154/BCM53156/BCM53158's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1----------3
2----------6
4----------7
5----------8

The following six tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

Table 3: 1000BASE-T External Loopback with External Loopback Plug

Register Writes	Comments
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode
Write 0040h to MII Control register	Enable Force 1000BASE-T
Write 8400h to Auxiliary Control register	Enable External Loopback Mode with external loopback plug

Table 4: 1000BASE-T External Loopback Without External Loopback Plug

Register Writes	Comments
Write 1800h to 1000BASE-T Control register	Enable 1000BASE-T Master Mode
Write 0040h to MII Control register	Enable Force 1000BASE-T
Write 8400h to Auxiliary Control register	Enable External Loopback Mode
Write 0014h to Auxiliary Control register	Enable External Loopback Mode without external loopback plug

Table 5: 100BASE-TX External Loopback with External Loopback Plug

Register Writes	Comments
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode

Table 6: 100BASE-TX External Loopback Without External Loopback Plug

Register Writes	Comment
Write 2100h to MII Control register	Enable Force 100BASE-TX full-duplex mode
Write 0014h to Auxiliary Control register	Enable external loopback mode without external loopback plug

Table 7: 10BASE-T External Loopback with External Loopback Plug

Register Writes	Comments
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode

Table 8: 10BASE-T External Loopback Without External Loopback Plug

Register Writes	Comments
Write 0100h to MII Control register	Enable Force 10BASE-T full-duplex mode
Write 0014h to Auxiliary Control register	Enable external loopback mode without external loopback plug

NOTE: To exit the External Loopback mode, a software or hardware reset is recommended.

1.5.3.20 Full-Duplex Mode

The BCM53154/BCM53156/BCM53158 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

1.5.3.20.1 Copper Mode

When auto-negotiation is disabled, full-duplex operation can be enabled using register settings.

When auto-negotiation is enabled, the full-duplex capability is advertised for one of the following, depending on the register settings:

- 10BASE-T
- 100BASE-T
- 1000BASE-T

1.5.3.21 Master/Slave Configuration

In 1000BASE-T mode, the BCM53154/BCM53156/BCM53158 and its link partner perform loop timing. One end of the link must be configured as the timing master, and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. Each end generates an 11-bit random seed if the two settings are equal, and the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM53154/BCM53156/BCM53158 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted. This is used to set the BCM53154/BCM53156/BCM53158 to manual master/slave configuration or to set the advertised repeater/DTE configuration.

1.5.3.22 Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM53154/BCM53156/BCM53158 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM53154/BCM53156/BCM53158 is configured to advertise 1000BASE-T capability.

The BCM53154/BCM53156/BCM53158 also supports software controlled Next Page exchanges. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM53154/BCM53156/BCM53158 automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM53154/BCM53156/BCM53158 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM53154/BCM53156/BCM53158 is not configured to advertise 1000BASE-T capability, the BCM53154/BCM53156/BCM53158 does not advertise Next Page ability.

1.5.3.23 XLMAC

XLMAC is used for the implementation of 10G Ethernet layer for the BCM53154/BCM53156/BCM53158. The XLMAC core is designed as a single module, supporting four 10G/2.5G/1G/100M/10M MACs. The basic idea is to have a single core optimized for multi-lane operation to save area and power.

1.5.4 Interdevice Interface

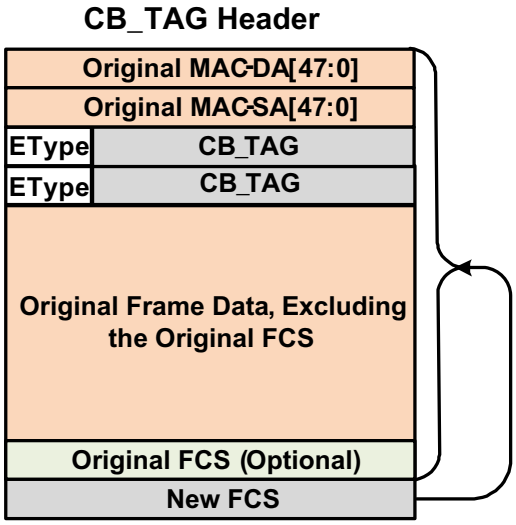
The BCM53154/BCM53156/BCM53158 can connect to two types of external devices: another BCM53154/BCM53156/BCM53158 (cascade) and/or and external processor (CP). The information required for these two application is similar and uses a common header.

The processor can be connected to any port including the internal processor. In Robo terminology, this port is designated as an IMP (internal management port). Frames that are sent to these destinations use the same forwarding rules as any other destination, for example DLIs. There are various ways frames can be directed to each of these destinations including the CFP, ARL, and various filters. Part of the DLI instruction could be to insert the CB tag which provides additional information to aid in processing the frames.

There is one type of IMP header designs which the BCM53154/BCM53156/BCM53158 supports: CB TAG – 8B CB tag which is inserted directly after the MAC-SA

- This format is parseable via the CT-TAG Ethertype.
- This format might include an optional timestamp with a separate Ethertype.

Figure 2: IMP/CB Header Formats



The following rules and guidelines are used for:

- All frames on a cascade port will carry the CB tag.
- Traffic on the IMP port may or may not have the CB tag.
- Normal processing (for example, a port is the destination of the frame) can be sent without a tag.
- When a CB receives a frame with a CB_TAG, the SPG, SLI, and VSI are reconstituted based on information in the tag. It is presented to the ARL lookups as if the frame was processed by the receive logic.
- There are few exceptions to this: traps, mirroring and directed forwarding.
- After the tag is parsed it is removed.

NOTE: For unicast, multicast, traps, and exception forwarding, it is intended that the source information (SPG, LIN, VSI) is populated in the receive header. This enables the CPU to use this in processing to determine the how to forward the frame. In addition, it is expected the CPU properly sets these fields when it sends a frame to the switch which is sent out.

The Switch to CP and CP to Switch tag formats are purposely defined to be consistent across the IMP and Cascade modes. The forwarding codes (fwd_op) are defined to allow the hardware to interpret the intended function from the code point regardless of the specific IMP or Cascade type in most cases.

1.5.4.1 Switch to Control Plane: CB Tag

This tag is used to communicate information to an attached CPU or cascaded BCM53154/BCM53156/BCM53158. The format and fields are defined in the following tables. The tag is attached to frames using editing directives. The directive could be associated with a port (PET table) or DLI. The Ethertype for this tag is taken from a configuration register. The format and fields are defined in Table 9.

Table 9: Switch to CB TAG Format

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>09</th><th>08</th><th>07</th><th>06</th><th>05</th><th>04</th><th>03</th><th>02</th><th>01</th><th>00</th></tr>
<tr><td colspan="16">Ethertype</td></tr>
<tr><td colspan="3">TC</td><td colspan="2">DP</td><td colspan="3">FWD_OP</td><td>DEV</td><td colspan="8">LBH/TRAP_GROUP/SPP/DPP</td></tr>
<tr><td colspan="12">DEST[11:0] - depends on FWD_OP {for example, DLLI/DG/EXCEPTION}</td><td>R</td><td>R</td><td colspan="2">SPG</td></tr>
<tr><td colspan="3">SPG</td><td>T</td><td colspan="12">N_VSI [11:0] (VSI or LIN based on T)</td></tr>
</table>

Table 10: Switch to CP Header Format Fields

Field	Function
Ethertype	Configured value
TC	TC value classified for the packet by the switch
DP	Discard precedence
DEV	Source device identifier; configured by software
SPG	Source Port Group – SPG determined for the frame
FWD_OP	Forwarding Operation – see table
T	LIN Type indicator. 0 is LIN, 1 is PV format
N_VSI	Source Local Logical Interface: If T = 1 (type PV), SLLI = {1,0,SPG}; VSI=N_VSI else(type LIN) SLLI={0,N_VSI}; VSI=LIN2VSI(N_VSI);
DEST - overlay	Overlay field with one of the following depending on FWD_OP
DLLI	Destination Logical Local Interface: If FWD_OP = UNICAST
DG	Destination Group (multicast/broadcast): If FWD_OP = MULTICAST
EXCEPTION	Exception – Identifies the reason a trap was triggered (TRAP, SLIC, CFP): If FWD_OP = TRAP
LBH - overlay	Trap Group/Load Balancing Hash : If FWD_OP=TRAP, TRAP_GROUP else LBH
LBH	Load balancing hash- Valid for all op codes except 2
Trap_group	Trap group for the SLICT and CFP traps in FWD_OP=2
SPP	Source Physical Port for traps (FWD_OP=2)
DPP	Destination Physical Port
RSVD	Reserved – write as zero, ignore on receipt

The forwarding operation (FWD_OP) field defines the content of the DEST field and provides information to the CPU regarding why the frame was delivered. The DEST field in the header is overlay with number of meanings summarized in the following table.

Table 11: IMP Header Forwarding Operation: Switch to CP

FWDOP	Function	DEST	LRN?	TG/LBH/SPP	Notes – processing at EPP
0	CP Directed Forwarding	0	No	DPP	Frame is directly sent on port specified by LBH/DPP field.
0	Unicast Directed Forwarding	DLLI	Yes	LBH	Unicast forwarding with known destination, that is, the DLI. The SPG, N_VSI, and T fields are used to reconstitute the SLI for the frame before the ARL Source lookup is done.
1	Multicast Directed Forwarding	DG	Yes	LBH	Multicast forwarding with known destination i.e. DG. The SPG, N_VSI, and T fields are used to reconstitute the SLI for the frame before the ARL Source lookup is done.
2[a]	SA Learn	SA_LRN (trap_id)	Yes	LBH	Learning message: This is generated based on SA Miss in the source device ARL lookup. The SPG, T and N_VSI are used to in the ARL lookup. This is converted to CA_SA_LRN trap.
2[a]	SA Move	SA_MOVE (trap_id)	Yes	LBH	SA Move message: This is generated based on SA move in the source device ARL lookup. The SPG, T and N_VSI are used to in the ARL lookup. This is converted to CA_SA_LRN trap.
2[a]	Mirror	128-191 (mirror_Id)	No	LBH	This is a copy generated due to mirroring, the mirror id is extracted from the DEST and the MTGT is used to determine how the frame is handled.
2[a]	Trap	1-127 (trap_id)	No	SPP	This is a copy generated due to a trap condition. The trap_id is extracted from the DEST field and the TCT table will govern the handling of this frame.
2[a]	SLIC_TRAP	256-511 (slic_trap)	No	Trap_group	This is a copy generated due to a SLIC trap condition. The trap_group is extracted from the LBH field and the MTGT table is use to determine how the frame is handled.
2[a]	CFP_TRAP	2048-3071 (action_idx)	No	Trap_group	This is a copy generated due to a CFP trap condition. The trap_group is extracted from the LBH field and the MTGT table is use to determine how the frame is handled.
2[a]	NULL TAG	0x0	Yes	X	NOP TAG – CB tag is removed and processed as if it arrived on the CPU port (backwards compatibility so all frames can have a tag), This use and unused trap_group code point.
3–7	Reserved	n/a	n/a	Na/	Reserved for future use.

a. For FWD_OP = 2 the DEST is defined as an EXCEPTION following the encoding shown in Figure 36.

Here are some notes on processing frames at the CPU/Cascaded Device:

- The CB tag is removed on ingress.
- If fwd_op = 0x0 and DLLI is zero, a valid destination was not determined by the switch (DLF destination lookup failure).
- Flooding uses a multicast forwarding with a zero DG. In this case, the flooding map (pg_map) comes from the VSIT based on the VSI in the frame (or LIN2VSI).
- Multicast is handled by used the DG as multicast group.
- For FWD_OP = 2 the encoding the DEST field is used to identify the type of frame (SA-Learn, Mirror, TRAP). The encoding follows the EXCEPTION space shown in Figure 36.
- The DEV field must be preserved if the frame is sent to a CPU with CB_TAG. This allows the CPU to determine which of the two devices the originated exception frame.
- SA learning and SA movement traps are converted to cascaded version of the trap and the {vsi, smac} is inserted in the ARL table if possible.
- Mirror implies the frame was mirrored or sampled; the mirror_group is extracted from the DEST field and the mirror is handled group gives further information or will be used by a cascaded BCM53154/BCM53156/BCM53158 to process the mirror.

- SA learn packets will be locally learned and converted to local cascaded traps for cascade processing.
- The trap packet uses the trap_group to process the frame. Note this is the only format that has a SPP versus a SPG.

1.5.4.2 Switch to Control Plane: Time Stamp Tag

This section describes the tag used from the switch to CPU to send the time stamp. This tag is added using an egress editing directive. The format and fields are defined in the following tables. The Ethertype for this tag is taken from a configuration register.

Table 12: Egress CB TS Tag

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ethertype															
TIMESTAMP[47:32]															
TIMESTAMP[31:16]															
TIMESTAMP[15:0]															

The Ethertype is taken from a software configured register. Timestamp is the 48 bit value sampled at Start of Packet when the frame arrived.

1.5.4.3 Control Plane to Switch: CB Tag

This section describes the tag used from the Control Plane to Switch. The fields are the same as the Switch to CP format described above. Normal frame processing (Unicast, Multicast, and Flooding) rely on the SPG, T and N_VSI field being set properly by the CPU. As noted before, this fields will be valid for frames received by the CPU. It is therefore possible, to direct this frame to a DLI by simply populating the DLI, FWD_OP and sending the frame back into the switch using this format. The following notes apply to sending frames from the CPU:

- To send a Unicast frame out a port group; Frame learned by ARL and egress edits are applied:
  - Set FWD_OP=0 to Unicast Directed Forwarding
  - Set DEST = DLLI - frame will be forwarded based specified DLI
  - Set T, SPG, N_VSI - frame will be learned in this context
- To send a Unicast frame out a physical port without any checks (VLAN membership, STP, or filters); Frame is not learned by ARL and egress edits are not applied:
  - Set FWD_OP=0 to Unicast Directed Forwarding
  - Set DEST = 0
  - Set LBH/DPP field to desired port (DPP); Note this is the only format that has a DPP versus DPG.
- To send a frame to a multicast group:
  - Set FWD_OP=1 to Multicast Directed Forwarding;
  - Set DEST to DG - frame will be forwarded based specified DLI
  - Set T, SPG, N_VSI - the SLLID to SLLID for frame will be derived from these fields for source port knock-out.
- To send a frame and have the switch forward the frame; Frame is learned by ARL:
  - Send the frame without the IMP/CB tag

1.5.5 MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53154/BCM53156/BCM53158 implements 66 MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. This latter group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The section below describes each individual counter.

The BCM53154/BCM53156/BCM53158 offers the MIB snapshot feature per port. A snapshot of a selected port MIB registers can be captured and available to the users while MIB counters are continuing to count.

1.5.5.1 MIB Counters

All counters can be read/write access. The reset values are all zero.

Table 13: Receive MIB Counters (per port)

Receive Counter	Width	Description
RxDropPkts	32	Number of good packets received by a port that were dropped due to a lack of resources (for example, lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (for example, receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters.
RxOctets	64	Number of data bytes received by a port (excluding preamble, but including FCS), including bad packets.
RxBroadcastPkts	32	Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed.
RxMulticastPkts	32	Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed.
RxSAChanges	32	Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed.
RxUndersizePkts	32	Number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS).
RxOversizePkts	32	Number of good packets received by a port that are greater than standard max frame size. The maximum packet size can be programmed.
RxFragments	32	Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
RxJabbers	32	Number of packets received by a port that are longer than standard max frame size and have either an FCS error or an alignment error.
RxUnicastPkts	32	Number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed.
RxAlignmentErrors	32	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.
RxFCSErrors	32	Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets	64	Total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed.
JumboPktCount	32	Number of good packets received by a port that are greater than the standard maximum size and less than or equal to the jumbo packet size, regardless of CRC or alignment errors.

Table 13: Receive MIB Counters (per port) (Continued)

Receive Counter	Width	Description
RxPausePfcPkts	32	When PAUSE is configured: This counter counts the number of PAUSE frame on the port. When the port is configured in PFC mode it counts the number of PFC frames. Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88–08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00–01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network.
RxSymbolErrors	32	Total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event.
RxDiscard	32	Number of good packets received by a port that were discarded by the Forwarding Process. This would include any shaping or DOS filters.
RxPkts64Octets	32	Number of packets received (including error packets) that are 64 bytes long.
RxPkts65to127Octets	32	Number of packets received (including error packets) that are between 65 and 127 bytes long.
RxPkts128to255Octets	32	Number of packets received (including error packets) that are between 128 and 255 bytes long.
RxPkts256to511Octets	32	Number of packets received (including error packets) that are between 256 and 511 bytes long.
RxPkts512to1023Octets	32	Number of packets received (including error packets) that are between 512 and 1023 bytes long.
RxPkts1024toMaxPktOctets	32	Number of packets received (include error packets) that are between 1024 and the standard maximum packet size inclusive.

Table 14: Transmit MIB Counters

Transmit Counter	Width	Description
TxDropPkts	32	This counter is incremented every time a transmit packet is dropped due to lack of resources (for example, transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters.
TxOctets	64	Total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts	32	Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts	32	Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions	32	Number of collisions experienced by a port during packet transmissions.
TxUnicastPkts	32	Number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision	32	Number of packets successfully transmitted by a port that have experienced exactly one collision.
TxMultipleCollision	32	Number of packets successfully transmitted by a port that have experienced more than one collision.
TxDeferredTransmit	32	Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. This only applies to the Half Duplex mode, while the Carrier Sensor Busy.
TxLateCollision	32	Number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxExcessiveCollision	32	Number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.
TxPausePfcPkts	32	Number of PAUSE control frames sent when the port is configured in PAUSE mode. In PFC mode, it counts the number of PFC frames sent.
TxFrameInDisc	32	Number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). This attribute only increments if a network device is not acting in compliance with a flow control request or the ROBO GE Switchcore internal flow-control/buffering scheme has been configured incorrectly.
TxQ0PKT	32	Total number of good packets transmitted on COS0, which is specified in MIB queue select register when QoS is enabled.
TxQ1PKT	32	Total number of good packets transmitted on COS1, which is specified in MIB queue select register when QoS is enabled.
TxQ2PKT	32	Total number of good packets transmitted on COS2, which is specified in MIB queue select register when QoS is enabled.
TxQ3PKT	32	Total number of good packets transmitted on COS3, which is specified in MIB queue select register when QoS is enabled.
TxQ4PKT	32	Total number of good packets transmitted on COS4, which is specified in MIB queue select register when QoS is enabled.
TxQ5PKT	32	Total number of good packets transmitted on COS5, which is specified in MIB queue select register when QoS is enabled.

Table 14: Transmit MIB Counters (Continued)

Transmit Counter	Width	Description
TxQ6PKT	32	Total number of good packets transmitted on COS6, which is specified in MIB queue select register when QoS is enabled.
TxQ7PKT	32	Total number of good packets transmitted on COS7, which is specified in MIB queue select register when QoS is enabled.
TxPkts64Octets	32	Number of transmitted packets (including error packets) that are 64 bytes long.
TxPkts65to127Octets	32	Number of transmitted packets (including error packets) that are between 65 and 127 bytes long.
TxPkts128to255Octets	32	Number of transmitted packets (including error packets) that are between 128 and 255 bytes long.
TxPkts256to511Octets	32	Number of transmitted packets (including error packets) that are between 256 and 511 bytes long.
TxPkts512to1023Octets	32	Number of transmitted packets (including error packets) that are between 512 and 1023 bytes long.
TxPkts1024toMaxPktOctets	32	Number of transmitted packets that (include error packets) are between 1024 and the standard maximum packet size inclusive.

1.5.6 Integrated High-Performance Memory

The BCM53154/BCM53156/BCM53158 embeds a high-performance SRAM for storing packet data and associated metadata.

The integrated memory is 1 MB and can be flexibly partitioned into a packet buffer region, and a region available to the M7/8051 for instruction/data memory as well as storage for packets forwarded to the CPU (UM mode is restricted by OTP to only 128 KB of the 1 MB of memory). The BCM53154/BCM53156/BCM53158 M7 processor also has 32 KB ITCM, 64 KB DCTM, 16 KB I-Cache, and 16 KB D-Cache.

In addition, instead of the IVM and EMV, the following tables exist:

- Logical Interface Mapper (LIM): 2K entry hash table to support virtual ports and double-tagged frames, and so forth.
- VSI Tag Control (VTC): 4K entry with per port controls for egress edits

This eliminates the need for external memory and allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves nonblocking performance for stand-alone 8-port applications and for applications with up to 15 ports and 33 Gb/s throughput.

1.5.7 Robo 2 Switch Core

The core of the BCM53154/BCM53156/BCM53158 devices is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queuing.

1.5.7.1 Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

1.5.7.2 Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully nonblocking solution.

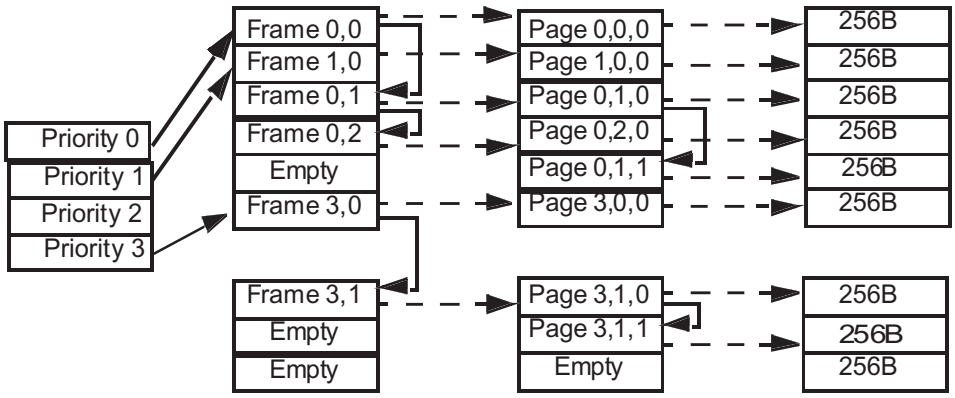
1.5.7.3 Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see Figure 3). The first level is the TXQ linked list, and the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame TC order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to eight transmit queues for servicing Quality of Service (QoS). All eight transmit queues share the all entries of the TXQ table. The TXQ table is maintained as a linked list, and each node in the TXQ uses one entry in the TXQ table.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 9720-byte jumbo frame requires 38 buffer tags for handling the frame.

Figure 3: TXQ and Buffer Tag Structure



1.6 Notational Conventions

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active low (such as CE).
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m (such as [7:0] indicates bits 7 through 0, inclusive).
- The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage (for example, 1 KB means 1,024 bytes, 100 Mb/s [referring to fast Ethernet speed] means 100,000,000 b/s, and 133 MHz means 133,000,000 Hz).

Chapter 2: Features and Operation

2.1 Overview

The BCM53154/BCM53156/BCM53158 switches include the following features:

The following sections discuss each feature in more detail.

2.2 ARM Cortex-M7 Core

The BCM53154/BCM53156/BCM53158 integrates a low-power and high-performance ARM Cortex-M7 processor core with a clock speed of up to 400 MHz. The ARM Cortex-M7 core includes integrated 16 KB two-way set-associative I-Cache and 16 KB four-way set-associative D-Cache. The BCM53154/BCM53156/BCM53158 also supports a 32 KB ITCM and 64 KB DTCM.

2.3 Quality of Service and Scheduling

The Quality of Service (QoS) feature provides up to eight internal queues per port to support eight different traffic classes (TCs). Traffic class is an internal representation of priority of an incoming packet inside the device. The traffic class assignment can be programmed so that the user can assign incoming packets to higher/lower TC priorities through TC Mapping. Then, each TC is mapped to one of eight internal class-of-service (CoS) egress queues through TC-to-CoS process. Packets assigned (mapped) to a higher priority output queue in the switch experience less delay than packets with a lower priority under congested conditions. This can be important in minimizing latency for delay-sensitive traffic.

In UM+ and MM, the TC/DP mapping takes a hierarchy in the following descending order:

- Direct instruction – via IMP or Cascade header
- CFP output – flow processing
- SLI Context TCAM match with TC and/or DP override
- This is typically reserved for traffic to the IMP/CP
- TC resolution logic based on mapping a field from packet header – for example, {PCP,DEI} --> TC, DP
- Port default

The DP value encodes three colors:

- GREEN for low drop
- YELLOW for medium drop
- RED for high drop

The rate limiter may be *color-blind* or *color-aware*. Its output DP value, together with the TC, is used to derive PCP and DSCP remarking at the egress. The final PCP and DSCP may encode the *color* of the egress packet per the trTCM scheme (see RFC 2698 and RFC 4115, Section 11).

2.3.1 TC2CoS Mapping

All packets should be configured to be mapped to appropriate TCs, and those TCs should be mapped to appropriate egress queues through the Destination Physical Port and Traffic Class to Queue (TC2QD) table. This allows unique mapping of TC to queue for each port, including the IMP and internal CPU ports.

A packet may be sent to the CPU through the IMP (any port can be an IMP port) or the dedicated internal CPU port. Each event that results in sending a packet to the CPU can be mapped to a specific queue and will include an exception ID indicating the reason why the packet is sent to the CPU.

NOTE: In addition to determining the CPU queue in nonaggregation mode, the exception ID may also help software process the packet in all modes.

2.3.2 Egress Queues and Scheduler

2.3.2.1 Egress Transmit Queues

Each Ethernet egress port has eight transmit queues (CoS0–CoS7), and the depth of each queue is configurable. Each CoS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purposes. Every Ethernet (ingress) port has its own set of counters to measure the buffer occupancy and the arrival rate related to the traffic received from the port.

2.3.2.2 Two-Level Scheduler

The scheduling element can be configured to be one of the following operating modes:

- Priority Queuing (PQ) or Strict Priority (SP)
- Weighted Round Robin (WRR): packet-based scheduling
- Weighted Deficit Round Robin (WDRR): byte-based scheduling
- Round-Robin Queuing (RRQ)
- AVB as well as Time-Aware Scheduling per TSN

2.3.3 Shaper

BCM53154/BCM53156/BCM53158 supports a per-queue bandwidth and packet shaper. The shaper can limit the amount of bandwidth consumed and the number of packets sent to the management processor.

2.4 AutoDOS/AutoVOIP/Auto LoopDetect

The BCM53154/BCM53156/BCM53158 software includes a set of "Auto" features that are activated upon switch activation and do not require any post power-up configuration to operate properly. This set includes the following three features: AutoDOS, AutoVoIP, and AutoLoopDetect. These features are important when the switch is in unmanaged ('U') mode and the user still requires control of basic switch operation.

NOTE: Auto features requires an external flash memory.

2.4.1 AutoDOS

The AutoDOS feature detects potential DOS attacks and drops the suspected packets automatically to defeat the attack. There are several possible DOS attacks and a default set must be selected for detection and dropping in unmanaged mode. In managed mode, AutoDOS is a feature, but the types of attacks to detect and drop are programmable. A packet which will be dropped may still be mirrored, but will not be forwarded.

Table 15 describes the DOS attacks that are detected and may be selected for packet dropping. Two columns have been added to indicate which are detected by the ROBO and Voyager and to show what is supported by the CB.

Table 15: DOS Attack Control

DOS Type	Description	Supported in the BCM53154/ BCM53156/BCM53158?
MAC_LAND	MACDA=MADSA in an Ethernet packet.	Yes
IP_LAND	IPDA=IPSA in an IP (v4/v6) datagram.	Yes
TCP_BLAT	DPort=SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
UDP_BLAT	DPort=SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
TCP_NULLScan	Seq_Num=0 and **All** TCP_FLAGs=0, in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
TCP_XMASScan	Seq_Num= 0 and FIN=1 and URG=1 and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
TCP_SYNFINScan	SYN=1 and FIN=1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
TCP_SYNError	SYN=1 and ACK=0 and SRC_Port<1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.	Yes
TCP_ShortHDR	The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size.	Yes
TCP_FragError	The Fragment_Offset=1 in any fragment of a fragmented IP datagram carrying part of TCP data.	Yes
ICMPv4_Fragment	The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram.	Yes
ICMPv6_Fragment	The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram.	Yes
ICMPv4_LongPing	The ICMPv4 Ping (Echo Request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header.	Yes
ICMPv6_LongPing	The ICMPv6 Ping (Echo Request) protocol data unit carried in an unfragmented IPv6 datagram with its Payload Length indicating a value greater than the MAX_ICMPv6_Size.	Yes

2.4.2 AutoVOIP

The AutoVOIP feature detects VoIP streams and designates them as a high priority, that is, marking the frames' p-bits with a high-priority value. The purpose is to provide better quality of service for VoIP traffic which is sensitive to lower qualities of service. When talking on a VoIP phone, a user expects to have no interruptions in the conversation and excellent voice quality. The BCM53154/BCM53156/BCM53158 recognizes VoIP packets based on the MAC OUI field of arriving frames (OUI = highest 24 bits of the MAC address). Those MAC OUIs are associated with known VoIP vendors like Cisco, Avaya, 3COM, and others.

Table 16 presents the VoIP vendor OUIs that are detected by the AutoVoIP feature.

Table 16: VoIP Vendor OUI

Vendor Name	Vendor OUI
Siemens_ag_phone	
Avaya	00:04:0D
Cisco	00:03:6B
3COM	00:E0:BB
Polycom	00:E0:75
Pingtel	00:D0:1E
Alcatel	00:80:9F
Nortel	00:13:65 00:16:CA
Aastra	00:08:5D
Intertel	00:10:36
Shoretel	00:10:49
Giant	00:09:6E
Adtran	00:A0:C8
Moimstone	00:11:A9
Teledex	00:0A:06
TCL	00:0E:1F
Wistron	00:16:D3
H3C	00:0F:E2
Tecom	00:03:C9 00:19:15
Fujitsu	00:0B:5D
NEC	00:60:B9
Hitachi	00:00:87

2.4.3 AutoLoopDetect

This feature detects a loop in the network, but does not prevent it like spanning tree. The purpose is to provide an indication (usually via LED) that a loop exists in the network so that a network administrator can clearly see it and eliminate it using manual means (not protocol). AutoLoopDetect transmits periodically a loop discovery frame (timer triggered) which is a broadcast frame with a Broadcom specific header (includes a loop discovery opcode). The loop discovery frame also has an ID that can be used to determine the frame's source. If a port receives a loop discovery frame from itself, a loop condition in the network is discovered and the LED on the corresponding port is set.

AutoLoopDetect uses the BCM53154/BCM53156/BCM53158 uC8051 controller to generate the relevant frames. When the frame returns, the IPP Tag-Parser detects it and forwards it to the uC8051. Identifying the packet and sending it to the uC8051 can be implemented as a trap in the SLIC TCAM. Instead of dropping the trapped packet, it will be forwarded by the trap to the uC8051.

2.5 VLAN Filter

The virtual LAN (VLAN) filter feature partitions the switching ports into virtual private domains designated on a per-port basis. Data switching outside of the port's private domain is not allowed. The BCM53154/BCM53156/BCM53158 provide flexible VLAN configuration for each ingress (receiving) port.

The VLAN filter feature works as a filter, filtering out traffic destined to non-private domain ports. For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame will be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the non-private domain ports. The frame is forwarded only to those ports that meet the ARL table criteria, as well as the VLAN filter criteria.

2.6 Private VLAN

The private VLAN feature, also known as port isolation, enables the creation of isolation groups that restrict forwarding among the ports that are members of the group. The BCM53154/BCM53156/BCM53158 supports four private VLAN groups.

2.7 IEEE 802.1Q VLAN

The BCM53154/BCM53156/BCM53158 supports IEEE 802.1Q VLANs and Port VLAN to Logical Interface (PV2LI) to support the full 4096 table entries. that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM53154/BCM53156/BCM53158 autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups.

2.7.1 VSI/VLAN Table (PV2LI)

The BCM53154/BCM53156/BCM53158 provides a dedicated, efficient method. A 4K entry {port,vid} to the LI table (PV2LI) is used. This table supports the full 4K VLAN name-space. PV2LI does not support VLAN translation or Virtual Ports as the received VID is used directly to assign the VSI, that is, all members of a VSI using the PV2LI table must share the same VID or be natively tagged. Native tagging refers to untagged frames where the CVID is inferred-based on the receive port.

2.8 Double-Tagging

The BCM53154/BCM53156/BCM53158 provide the double tagging feature, which is useful for ISP applications. When the ISP aggregates incoming traffic from each individual customer, the extra tag (double tag) can provide an additional layer of tagging to the existing IEEE 802.1Q VLAN. The ISP tag (extra tag) is a way of separating individual customers from other customers. Using the IEEE 802.1Q VLAN tag, the individual customer's traffic can be identified on a per-port basis.

2.9 Jumbo Frame Support

The BCM53154/BCM53156/BCM53158 can receive and transmit frames of extended length on ports linked at Gigabit speed. Referred to as jumbo frames, these packets are longer than the standard maximum size, but shorter than 9728 bytes. Jumbo packets can be received or forwarded to 1000BASE-T, 2.5G, and 10G linked ports that are jumbo-frame enabled. Up to 38 buffer memory pages are required for storing and the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo enabled, it is recommended that no more than two be enabled simultaneously to ensure system performance. There is no performance penalty for enabling additional jumbo ports beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

2.10 Port Trunking

The BCM53154/BCM53156/BCM53158 supports up to 32 trunks and total 32 ports (in two cascaded BCM53154/BCM53156/BCM53158 devices). The grouping of links is flexible and configurable, even across two cascaded BCM53154/BCM53156/BCM53158 devices. Each group supports automatic failover and can contain up to 32 links per group

The distribution can be based on a hash of DA, SA, or DA + SA; it is a programmable feature.

- MAC-DA (default)
- MAC-SA
- MAC-DA + MAC-SA (+VSI)

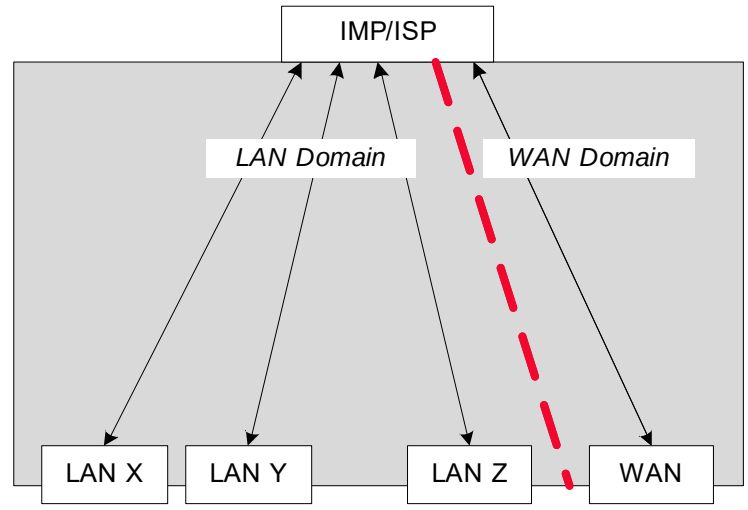
Additional fields may be added to the hash, including L3 and L4 fields.

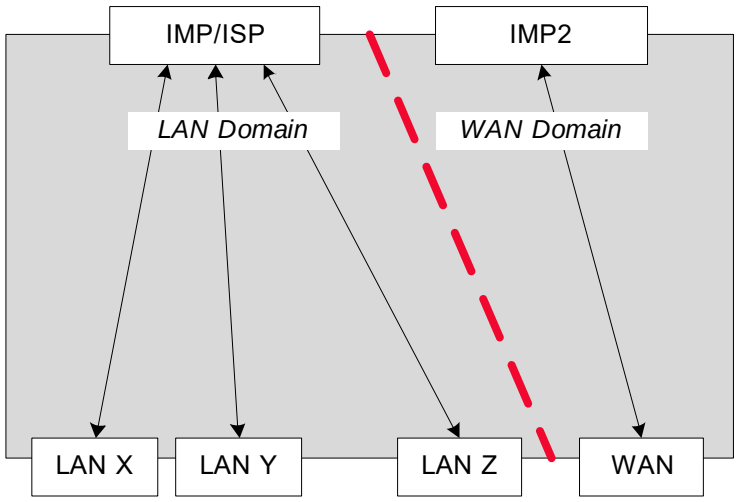
2.11 WAN Port

The BCM53154/BCM53156/BCM53158 offers a programmable WAN port feature: It has a WAN Port Select register. Select a port as a WAN port, then all that port's traffic is forwarded to the CPU port only. The non-WAN port traffic from all other local ports does not flood to the WAN port.

Figure 4 shows the WAN and LAN domain separation when the WAN port is selected.

Figure 4: WAN and LAN Domain Separation





2.12 Ingress Rate Limiters

2.12.1 Ingress Traffic Management

The BCM53154/BCM53156/BCM53158 supports flexible and hierarchical profile-based rate limiting (policer or shaper) and marking schemes. The BCM53154/BCM53156/BCM53158 adopts a hierarchical design.

2.12.2 Per-Flow Rate Limiting

The BCM53154/BCM53156/BCM53158 identifies traffic flows for ACLs, rate limiting, counting, flow-based packet modification, and forwarding override. Total 1K flows are supported. Each flow may be associated with a meter where users may limit the receiving rate (byte rate or packet count).

2.12.3 Flow Control

The BCM53154/BCM53156/BCM53158 supports the flow control feature. When a packet is dropped or marked as red, flow control to the ingress port may be activated.

- For Unmanaged (UM) and Unmanaged+ (UM+) switches, only IEEE 802.1x pause frames are supported.
- For managed switches, IEEE 802.1Qbb PFC is further supported on all ports.

2.13 Protected Ports

Protected Ports is the Private VLAN (Isolation Groups) feature and allows certain ports to be designated as protected. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. Several applications that can benefit from protected ports:

- Aggregator: For example, all the available ports are designated as protected ports except a single aggregator port. No traffic incoming to the protected ports is sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent nonsecured ports from monitoring important information on a server port, the server port and nonsecured ports are designated as protected. The nonsecured ports will not be able to receive traffic from the server port.

2.14 Port Mirroring

The BCM53154/BCM53156/BCM53158 supports port mirroring, allowing ingress and/or egress traffic to be monitored by sending a copy of the traffic to a designated port. The BCM53154/BCM53156/BCM53158 can be configured to mirror ingress traffic on a port, VLAN, or flow basis. Mirroring multiple ports is possible but can create congestion at the mirror capture port. Several filters are used to decrease congestion. Up to 64 mirrors may be configured.

2.15 IGMP Snooping

The BCM53154/BCM53156/BCM53158 supports IP-layer IGMP Snooping which includes IGMP unknown, query, report and leave messages.

A frame with a value of 2 in the IP header protocol field and IGMP frames are forwarded to the CPU port. The management CPU can then determine from the IGMP control packets which port should participate in the multigroup session. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. IGMP frames will be trapped only to the CPU port if one of the following is enabled:

- Blocked
- Forwarded normally
- Send to CPU
- Forward and copy to CPU

2.16 MLD Snooping

The BCM53154/BCM53156/BCM53158 supports IP-layer MLD Snooping and includes MLD query, report, and done messages. For the each of query and report/done message types, there are four options available: discard, forward normally, forward to CPU, or forward normally and copy to CPU. The CPU is then expected to interpret these messages and configure the address table accordingly.

2.17 IEEE 802.1X Port-Based Security

IEEE 802.1X is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM53154/BCM53156/BCM53158 detects EAPOL frames by checking the destination address of the frame. The Destination addresses should be either a multicast address as defined in IEEE 802.1X (01-80-C2-00-00-03) or a user-predefined MAC (unicast or multicast) address. Once EAPOL frames are detected, the frames are forwarded to the CPU so it can send the frames to the authenticator server. Eventually, the CPU determines whether the requestor is qualified or not based on its MAC_Source addresses, and frames are either accepted or dropped. The per-port EAP can be programmed in the register.

BCM53154/BCM53156/BCM53158 provides three modes for implementing the IEEE 802.1X feature. Each mode can be selected by setting the appropriate bits in the register.

The Basic Mode (when EAP Mode = 00'b) is the standard mode, the EAP_BLK_MODE bit would be set before authentication to block all of the incoming packets, upon authentication, the EAP_BLK_MODE bit would be cleared to allow all the incoming packets. In this mode, the Source Address of incoming packets is not checked.

The second mode is Extended Mode (when EAP Mode = 10'b), where an extra filtering mechanism is implemented after the port is authenticated. If the Source MAC address is unknown, the incoming packets would be dropped and the unknown SA would not be learned. However if the incoming packet is IEEE 802.1X packet, or special frames, the incoming packets will be forwarded. The definition of the Unknown SA in this case is when the switch cannot match the incoming Source MAC address to any of the addresses in ARL table, or the incoming Source MAC address matches the address in ARL table, but the port number is mismatched. The third mode is Simplified Mode (when EAP Mode = 11'b). In this mode, the unknown Source MAC address packets would be forwarded to CPU rather than dropped. Otherwise, it is same as the Extended Mode operation.

NOTE: The BCM53154/BCM53156/BCM53158 checks only the destination addresses to qualify EAPOL frames. Ethernet type fields, packet type fields, or non-IEEE 802.1Q frames are not checked.

2.18 DoS Attack Prevention

The BCM53154/BCM53156/BCM53158 supports the detection of the following DoS (Denial of Service) attack types based on the register setting, which can be programmed as a filter for each type of DoS packet respectively.

Each filter supports:

- Drop
- Forward as usual
- Send to CPU with an exception ID
- Forward and copy to CPU

Table 17: DoS Attacks Detected by BCM53154/BCM53156/BCM53158

DoS Attack Type	Description
IPV4_SHORT_FRAGMENT	(MF) bit set to one and has a Total Length field less than the amount specified in the Short_Frag_Config register. AKA Teardrop.
IIPV4_MCAST_SA	(SA[31:28]=14 or SA=255.255.255.255).
IPV4_BCAST_DA	(DA=255.255.255.255).
IPV4_DA_ZERO	IPv4 Source Address is multicast (DA[31:28] = 0x0) 0.0.0.0/8
IPV4_LOOPBACK	IPv4 SA or DA is loopback (127.0.0.0/8)
PV4_DA_EQ_SA	IPv4 SA == DA
IPV4_NONAT	The IPv4 header's SA and DA are not in the same address space where an address space is one of the private address spaces (10.0.0.0/8, 172.16.0.0/12, 192.168.0.0/16) or the public address space.
IPV4_PRIVATE	DA or SA is 10.0.0.0/8, 172.16.0.0/ 12, or 192.168.0.0./16
IPV4_TCP_HDR_REWRITE	IPv4 Protocol is TCP (0x6) and IPv4 offset is 0x1 or 0x2
IPV4_ICMP_FRAGMENT	IPv4 protocol is ICMP (0x01) and offset != 0x00 || mf=1
IPV4_TTL_ZERO	IPv4_TTL is zero
IPV6_SHORT_FRAGMENT	More Fragments (MF) bit set to one and Payload Length field less than the amount specified in the Short_Frag_Config register. Teardrop.
IPV6_MCAST_SA	IPv6 SA is multicast (SA[127:120] = 0xFF)
IPV6_DA_ZERO	IPv6 DA = ::0
IPV6_DA_EQ_SA	IPv6 SA = DA
IPV6_LOOPBACK	IPv6 DA or SA is 0x0000001
IPV6_ICMP_FRAGMENT	ICMPv6 protocol data carried in a fragmented IPv6 datagram.
TCP_DP_EQ_SP	DPort = SPort in a TCP header, in an unfragmented IP datagram or the first fragment of a fragmented IP datagram
UDP_DP_EQ_SP	DPort=SPort in a UDP header, in an unfragmented IP datagram or the first fragment of a fragmented IP datagram
TCP_NULL_SCAN	Seq_Num=0 and all TCP flags=0 in a TCP header carried an unfragmented IP datagram or the first fragment of a fragmented IP datagram
TCP_XMAS_SCAN	Seq_Num=0, FIN=1, URG=1, and PSH=1 in a TCP header carried an unfragmented IP datagram or the first fragment of a fragmented IP datagram
TCP_SYN_FIN_SCAN	SYN=1 and FIN=1 in a TCP header carried an unfragmented IP datagram or the first fragment of a fragmented IP datagram
TCP_SYNC	SYN=1, ACK=0, and SRC_PORT<1024 in a TCP header carried an unfragmented IP datagram or the first fragment of a fragmented IP datagram.

Table 17: DoS Attacks Detected by BCM53154/BCM53156/BCM53158 (Continued)

DoS Attack Type	Description
TCP_HDR_LENGTH	The length of a TCP header carried in the first fragment of a fragmented IP datagram is less than a configured MIN_TCP_Header_Size. (Default set at 20B, which is the minimal length)
TCP_HDR_FRAGMENT	The first IP fragment must be large enough to contain all required TCP header. For IP packets with Fragment Offset = 0, its length must be longer than a set threshold.
ICMP4_LONG_PING	ICMPv4 Ping (Echo Request) PDU is carried in an un-fragmented IPv4 datagram whose Total Length has a value that is greater than **MAX_ICMPv4_Size** + size of IPv4 header. Where the **MAX_ICMPv4_Size** is programmable between 0 and 9.6K bytes, inclusive. The default is set to 512.
ICMP6_LONG_PING	ICMPv6 Ping (Echo Request) PDU is carried in an un-fragmented IPv6 datagram whose Payload Length has a value greater than **MAX_ICMPv6_Size,** where the **MAX_ICMPv6_Size** is programmable between 0 and 9.6K bytes, inclusive. The default is set to 512.
IPV4_SMURF	IPv4 frame to broadcast address (255.255.255.255) with protocol=ICMP OR UDP, CODE=ECHO OR DPORT=7 {SMURF, FRAGLE}
IPV6_SMURF	IPv6 frame to broadcast link local address FF02:: with protocol=ICMP OR UDP, CODE=ECHO OR DPORT=7 {SMURF, FRAGLE}

- MAX_ICMPv4_Size is programmable between 0 and 9.6 KB, inclusive.
- MAX_ICMPv6_Size is programmable between 0 and 9.6 KB, inclusive.

2.19 CFP (Compact Field Processor)

The BCM53154/BCM53156/BCM53158 includes the CFP flow processing capability as in the ROBO family of switches. The CFP module is a TCAM-based policy engine for flow classification, packet forwarding, traffic management, statistics collection, and access control. The CFP supports line-rate operation when used for ingress flow processing.

The CFP supports up to 15 flexible key formats for each of the following packet types: IPv4, IPv6, and non-IP. Up to four keys may be assembled for each packet. Two keys can be aggregated, with width expanded, to logically create a key that is twice as wide. This is done by concatenating key 0 and key 1 or by concatenating key 2 and key 3. This is supported on a key-by-key basis. That is, a single key may be double wide while all others are single wide.

Up to four rule matches can be processed per packet. Each rule that is matched may apply one or more of the 9 policy actions. The lowest rule number with a policy enabled specifies the action for that policy. Collectively, the policies are processed across all four possible matches. For example, one rule may change the forwarding destination and another rule may apply a meter.

2.19.1 Summary of CFP Features

- 1Kx192b TCAM
- Each key size is 192 + valid bits with 4 key per frame
- Key width expansion for round 0 and 1 and 2 and 3: Maximum rule widths of 190b or 380b (double wide)
- Capacity: 1K 192b rule; each 380b rule takes two entries
- Counters: 1Kx70b capacity with two modes (each rule specifies the counter mode)
  - 38b packet and 32-bit byte
  - 32b in-profile packets and 32b out-of-profile packets

Flexibly assigned 511 policy based meters

The BCM53154/BCM53156/BCM53158 supports the CFP rules to canonical policy actions shown in Table 18.

Table 18: Canonical Policy Actions

No.	Primary Policy	Description
1	Override	If set all other rule matches of higher rule number are ignored
2	Change_fwd	Specifies the destination to which the frame is forwarded
3	Meter Frame	Meter frame using associated meter
4	Change_TC	Changes TC
5	Change_DP	Changes DP
6	Mirror Frame	mirror != 0, mirror frame using mirror
7	Trap Frame	cfp_trap_id =! 0, trap frame via TGT; set trapID to cfp_trap_od+CFP_TRAP_OFFSET
8	Disable learning	Disable learning
9	DLF override	Override DLF decision

2.19.2 Parser

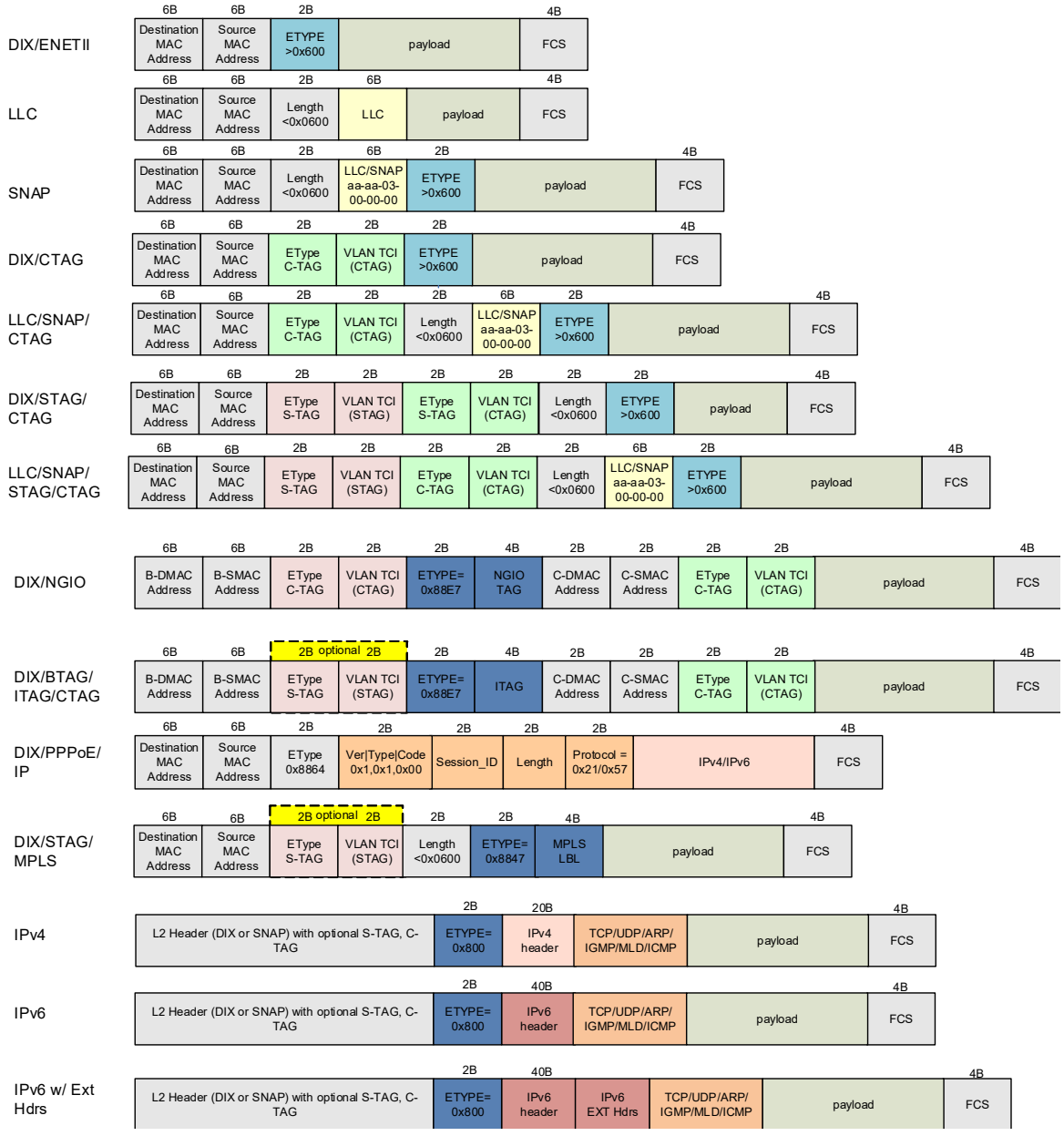
The BCM53154/BCM53156/BCM53158 ingress parser is capable of parsing a rich set of packet formats as illustrated in Figure 5 on page 51.

- L2 headers
  - LLC
  - DIX/ENTII
  - SNAP encapsulated IPv4 and IPv6
- PPo IEEE 802.1Q VLAN tags - single-tagged packets
  - IEEE 802.1ad – double tagged packets (for example, STAG and CTAG)
  - IEEE 802.1ah – MAC-in-MAC ITAGs
  - IEEE 802.1BR Port Extender tags
  - Cisco MAC-in-MAC TAG
  - Broadcom Channelization over Ethernet (CoE) tags
  - 4x User programmed L2 tags: program the 2B TPID and associated tag size
    - Tag sizes of 4B, 6B or 8B are supported
- ARP (address resolution protocol)
- MPLS – single label
- PPPoE
  - PPPOE session packets (Ethertype = 0x8864) described in RFC2516 with:
    - version=1, type=1, code=0.
    - PPP Protocol=0x21 for IPv4, or 0x57 for IPv6 with full L4 parsing support.
  - PPPoE Discovery (ET=0x8863).
- L3 IPv4 and IPv6 headers.
  - The parser extracts DSCP field which can be subsequently used to support QoS.
- 4x L3 protocols identified by user programmed Ethertype.
- IPv4
  - Mo options (fixed HL=20)
  - ICMP (1) for IPv4
  - IGMP (2) for IPv4
- IPv6
  - ICMPv6
    - MLD for snooping
    - Neighbor Discovery (ND)
  - At most one extension header that is not L4 is processed from this following list.
    - IPv6 Frag header (44)
    - Dest Options (60)
    - AH Header (51)
    - No next Header (59) – stop parsing
  - All other extension headers and not parsed and L4 protocol is unknown.
- L4 Protocols
  - TCP(6)/UDP(17) headers for IPv4 and IPv6
  - 2 programmable L4 protocols which include the first 32 bits of the payload as {Dport|Sport}
- IEEE 1588 PTP frames including event messages.

  - Both directly over Ethernet (using Ethertype) and over UDP (using destination port).
- Up to ~128 user defined header formats and/or specific addresses or protocols.
  - For example, Local MAC-DA, BPDUs, and so forth, using the SLIC TCAM.

Figure 5 on page 51 shows the packet formats parsed by the parser.

Figure 5: Packet Formats Parsed by the Parser



2.20 Multiple Spanning Tree Protocol

The BCM53154/BCM53156/BCM53158 supports up to 128 multiple spanning trees and can be configured to forward BPDU packets to the management port only.

2.21 Software Reset

The BCM53154/BCM53156/BCM53158 provides Software Resets. Software Resets can be triggered by setting the register.

NOTE: Software Reset sets all the register and the table (ARL, VLAN) contents to the default values. Software Reset will not latch in the strap pin values, but the previous latched strap pin values are retained.

2.22 1588 Time Synchronization Support

The BCM53154/BCM53156/BCM53158 supports 1588v2 for applications that require precision time synchronization among multiple operational nodes. These applications include automation and control systems, measurement and automatic test systems, power generation, transmission and distribution systems, navigation, emulation of TDM circuits in a packet-based network, and backup for other time sources such as loss of GPS signal.

The BCM53154/BCM53156/BCM53158 supports the following time synchronization operation:

- One-step
- Two-step

  The firmware stack participates in the handshake protocol.
- E2E (End-to-End) TC support

  The correction field in a PTP message is updated only with the residence time, that is, time for the PTP message to propagate through the switch.
- PTP (Peer-to-Peer) TC support

  The integrated Cortex-M7 processor or external CPU run PTP stack to measure link delay between two adjacent switches. This link delay information is made aware of by the hardware such that link delay is accounted for PTP timing synchronization. Specifically, the hardware will add link delay to the correction field of a PTP message.

NOTE: The BCM53154/BCM53156/BCM53158 supports 1588 MC and BC as well as TC. In managed mode, it has full 1588v2 support.

2.23 Port Extender

The BCM53154/BCM53156/BCM53158 supports a Port Extender (PE) for centralized switch architecture. Both the Channelization of Ethernet (CoE) and IEEE 802.1BR models are supported. These two models are similar, but the BCM53154/BCM53156/BCM53158 uses *TAGs with different format* to tag packets for switching.

In generic terms, an E-channel refers to a configured connectivity path between the Controlling Bridge and the External Extended Port (data channel), and/or the Uplink ports (control channel for PEs).

2.24 Egress PCP/DEI Remarking

The BCM53154/BCM53156/BCM53158 provides an egress PCP/DEI remarking feature. Each egress port provides a mapping from TC/DP to IEEE 802.1P. These tables are used to map the internal TC/DP value to the egress PCP and DEI values for STAG and CTAG modification.

- The two tables are indexed by the internal {TC, DP} value.
- Output of the two tables are {S-PCP, S-DEI} and {C-PCP and C-DEI}, respectively.

2.25 Address Management

The BCM53154/BCM53156/BCM53158 Address Resolution Logic contains the following features:

- IVL and SVL Support
- Drop Controls
- ARL Hashing Algorithm
- ARL-based Forwarding under Unmanaged Mode (UM)
- ARL-based Forwarding under Managed Mode (UM+, UM)
- Basic Management Mode (without Virtual Ports in use)
- Advanced Managed Mode with VLAN Translation (without Virtual Ports)

2.25.1 ARLFM Table

The Address Resolution Lookup Forwarding Map (ARLFM) is the primary method for forwarding bridged packets. In the case of UM/UM+, the ARLFM key of {FID, MAC} is used for all forwarding where FID represents the VSI for Independent VLAN Learning (IVL) or a group of VSIs for Shared VLAN Learning (SVL). In other applications, different keys may be configured to forward on different fields. For example, host routes or MPLS label switching may be supporting using the IPv4 DA or the MPLS label, respectively.

The BCM53154/BCM53156/BCM53158 supports up to 8 forwarding tables. The size of the table(s) is configurable. By default, a single ARLFM table using the key {FID, MAC} is used with a size of 16K entries. FID is taken from VSI Table. The contents of the ARLFM are shown in Table 19. The table includes additional state fields that are used to support aging, creating static entries and validating the key match (that is, valid, age, and key).

Table 19: ARLFM Table Entry

1 bit	DST_IS_MC	0: Unicast DLI either type N or PV 1: Multicast destination group (DG)
12 bits	Destination (DLLIID_DG)	Destination: Overlay of multicast group (DG) or destination logical interface (DLLIID). The DLLID can be type LIN or PV.
2 bits	fwd_ctrl (valid)	Control field for MAC-based security: 0'b00: Normal forwarding 0'b01: Forward per destination and copy to CP 0'b10: Drop if match is on destination lookup (deny destination) 0'b11: Drop if match on source lookup (deny source)
2 bits	Valid	0 – Empty 1 – Pending – Learned by hardware. Miss from a forwarding perspective. 2 – Valid 3 – Static – Is not aged.
1 bit	hit	Current age of entry

The option to support additional tables allows users to adapt the forwarding plane to their applications. For example, a second table may be created that uses the key {VSI, TC} to enable VLAN forwarding based on traffic class.

2.26 Power-Saving Modes

The BCM53154/BCM53156/BCM53158 offers different power savings modes for different operating states. All the power saving scheme are implemented without any external CPU requirement.

The various power savings modes are:

- **Auto Power Down mode:** This is a stand alone PHY feature which is enabled by a register bit setting. The PHY shuts off the analog portion of the circuitry when cable is not connected or the link partner power is down.
- **Energy Efficient Ethernet (EEE) mode:** Energy Efficient Ethernet is IEEE 802.1az, an extension of the IEEE 802.3 standard. IEEE defines support for the PHY to operate in Low Power Idle (LPI) mode. When enabled, this mode supports QUIET times during low link utilization, allowing the both sides of link to disable portions of each PHY's operating circuitry and save power.

NOTE: The EEE function is for the GPHY port only

2.26.1 Auto Power Down Mode

Auto Power Down mode saves PHY power consumption while the link is down. When the user enables the Auto Power Down mode through a PHY register bit setting, the PHY goes into the power savings mode automatically whenever it is in link-down state. During the Power Down state, the PHY wakes up every 2.7 or 5.4 seconds, depending on the register settings, and checks for a link signal. If no link signal is detected, then the PHY goes back to Power Down state, or the PHY wakes up and resumes the link process.

Auto Power Down mode applies to the following conditions:

1. Cable is plugged in, but the link partner is shut down (for example, when a PC is off), so the port is in link down state.
2. Cable is unplugged, so the port is in link down state.

2.26.2 Energy Efficient Ethernet Mode

Energy Efficient Ethernet (EEE) power savings mode saves PHY power consumption while the link is up but when extended idle periods may exist between packet traffic. In EEE power savings mode PHY power consumption is scalable to the actual bandwidth utilization. The PHY can go in to Quiet mode (low-power idle mode) when there is no data to be transmitted. This feature is based on the latest IEEE 802.3az standard. The EEE supporting capability of the link partner is a must for this feature to work, and the discovery of the capability is during auto-negotiation through Link Layer Discovery Protocol (LLDP). This EEE feature is an embedded PHY feature and no external CPU is required.

In this mode, the MAC determines when to enter low power mode by examining the state of the transmit queues associated with each MAC. Four simple adjustments (settings) are used to trigger (optimize) the behavior of EEE control policy. These adjustments are:

- Two-part sleep delay timer
- Minimum low-power idle duration timer
- Wake transition timer

The two-way communication between the PHY and its link partner is required for the PHY to achieve the power savings on both sides. The transmit PHY sends a sleep symbol to the link partner, and the link partner enters low power state. When the transmit PHY sends a wake symbol, the regular packet transfer mode resumes.

2.27 VLAN Translation

The BCM53154/BCM53156/BCM53158 supports VLAN translation (VT) for broadband MDU/MTU applications. VLAN translation refers to a technology that modifies VLAN tags to isolate subscriber traffics and distinguish services. It is a MM switch feature, and there can be many modes:

- Single-tagged 1:1 VLAN mapping. The outer VID of a frame is mapped to a new VID. Each VID is mapped to a different VID. (Isolate Subscribers)
- Single-tagged N:1 VLAN mapping. The outer VID is mapped to a new VID. Multiple VIDs are mapped to the same VID. (Service VLAN)
- Double-tagged 2:2 VLAN mapping. The outer and inner VID are mapped to new outer and inner VID. (Access/Aggregation)
- Double-tagged 1:1 VLAN mapping. The outer VID is mapped to a new outer VID. The inner VLAN ID remains unchanged. (Access/Aggregation)
- Double-tagged N:1 VLAN mapping: The outer VID is mapped to a new outer VID. The inner VID remains unchanged. An outer VID or a segment of VID of a frame can be mapped to a new outer VID. The inner VID remains unchanged.

2.28 Watch Dog

The BCM53154/BCM53156/BCM53158 supports watch dog timer functionality. Detailed information on features and usage are provided in the Programmer Reference Guide (Robo2-RoboOS-PG13x).

Chapter 3: Applications and Configuration

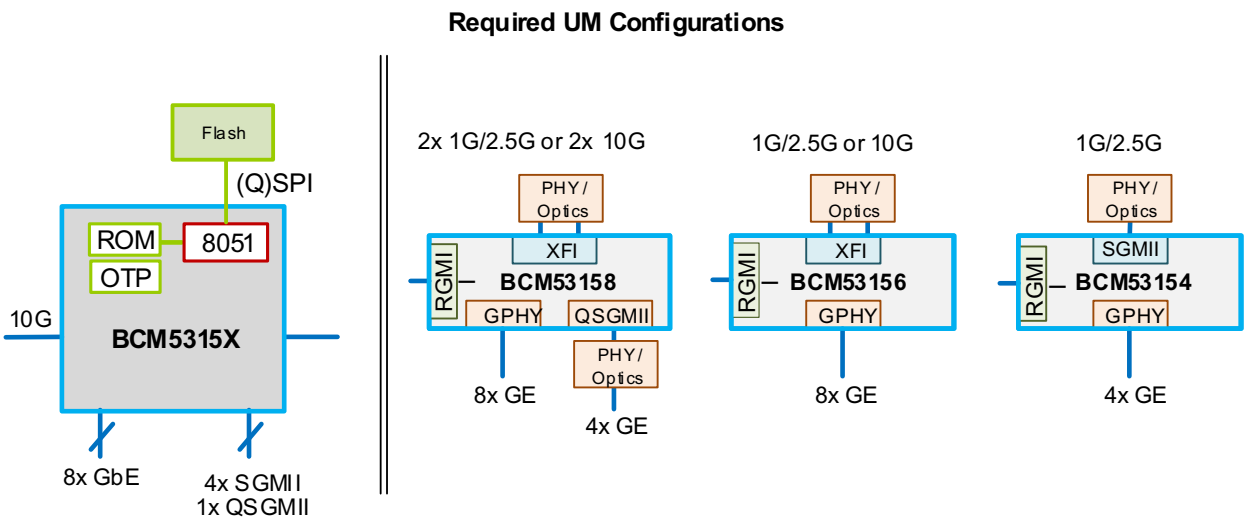
3.1 Overview

The BCM53154/BCM53156/BCM53158 supports unmanaged, web managed, and fully managed modes of operation. Each of these modes is discussed in more detail in the following sections.

3.2 Unmanaged Applications (UM)

UM operation is an out-of-box operation. When power is applied to the box, it will initialize and forward frames without any other configuration or external interaction. This configuration uses the integrated M7 CPU. The device automatically forwards frames after power is applied. The configuration of the system is static and completely contained within the Flash. Figure 6 provides an overview of the SKUs supported.

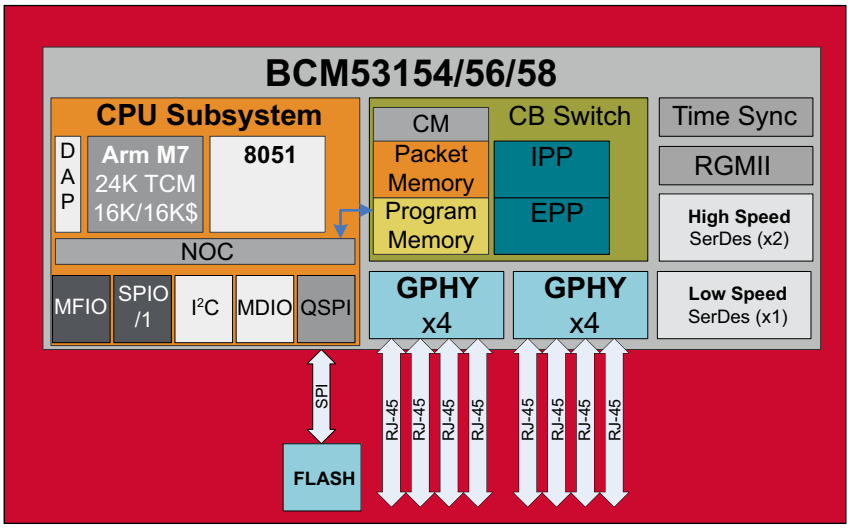
Figure 6: Unmanaged Applications



3.2.1 Unmanaged Base Configuration

The basic unmanaged configuration is the simplest possible application for BCM53154/BCM53156/BCM53158. In this case, only the internal PHY are used (8x1G). Figure 7 depicts the unmanaged base configuration.

Figure 7: Basic Unmanaged Configuration



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

The operational processors are the internal 8051 and integrated M7 CPU. The 8051 recognizes OTP and activates the M7. AVS and the rest of the Unmanaged software is running on the M7. An external Flash is required for AVS and is also used for optional customer configuration or bug fixes. Table 20 shows the valid straps and OTP in this configuration.

Table 20: Basic Unmanaged OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Enabled (off)	M7_Boot_src	M7 Flash
QSMII Disabled	Enabled (off)	Enable_qspi	Disable
ARL Size	8K Entries	Cascading_config	Stand-alone, hardware forwarding.
LIM Disable	Enabled (off)	–	–
CFP Disable	Enabled (off)	–	–
Robo 2 Switch Buffer Size[a]	512-8K PB, 8 KB 8051	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs for UM mode are restricted by the OTP to only 128 KB of the 1 MB of memory.

The embedded 8051 is responsible for the following features in this mode:

- Processing of straps and OTP configurations (ROM CODE)
- 8051 enters sleep mode and periodically runs link scan and error code (ROM CODE)

The integrated M7 CPU is responsible for the following features in this mode:

- AVS mechanism running (M7 Flash code)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Enabling internal PHYs (M7 Flash code)
- Enable forwarding (ROM CODE)
- Periodically runs link scan and error code (M7 Flash code)

3.2.2 Unmanaged with Advanced Features

The unmanaged applications have four value added features: AutoVOIP, AutoDOS, AutoQoS, and AutoLoopDetect. These four features require an external SPI flash to hold the configuration and program data for the integrated M7 CPU. The following is a list of functions performed:

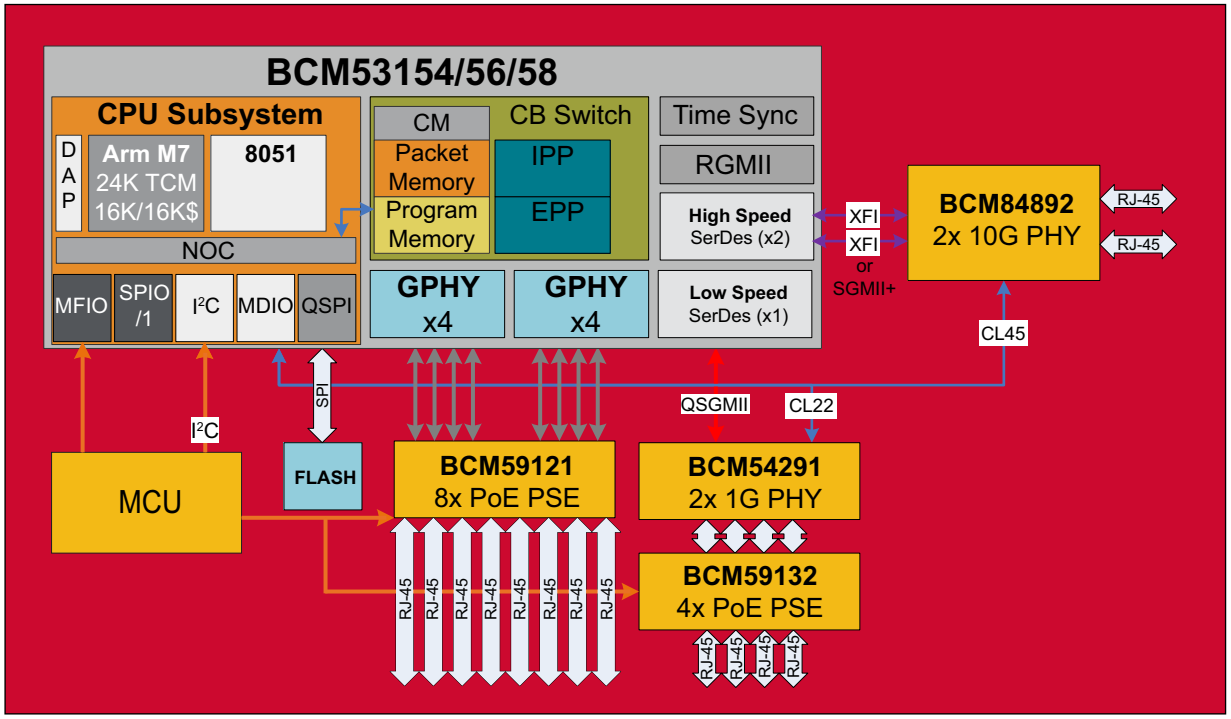
- Processing of straps and OTP configurations (ROM CODE)
- AVS mechanism running (M7 Flash code)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Enabling AutoVOIP, AutoDOS, and AutoQoS configuration (M7 Flash code)
- Enabling internal PHYs (M7 Flash Code)
- Enable forwarding (M7 Flash Code)
- Vectoring (executing from flash) to AutoLoopDetect Application Code or enters sleep mode (M7 Flash code)
- Periodically runs link scan and error code (ROM CODE)

3.2.3 High-Speed Unmanaged

The internal SerDes or external devices (PHY, PSE, and so forth) require additional code space and complexity. Figure 8 on page 60 provides a sample configuration of this application with external PSE, 10G, and 1G copper PHYs.

NOTE: It is recommended to use the indirect access mode for a PoE solution (included MCU configuration) to get the latest maintenance and compliance test guarantee. This applies to the following figures in this section.

Figure 8: High-Speed Unmanaged



NOTE: It is recommended to use the indirect access mode for a PoE solution (included MCU configuration) to get the latest maintenance and compliance test guarantee.

Table 21 describes the values for the valid OTP and strap settings.

NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 21: High-Speed Unmanaged OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	M7_Boot_src	M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Stand-alone, hardware forwarding.
LIM Disable	Enabled (off)	–	–
CFP Disable	Enabled (off)	–	–
Robo 2 Switch Buffer Size[a]	1 MB-8K PB, 8 KB 8051	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs for UM mode are restricted by the OTP to only 128 KB of the 1 MB of memory.

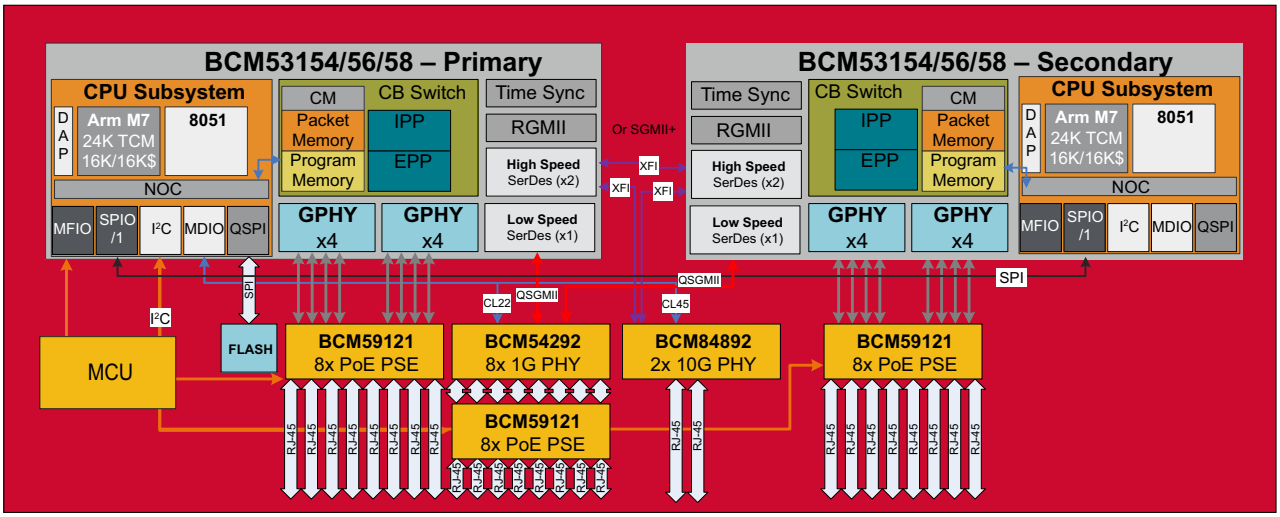
In this mode, the advanced 'auto' features are also available. The M7 flash code in this case implements the following features:

- Processing of straps and OTP configurations (ROM CODE)
- Basic unmanaged configuration of the switch core (M7 Flash CODE)
- Configuration of the internal SerDes (M7 Flash Code)
- Configuration of external PHYs, PSE, and so forth (M7 Flash Code)
- Enabling AutoVOIP, AutoDoS, AutoQoS, AutoLoopDetect configuration (M7 Flash Code)
- Play out customer specific configuration from to both internal and external devices (I^2C, MDIO) (M7 Flash Code)
- Enabling internal PHYs (M7 Flash Code)
- Enable forwarding (M7 Flash Code)
- Vectoring (executing from Flash XIP) to AutoLoopDetect Application Code or enters sleep mode (M7 Flash Code)
- Periodically runs link scan and error code (ROM CODE)

3.2.4 Unmanaged Cascade Support

In this application, two BCM53154/BCM53156/BCM53158 are connected together to provide more ports to the system. There are two different configurations shown. Figure 9 shows the first, which is a blocking configuration that provides 24x1G port with 2x10G external ports.

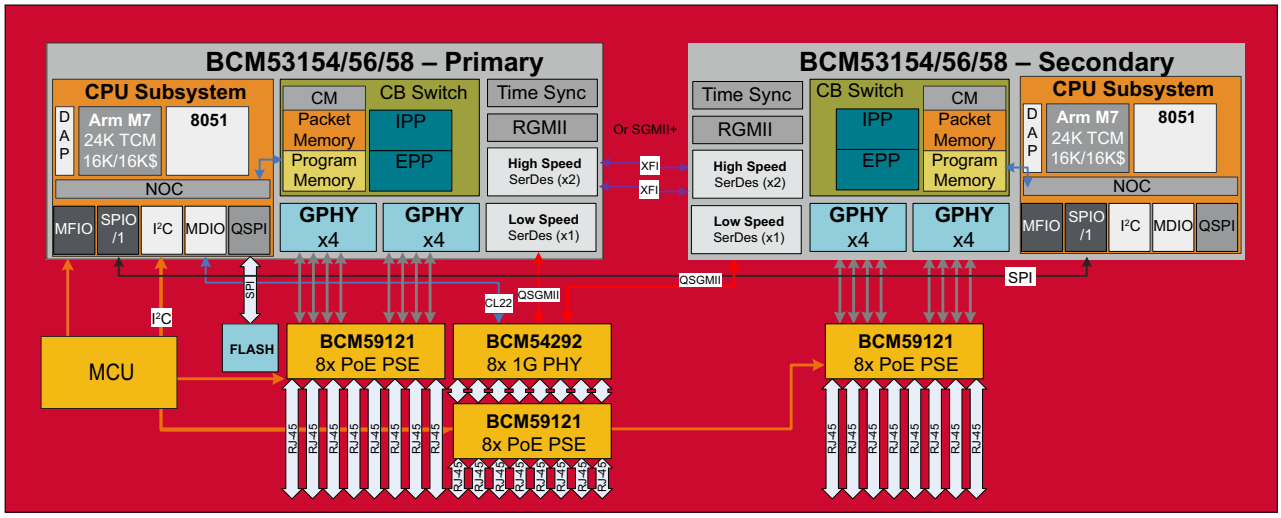
Figure 9: Unmanaged Cascade 24+2 Blocking



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Figure 10 on page 62 has a similar configuration, except a LAG is used across the 10G interface between two BCM53154/BCM53156/BCM53158 to achieve non-blocking operation.

Figure 10: Unmanaged Nonblocking 24G Solution



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 22 describes the values for the valid OTP and strap settings.

Table 22: High-Speed Unmanaged OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Primary vs Secondary
LIM Disable	Enabled (off)	–	–
CFP Disable	Enabled (off)	–	–
Robo 2 Switch Buffer Size[a]	1 MB-8K PB, 8 KB 8051	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs for UM mode are restricted by the OTP to only 128 KB of the 1 MB of memory.

In this mode, the advanced 'auto' features are also available. In this system, there are two BCM53154/BCM53156/BCM53158 where one is the primary and one is the secondary based on a strapping. The primary BCM53154/BCM53156/BCM53158 is responsible for configuring both devices. These devices are connected with an SPI interface. The hardware supports memory mapping model across this interface to facilitate using the same drivers for local and remote devices. External devices, such as PHYS and PSE are connected to the Primary BCM53154/BCM53156/BCM53158.

The M7 Flash code on the primary BCM53154/BCM53156/BCM53158 implements the following features:

- Processing of straps and OTP configurations (ROM CODE)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Configuration of the SerDes on Primary (M7 Flash code)
- Configuration of cascade on Primary (M7 Flash code)
- Configuration of the SerDes on Secondary (M7 Flash code)

- Configuration of cascade on Secondary (M7 Flash code)
- Configuration of external PHYs, PSE, and so on (M7 Flash code)
- Enabling AutoVOIP, AutoDoS, and AutoQoS configuration (M7 Flash code)
- Play out customer specific configuration from Flash to both internal and external devices (I^2C, MDIO) (M7 Flash code)
- Enable internal PHYs on Primary (M7 Flash code)
- Enable internal PHYs on Secondary this is via the MDIO on in the secondary device (M7 Flash code)
- Enable external PHYs (M7 Flash code)
- Enable forwarding on both Primary and Secondary devices (M7 Flash code)
- Vectoring (executing from flash) to AutoLoopDetect Application Code or enters sleep mode (M7 Flash code)

The M7 on the secondary BCM53154/BCM53156/BCM53158 device implements the following features:

- Processing of straps and OTP configurations (ROM CODE)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Identified as secondary based on straps (M7 Flash code)
- Does NOT enable PHYS or unmanaged forwarding (M7 Flash code)

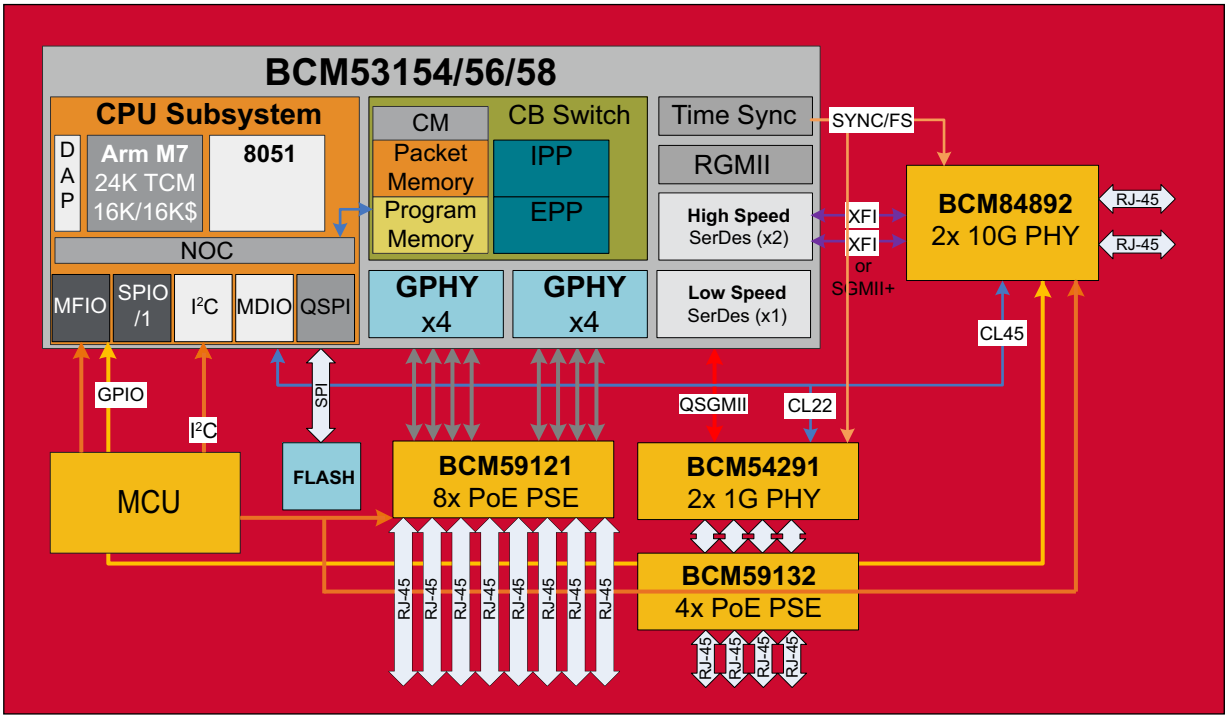
3.3 Web-Managed Application (WM)

Unmanaged+ and Web-managed are different terms used by the market to define the same set of application. These applications include advanced networking functions (that is, LAG, VLANS) which are statically configured via a web GUI interface. The M7 is the primary processor for these applications. It handles all of the necessary configuration of the device and runs the unmanaged application. All of these configurations always have Flash attached to the SPI interface. In all cases, only one CPU is connected to the internal management port. Web-managed applications can take advantage of all external interfaces (that is, I^2C.)

3.3.1 Web-Managed Stand-Alone

This configuration is stand-alone for web-managed. It requires an external SPI/QSPI flash.

Figure 11: Web-Managed Stand-Alone Configuration



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 23 describes the valid strapping and OTP in this configuration.

Table 23: Web-Managed OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Stand-alone-managed
LIM Disable	Enabled (off)	–	–
CFP Disable	Enabled (off)	–	–
Robo 2 Switch Buffer Size[a]	768 KB PB, 256 KB M7	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs have the entire 1 MB of memory enabled. The partitioning between the packet buffer and CPU regions is flexible, and under software control (not OTP control).

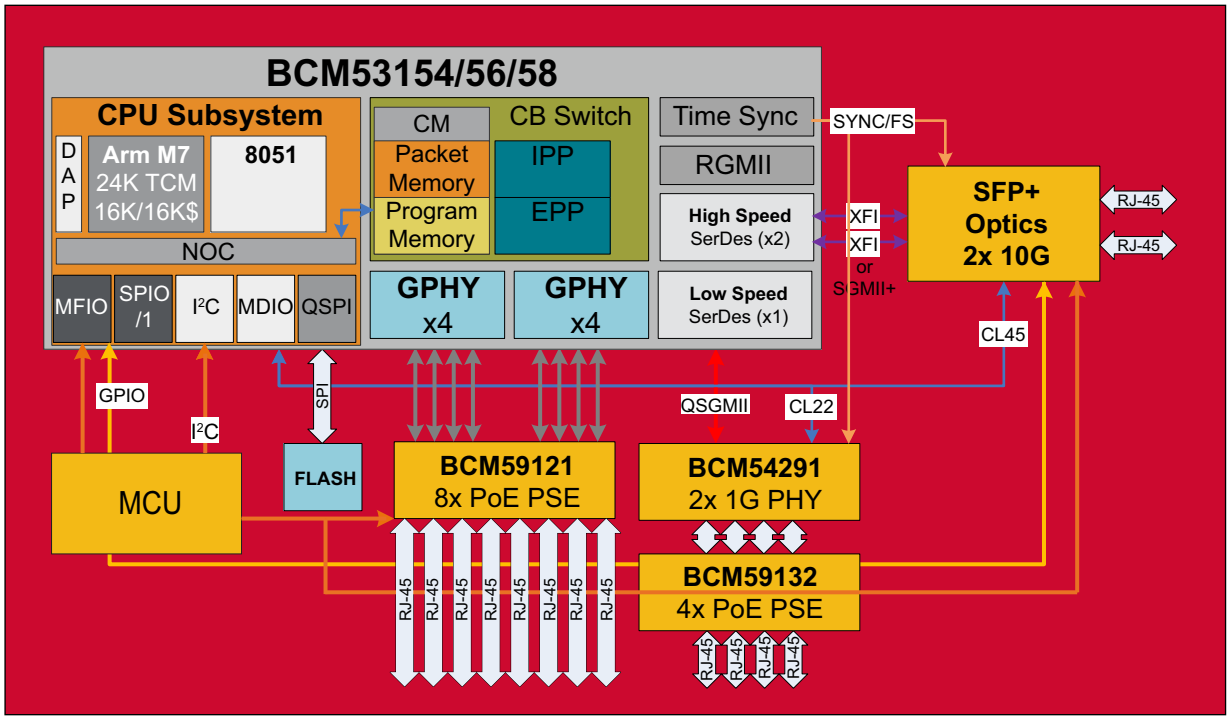
The BCM53154/BCM53156/BCM53158 initially runs the M7 Flash code which processes the following steps:

- Processing of straps and OTP configurations (ROM CODE)
- Begins executing from flash via XIP window (M7 Flash Code)
- OpenRTOS is loaded and unmanaged application (M7 Flash Code)

3.3.2 Web Managed with Optics

This configuration is the same as the stand-alone copper application except the 10G-BASE-T PHY is replaced by XFP optics. Instead of MDIO, XFP use a dedicated I^2C interfaces. In addition, a number of the MFIO pins can be used to control portions of the XFP (that is, TX_DISABLE).

Figure 12: Web-Managed with External Optics

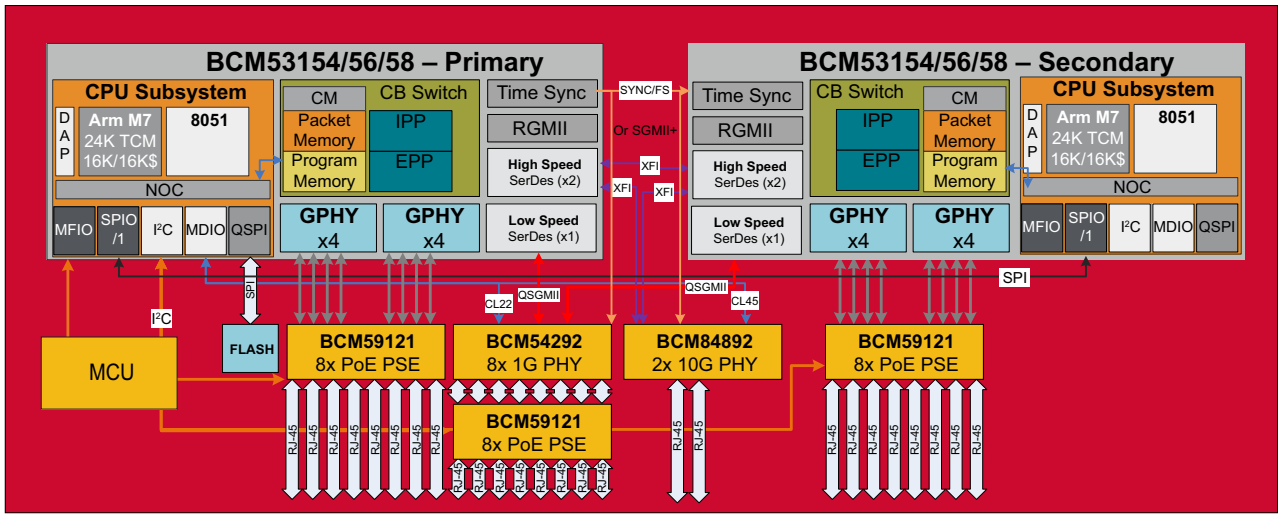


NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

3.3.3 Web-Managed Cascade

This is the configuration with two BCM53154/BCM53156/BCM53158. It is similar to unmanaged cascade configuration, except the CPUs is the M7.

Figure 13: Web-Managed Configuration with Cascading



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 24 describes the values for the valid OTP and strap settings.

Table 24: Web-Managed OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	Primary – M7 Flash Secondary – M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Primary versus Secondary
LIM Disable	Enabled (off)	–	–
CFP Disable	Enabled (off)	–	–
Robo 2 Switch Buffer Size[a]	768 KB PB, 256 KB M7	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs have the entire 1 MB of memory enabled. The partitioning between the packet buffer and CPU regions is flexible, and under software control (not OTP control).

In this system, there are two BCM53154/BCM53156/BCM53158 where is one primary and one is secondary based on a strapping. The primary BCM53154/BCM53156/BCM53158 is responsible for configuring both devices. These devices are connected with an SPI interface. The hardware supports memory mapping model across this interface to facilitate using the same drivers for local and remote devices. External devices, such as PHYS and PSE are connected to the Primary BCM53154/BCM53156/BCM53158.

The M7 Flash code on the primary BCM53154/BCM53156/BCM53158 implements the following features:

- Processing of straps and OTP configurations (ROM code)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Loads OpenRTOS
- Configuration of the SerDes on Primary (M7 Flash)
- Configuration of cascade on Primary (M7 Flash)
- Configuration of the SerDes on Secondary (M7 Flash)
- Configuration of cascade on Secondary (M7 Flash)
- Configuration of external PHYs, PSE, and so on. (M7 Flash)
- Enabling AutoVOIP, AutoDoS, and AutoQoS configuration (M7 Flash code)
- Play out customer specific configuration from QSPI Flash to both internal and external devices (I^2C, MDIO) (M7 Flash code)
- Enable internal PHYs on Primary (M7 Flash code)
- Enable internal PHYs on Secondary this is via the MDIO on in the secondary device (M7 Flash code)
- Enable external PHYs (M7 Flash code)
- Enable forwarding on both Primary and Secondary devices (M7 Flash code)

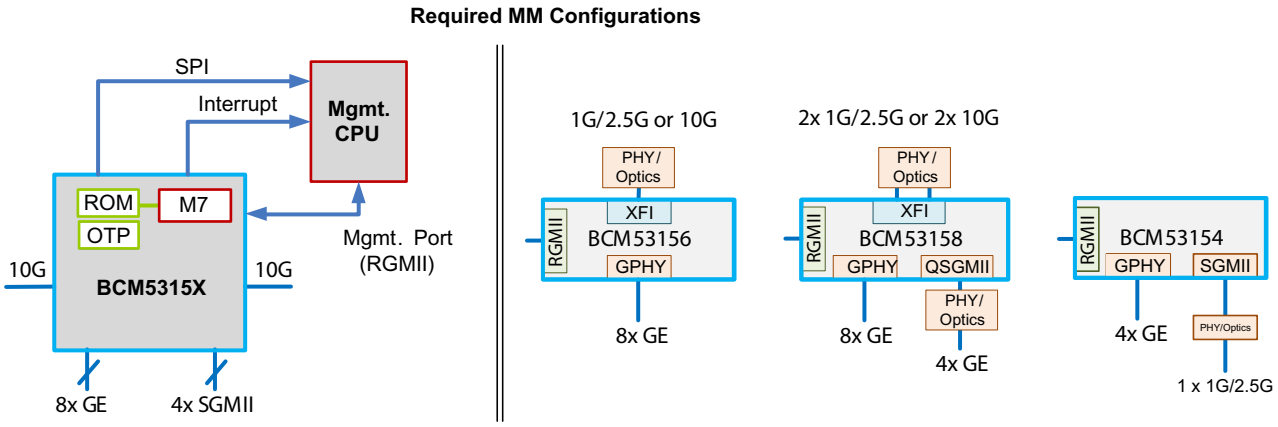
The secondary BCM53154/BCM53156/BCM53158 processes the following setups in the M7:

- Processing of straps and OTP configurations (ROM code)
- Basic unmanaged configuration of the switch core (M7 Flash code)
- Identified as secondary based on straps (M7 Flash Code)
- Does NOT enable PHYS or unmanaged forwarding (M7 Flash code)

3.4 Fully Managed Configuration

Managed Modes is used with an external CPU. There are two modes of operations: Dedicated and Hybrid. In dedicated mode, the M7 is held in reset and not used. Hybrid mode provides a cooperative mode where both the M7 and the external processor are operating. In this mode, the external processor pushes code into the internal BCM53154/BCM53156/ BCM53158 memory for execution by the M7. The external processor releases the reset to the M7. In both configurations, all configuration is via the external processor via the SPI interface.

Figure 14: Managed Configurations



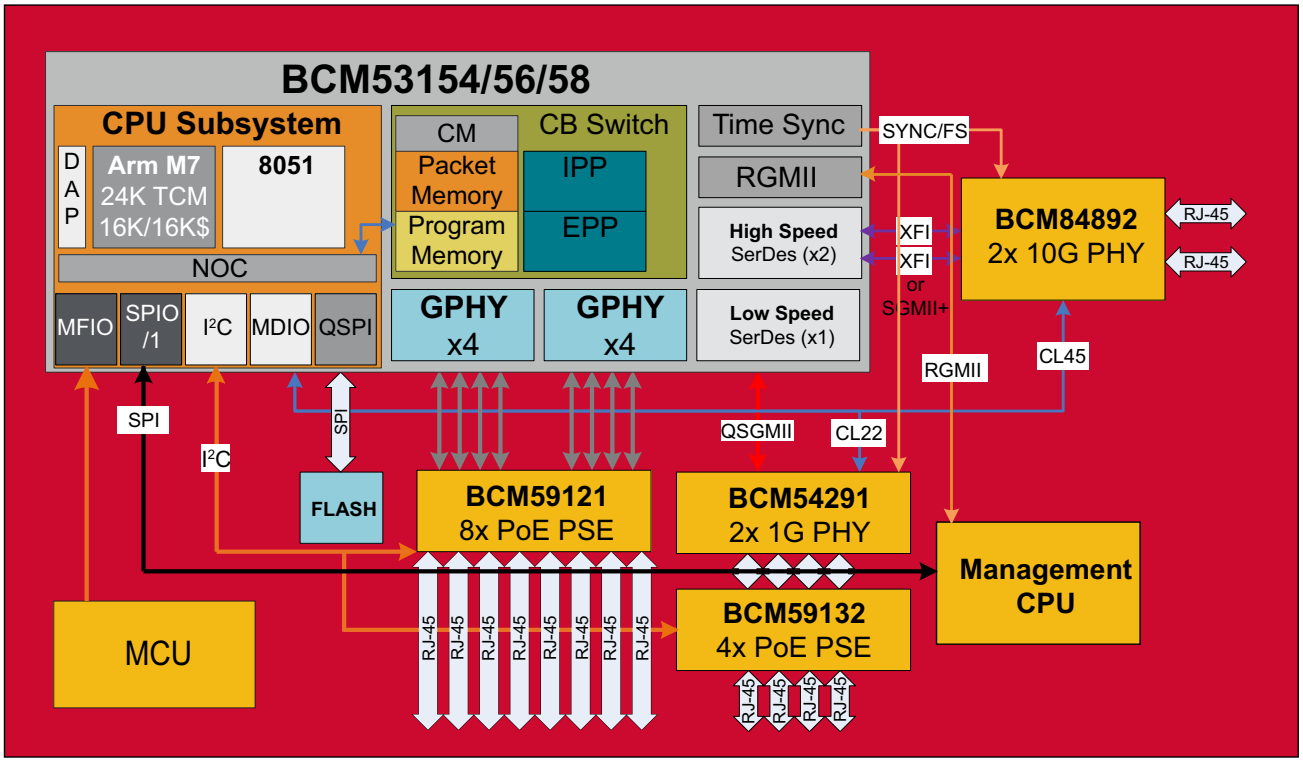
Here is a summary of features:

- All configuration of BCM53154/BCM53156/BCM53158 is handled by the external processor via the SPI slave interface.
- An external CPU is the management processor; the internal M7 may assist with this (hybrid mode).
- Packets which are destined for the external CPU are delivered by the IMP RGMII or any other port configured as an IMP port.

3.4.1 Managed Stand-Alone Configuration

The following shows a typical application for this configuration.

Figure 15: Managed Stand-Alone Configuration



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 25 describes the values for the valid OTP and strap settings.

Table 25: Managed Stand-Alone OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Stand-alone, no hardware forwarding
LIM Disable	Enabled (on)	–	–
CFP Disable	Enabled (on)	–	–

Table 25: Managed Stand-Alone OTP and Strap Configuration (Continued)

OTP Feature	Values	Strap Feature	Values
Robo 2 Switch Buffer Size[a]	768 KB PB, 256 KB M7	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs have the entire 1 MB of memory enabled. The partitioning between the packet buffer and CPU regions is flexible, and under software control (not OTP control).

The same code as unmanaged is executed by the M7 except it does not enable hardware forwarding.

The M7 Flash code on the BCM53154/BCM53156/BCM53158 device implements the following features:

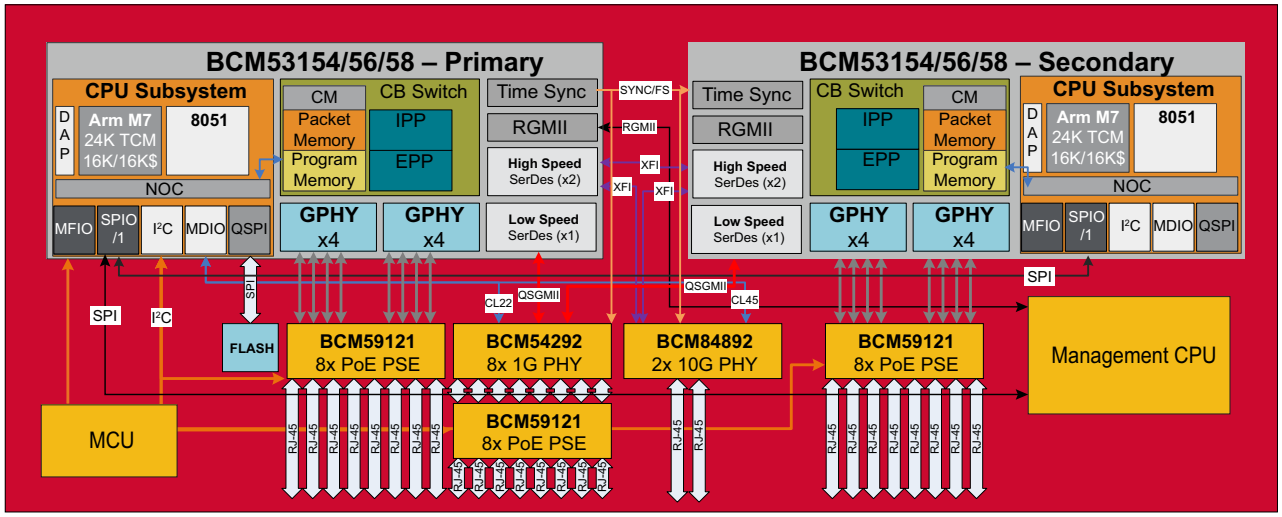
- Processing of straps and OTP configurations (ROM CODE)
- Basic unmanaged configuration of the switch core (M7 Flash Code)
- Identified as secondary based on straps (M7 Flash Code)
- Does NOT enable PHYS or unmanaged forwarding (M7 Flash Code)

The other initialization is done using the external processor.

3.4.1.1 Managed Cascade

This case is similar to the other cascade applications. The biggest difference is all configuration is performed by the external CPU.

Figure 16: Managed-Cascaded Configuration



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

The following straps shown in Table 26 are valid for this configuration.

NOTE: The cascaded configuration is stand-alone with no hardware forwarding. This is to prevent the unmanaged code from execution. Primary and Secondary configuration will be done via the external processor.

Table 26: Managed Cascade OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	Primary – M7 Flash Secondary – M7 Flash
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Primary – Stand-alone, no hardware forwarding Secondary – Stand-alone, no hardware forwarding
LIM Disable	Enabled (on)	–	–
CFP Disable	Enabled (on)	–	–
Robo 2 Switch Buffer Size[a]	768 KB PB, 256 KB M7	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs have the entire 1 MB of memory enabled. The partitioning between the packet buffer and CPU regions is flexible, and under software control (not OTP control).

The same code as unmanaged is executed by the M7 except it does not enable hardware forwarding.

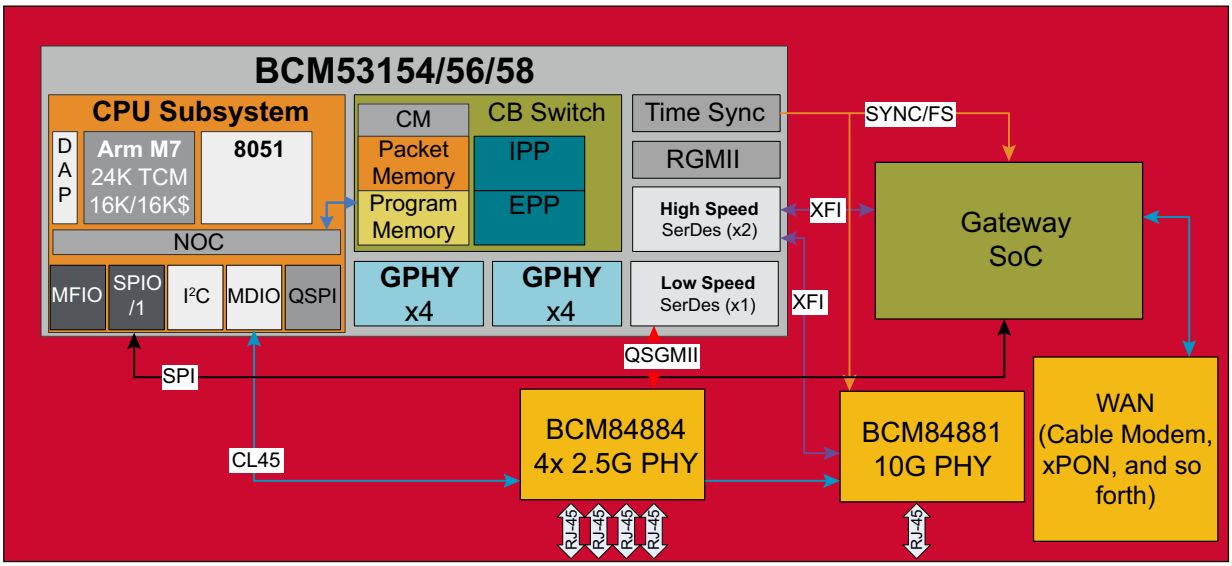
The M7 Flash code on BCM53154/BCM53156/BCM53158 device implements the following features:

- Processing of straps and OTP configurations (ROM CODE)
- Basic unmanaged configuration of the switch core (M7 Flash Code)
- Identified as secondary based on straps (M7 Flash Code)
- Does NOT enable PHYS or unmanaged forwarding (M7 Flash Code)

3.4.1.2 Managed Gateway

This is a special case of the managed operation. The primary difference is the external SoC is connected via one of the high-speed ports at 2.5/5/10G. In addition, this mode may operate when BCM53154/BCM53156/BCM53158 is in unmanaged mode with hardware forwarding and after the SoC boots, it will modify the configuration of the unmanaged switch.

Figure 17: Managed Gateway Operation



NOTE: See Table 2 for available interfaces and for the detailed port configuration of the BCM53154/BCM53156/BCM53158.

Table 27 shows the valid straps.

Table 27: Managed Stand-Alone OTP and Strap Configuration

OTP Feature	Values	Strap Feature	Values
XFI Disable	Disabled (on)	Boot_src	M7 Flash ROM
QSMII Disabled	Disabled (on)	Enable_qspi	Disable
ARL Size	16K Entries	Cascading_config	Stand-alone-no hardware forwarding Stand-alone-hardware forwarding
LIM Disable	Enabled (on)	–	–
CFP Disable	Enabled (on)	–	–
Robo 2 Switch Buffer Size[a]	768 KB PB, 256 KB M7	–	–
RGMII Disable	Disabled (on)	–	–
GPHY Disable	Disabled (on)	–	–
1G Disable	Disabled (on)	–	–

a. All SKUs have the entire 1 MB of memory enabled. The partitioning between the packet buffer and CPU regions is flexible, and under software control (not OTP control).

Chapter 4: Software Components

This section describes on of the software components the will run on the BCM53154/BCM53156/BCM53158. This is not an exhaustive list.

4.1 Robo 2 Switch Core Abstraction Libraries

A number of common software components are used across these application to provide a common, easy to use interface to the primarily Robo 2 switch core as well as some top level BCM53154/BCM53156/BCM53158 components (PHY). These libraries are used by both the M7 and external CPUs.

- OSAL (OS Abstraction Layer) (Broadcom) – This provides an abstraction layer to easy porting to different environments. OpenRTOS and Linux implementations will be done.
- CRAL (Coronado Bridge Register Abstraction Layer) (Broadcom) – This provides named register access to the Robo 2 switch core.
- FSAL (Forwarding and Switch Abstraction Layer) (Broadcom) – This API provides a simple and convenient way to control the Robo 2 switch core without having to manipulate the Robo 2 switch core registers directly.
- PHYMod (Broadcom) – This library is used to communicate and configure the internal and external PHY components.

4.2 8051 and M7 Running Environment

The operating environment is a bare metal environment. The following is list of components in the ROM environment:

Running on the 8051:

- SKU/OTP/Strap processing (ROM) – Process straps, OTP, and SKUS options.

Running on the M7:

- AVS mechanism
- Based device setup (ROM) – Configures PLL, clocks, and central memory.
- Basic Unmanaged Configuration (ROM) – Configures the Robo 2 switch core for default unmanaged configuration.
- Internal GPHY configuration (ROM) – Configures and enables GPHY ports.
- Link scan/error handling (ROM) – Handles links going up and down as well and any errors (ECC).

The following are advanced unmanaged features:

- Advanced registered playback – Reads register playback data from the QSPI Flash and applies it to the device and
- External components via MDIO and I^2C.
- AutoVOIP/AutoQoS/AutoDOS – Configures these features (that is, OUI and voice VLAN) from flash.
- AutoLoopDetect –Operation code which performs autoloop detect feature. This runs from flash.

4.3 M7 Operating System Environment

The M7 uses an operating system environment based on OpenRTOS/FreeRTOS. The following is a list of features:

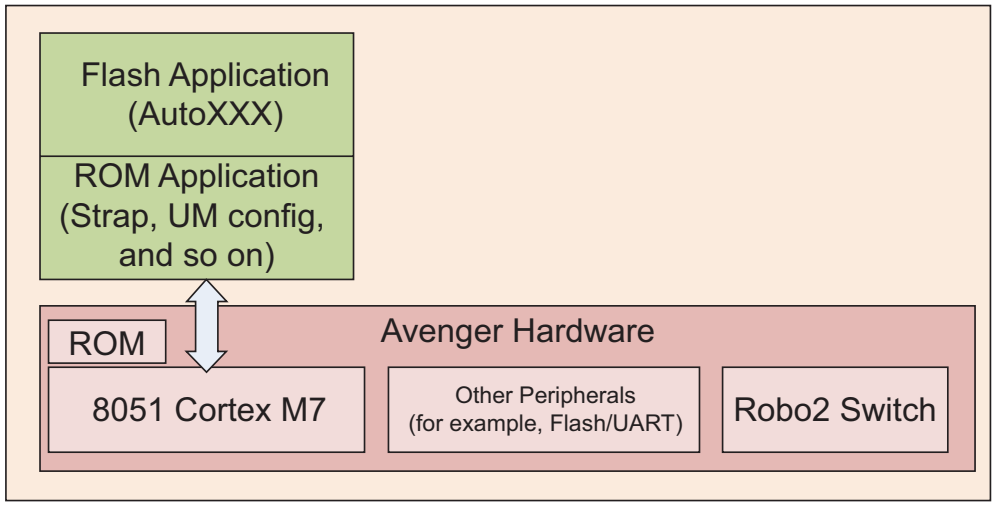
- Free/OPENRTOS (open source) – Real time operating system.
- ARM CMSIS-RTOS-CORE (ARM) – A generic peripheral driver interfaces for middleware making it reusable across supported devices provided by ARM. The API is RTOS independent and connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces.
- ARM CMSIS-Driver (ARM) – Portable device driver infrastructure.

- CRAL (Coronado Bridge Register Abstraction Layer) (Broadcom) – This is from our Robo 2 switch core common code library.
- OSAL (OS Abstraction Layer) (Broadcom) – This is from our Robo 2 switch core common code library.
- FSAL (Forwarding and Switch Abstraction Layer) – This is from our Robo 2 switch core common code library.
- TCP/IP Stack (open source) – The current selection for this stack lwIP.
- Web services: (licensed) – This will provides a http web server and back-end infrastructure for connecting into Robo 2 switch core.

4.4 Unmanaged Application

Figure 18 shows the basic unmanaged software components.

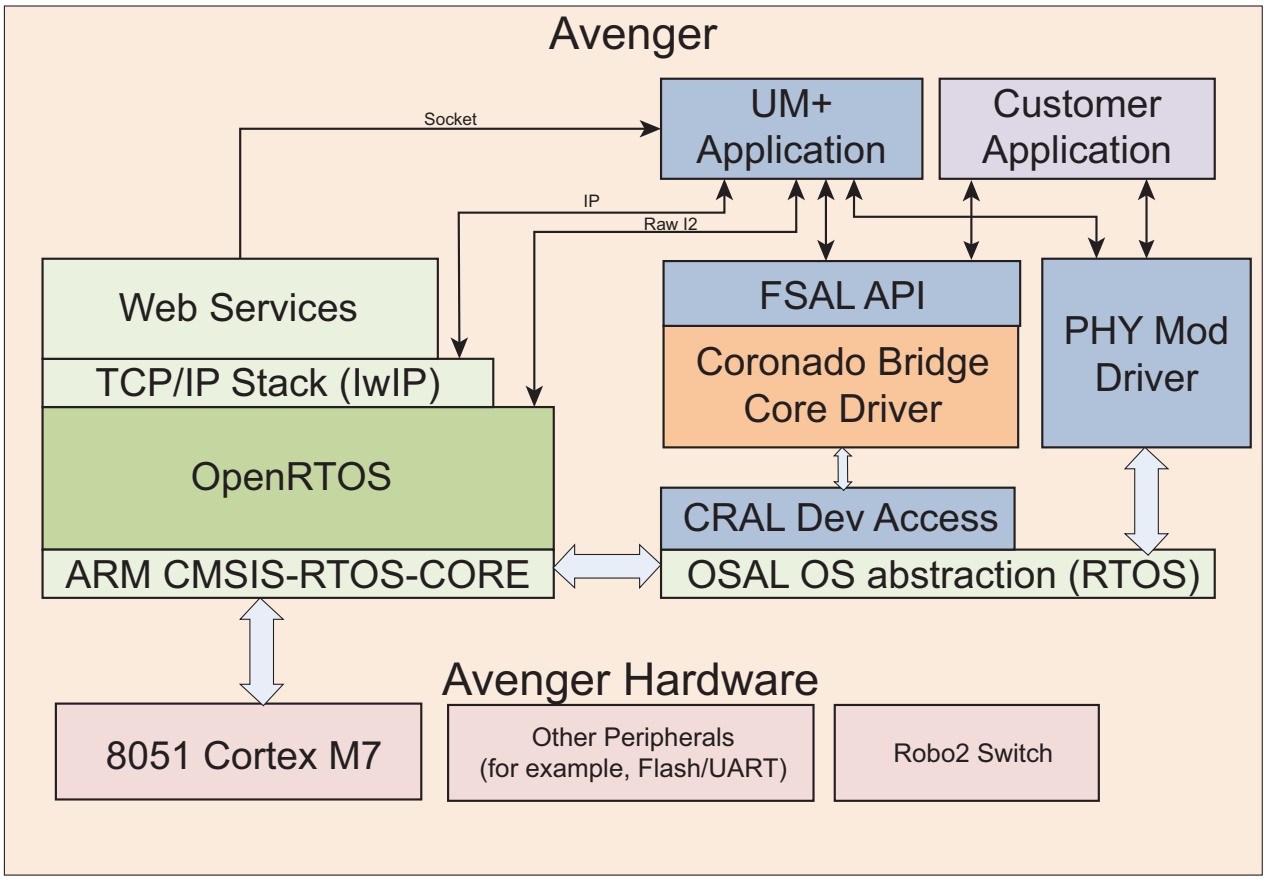
Figure 18: Unmanaged Software Components



4.5 Web-Managed Application

Figure 19 depicts the web-managed application.

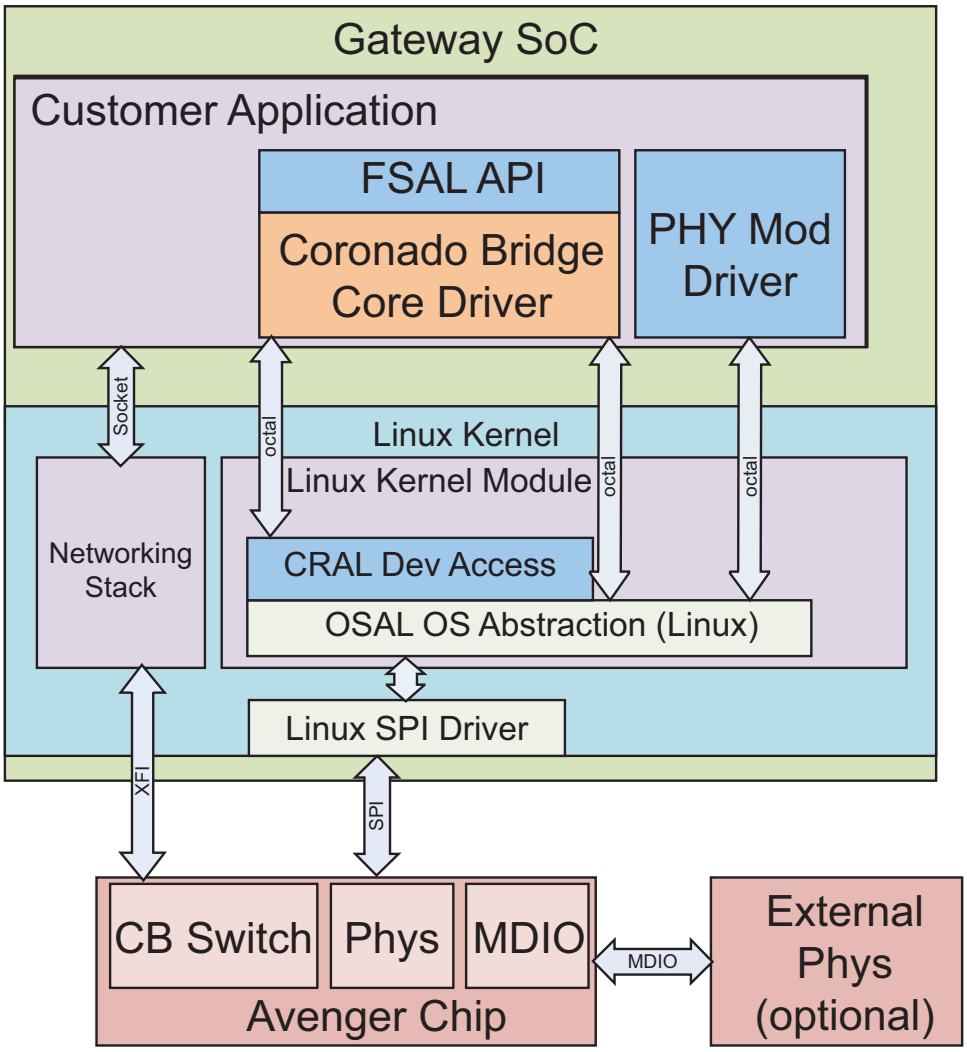
Figure 19: Web-Managed Application



4.6 Managed Application

Figure 20 shows the managed applications software components. It also has an external CPU.

Figure 20: Managed Application Software Components



Chapter 5: System Interfaces

5.1 Overview

The BCM53154/BCM53156/BCM53158 include the following interfaces:

- Copper Interface
- Frame Management Port Interface
- SerDes Interface
- Configuration Pins
- Programming Interfaces
- LED Interfaces
- Digital Voltage Regulator (LDO)

Each interface is discussed in detail in these sections.

5.2 Copper Interface

The internal PHYs transmit and receive data using the analog copper interface. This section discusses the following topics:

- Auto-Negotiation
- Line-Side (Remote) Loopback Mode

5.2.1 Auto-Negotiation

The BCM53154/BCM53156/BCM53158 negotiate a mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the BCM53154/BCM53156/BCM53158 automatically choose the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53154/BCM53156/BCM53158 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex.
- 100BASE-TX full-duplex and/or half-duplex.
- 10BASE-T full-duplex and/or half-duplex.

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be disabled by software control, but is required for 1000BASE-T operation.

5.2.2 Line-Side (Remote) Loopback Mode

The line-side loopback mode allows the testing of the copper interface from the link partner. This mode is enabled by setting bit 15 of the Miscellaneous Test register. The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the internal MAC interface.

5.3 Frame Management Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see “Interdevice Interface” on page 26. The port is configurable to RGMII using strap pins or software configuration.

NOTE: The Frame Management port interface supports only full-duplex mode.

The BCM53154/BCM53156/BCM53158 supports EEE features for external PHYs connected on the IMP and GMII (port5) only through the GMII interface.

5.3.1 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM53154/BCM53156/BCM53158 and an external management entity or an external PHY to provide additional data port capacity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits data synchronously using the TXD[3:0] and RXD[3:0] data signals. The BCM53154/BCM53156/BCM53158 offers either 2.5V or 1.5V RGMII interface with an external device.

5.4 SerDes Interface

The BCM53154/BCM53156/BCM53158 provides 1x QSGMII (BCM53158 Only) + 2x XFI interfaces.

5.5 Configuration Pins

Initial configuration of the BCM53154/BCM53156/BCM53158 takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes, and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration. See “Signal Descriptions” on page 95 for additional information.

5.6 Programming Interfaces

The BCM53154/BCM53156/BCM53158 can be programmed using the SPI interface. The interfaces share a common pin set that is configured using the strap pin. The “SPI Interface” provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM53154/BCM53156/BCM53158 register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol.

An explanation follows for using the serial interface with an SPI-compatible CPU (“SPI Interface”). Either mode can be selected with the strap pin. Either mode has access to the same register space.

5.6.1 SPI Interface

One way to access the BCM53154/BCM53156/BCM53158 internal registers is to use the SPI-compatible interface. This four-pin interface is designed to support a fully functional, bidirectional Motorola serial peripheral interface (SPI) for register read/write access. In addition, there is another SPI master for cascading configuration. The maximum speed of operation is 25 MHz.

5.6.2 SPI Slave

The SPI2 is a four-pin interface that comprises the following:

- SS2 – Slave select is used to signal start, end of transaction by the master.
- SCK2 – Slave Clock driven by Master.
- MOSI2 – Master output/slave input is used to send command, address and write data from the master. Data is received by slave one bit per clock; the endian-ness is Big endian.
- MISO2 – Master input/slave output is used to send read data from Slave. Data is sending one bit per clock, the endian-ness is Big endian.

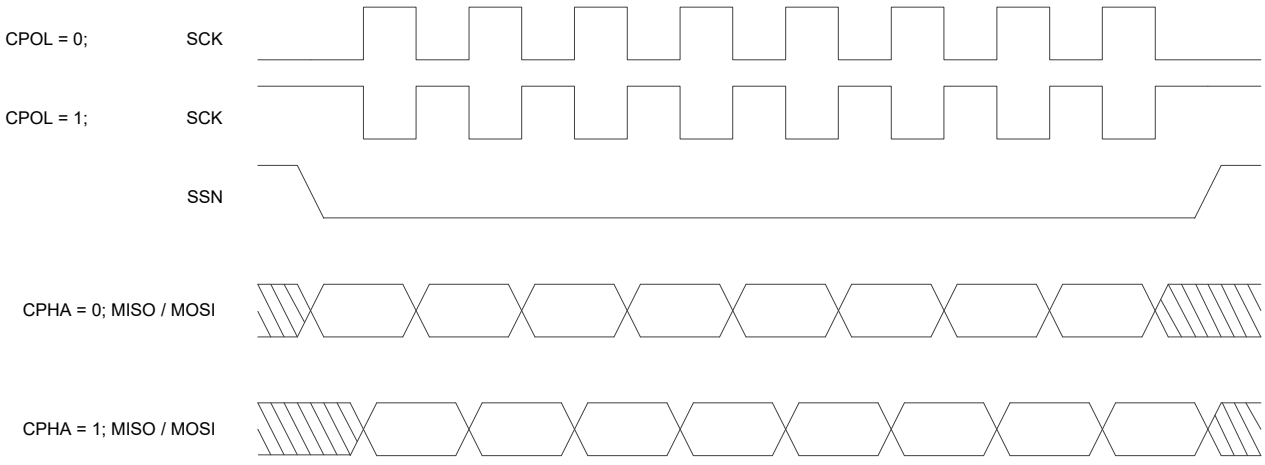
NOTE: In the BCM53154/BCM53156/BCM53158, the maximum SPI slave SCK frequency can be 25 MHz when the internal clock is 400 MHz and 20 MHz when internal the clock is 200 MHz.

5.6.2.1 SPI Transactions

In the idle state, the SSN should remain high and the SCK should be low. The master driving the SSN low indicates the start of the transaction. The SSN is held low until the end of the transaction. The clock is given by the master only when the SSN is low. The MOSI is used by the master to send the command, read the address, write the address, and write Data. The MISO is used to send back read data and status from the slave.

5.6.2.1.1 Clock Polarity and Phase

Figure 21: CPOL and CPHA



The CPOL are used to specify the base value of SCK, such as, value of SCK when in an idle state. The CPHA specifies the edges at which the data needs to be launched and captured. CPHA = 0 means transmitting data on the active to an idle state transition of SCK and capturing it on idle to active state transition. CPHA = 1 means transmitting data on the idle to active state transition of SCK and capturing it on active to idle state transition.

The SPI slave in the BCM53154/BCM53156/BCM53158 supports mode 1 (CPOL = 0/CPHA = 1) only on the A1 version. No other combination is supported. The SCK is low when idle. Transmit data is on the positive edge and receive is on the negative edge of SCK.

The SPI slave in the BCM53154/BCM53156/BCM53158 supports mode 1 (CPOL = 0/CPHA = 1) and mode 3 (CPOL = 1/CPHA = 1) on the B0 version. The default configuration is mode 3 support and can change to mode 1 support through a software override.

5.6.2.1.2 Fields

The following fields are used by SPI in BCM53154/BCM53156/BCM53158.

Table 28: Fields used in SPI

Field	No. of Bits	Description
Command	8	The command word specifies the operation to be performed.
Address	32	Address to be read/written to, given by SPI Master.
Status	16	Status of the latest Reads/Writes from SPIS. Separate status bytes are kept for reads and writes. And for overall SPI status.
Ack/Nack	8	Used only in Fast mode, to convey status of read, from SPIS.
Write Data	32x	Write Data is of variable length, but always in chunks of 32 bits as specified in the command word by the Master.
Read Data	32x	Read data will be of variable length, but always read in chunks of 32 bits from SPIS.

5.6.2.1.3 Command Word Format

Every transaction starts with the SSN going low. The first field after the SSN going low is the command. Multiple command word fields cannot exist in the same transaction. An 8-bit command word is used in the SPIS. The organization of the command word is as shown in Table 29 on page 79.

Table 29: Command Word Format

7	6	5	4	3	2	1	0
Transaction (Txn[3:0])				blen[2:0]			unused

To avoid confusion, read and write are termed as operations, while a transaction starts with SSN (active) going low and ends when the SSN goes high. A read or write operation may contain one or more transactions. The first field (in this case byte) is the command word.

5.6.2.1.4 Burst Length

Burst length is specified by the "blen" field in the command word for both read and write. Burst length is defined as follows:

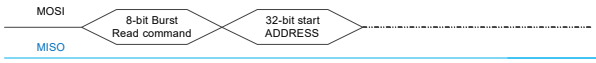
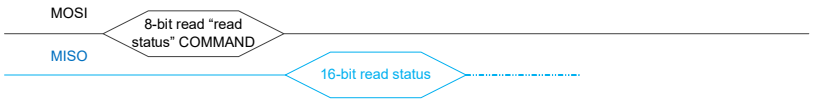
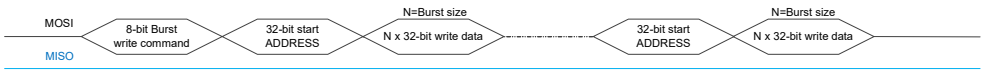
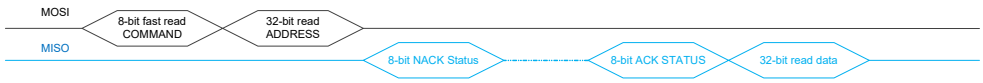
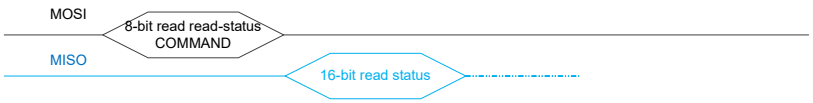
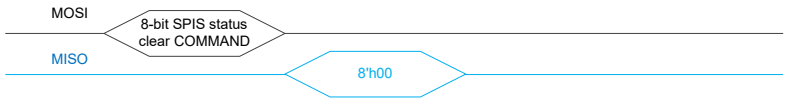
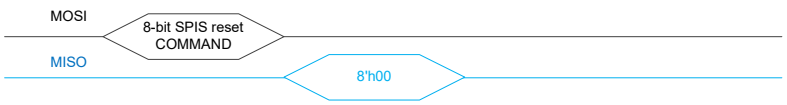
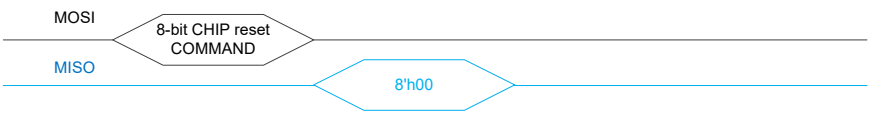
```
Burst_length = blen[2:0]+1.
```

One burst equals 4 bytes. Write/read data needs to always be in multiples of 4 bytes.

5.6.2.1.5 Supported Transactions

The SPI slave supports the following transactions, encoded using txn[3:0] as shown in Table 30.

Table 30: Transactions

Transaction	Tnx 3:0	Sequence of Steps
Read Request	0	
Read “Status”	1	
Read “Read Data”	2	
Write Request	4	
Read “Write Status”	5	
Fastmode Read	6	
Fastmode Write	7	
Read SPI Status	8	
Clear SPI Status	9	
Reset SPIS	10	
Reset Chip	11	

The total outstanding for both read and write is eight. The burst size limit is eight. In case the SPI slave receives more than eight requests for either a read or write, all requests after the limit (eight) is reached are aborted and an error status is reported through the SPI status register.

5.6.2.1.6 SPIS and Chip Reset

Two following reset transactions are provided in SPI Slave:

- SPIS Reset – Used to reset the SPI slave. This does not look at the state of the module before resetting it.
- Chip Reset – Tis generates a chip reset request, which goes to the CRU.

5.6.2.1.7 Read/Write Status Format

Read/Write status registers are 16-bit registers implemented as 2 bits per outstanding. The maximum number of outstanding transfers in which the slave can report status is eight. This 2-bit status reported by slave is encoded as follows:

- 2'b00 – Idle
- 2'b01 – Incomplete / Transaction Ongoing
- 2'b10 – Transaction finished successfully.
- 2'b11 – Transaction finished with error.

This only indicates the transaction status. In case of an error, the master can read the SPI status register to find the cause.

Table 31: Read/Write Status Register Format

15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Status $_{N}$	Status $_{N-1}$	Status $_{N-2}$	Status $_{N-3}$	Status $_{N-4}$	Status $_{N-5}$	Status $_{N-6}$	Status $_{N-7}$

5.6.2.1.8 SPI Status

SPI status will be implemented as a 16-bit status register as shown in Table 32.

Table 32: SPI Status Register Format

Bits	Field	Description
0	wr_ovf	Indicates that write requests overflowed. BCM5315X/BCM5316X supports up to 8 outstanding requests. Outstanding in this context of write means the status of write had not been read.
1	wr_abort	Indicates a write transaction on SPI had been terminated before it is complete.
2	wr_fm_oveflow	Fast mode write request received when there are outstanding write transactions. Fast mode should only be use when there are no outstanding transactions.
3	wr_fm_abort	Fast mode transaction aborted by SPI master
4	wr_axi_slverr	Slave error from NIC. Used when the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master.
5	wr_axi_decerr	Decode error from NIC. Generated, typically by an interconnect component, to indicate that there is no slave at the transaction address.
6	–	Unused
7	–	Unused
8	rd_ovf	Indicates that read requests overflowed. BCM5315X/BCM5316X supports up to 8 outstanding requests. Outstanding in this context of read means that the data had not been read.
9	rd_abort	Indicates a read request transaction on SPI had been terminated during the address phase.
10	rd_fm_oveflow	Fast mode read request received when there are outstanding write transactions. Fast mode should only be used when there are no outstanding transactions.
11	rd_fm_abort	Fast mode read transaction aborted by External master
12	rd_axi_slverr	Slave error from NIC. Used when the access has reached the slave successfully, but the slave wishes to return an error condition to the originating master
13	rd_axi_decerr	Decode error from NIC. Generated, typically by an interconnect component, to indicate that there is no slave at the transaction address.

Table 32: SPI Status Register Format (Continued)

Bits	Field	Description
14	–	Unused
15	–	Unused

5.6.2.1.9 ACK/NACK Byte Format

ACK/NACK bytes are used to convey the status of fast mode read and write transactions.

Table 33: ACK/NACK Byte Format

7	6	5	4	3	2	1	0
Unused (0)						txn_error	txn_done

The txn_error field is used to indicate that an error has occurred in the fast mode transaction. It is valid only if a transaction is done, that is, txn_done = 1;

5.6.2.2 SPI Slave Operation

The BCM53154/BCM53156/BCM53158 supports the following SPI slave operations:

5.6.2.2.1 Slave Mode Normal Write

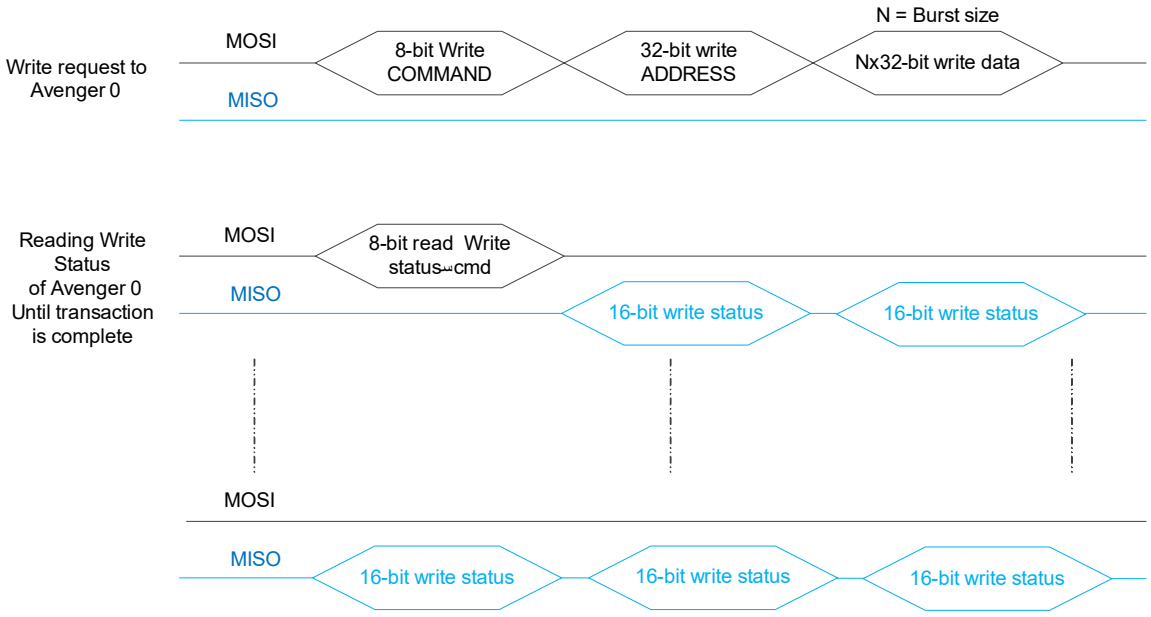
In a Normal Write operation, an 8-bit command, which specifies the operation to be performed and the size of write data in chunks of 32-bit words, is followed by 32-bit write address and write data.

Out of reset, all eight status fields in status a register are in an IDLE status. When a write request is received, the corresponding status field is updated to an INCOMPLETE status. When the write is done or if an error is reported, the status is updated to a FINISHED SUCCESSFULLY or a FINISHED WITH ERROR status, respectively. This status is retained until the Master reads this status, after which it is cleared to IDLE status.

The status is implemented like a shift register. Every new request would result in the status being left-shifted by two (with INCOMPLETE status). A burst of length N, is treated like N separate writes, and hence, results in the status being right-shifted by N*2(with INCOMPLETE status). In case the burst write request results in the number of outstanding transactions crossing the limit of eight, the whole write request is discarded and the write status is not updated, such as, it remains IDLE. Only the SPI status register flags the error status.

A write operation is considered finished only after the write done status is conveyed to the master. Until the status is given to the master, the status is retained in the write status register.

Figure 22: Slave Mode Normal Write



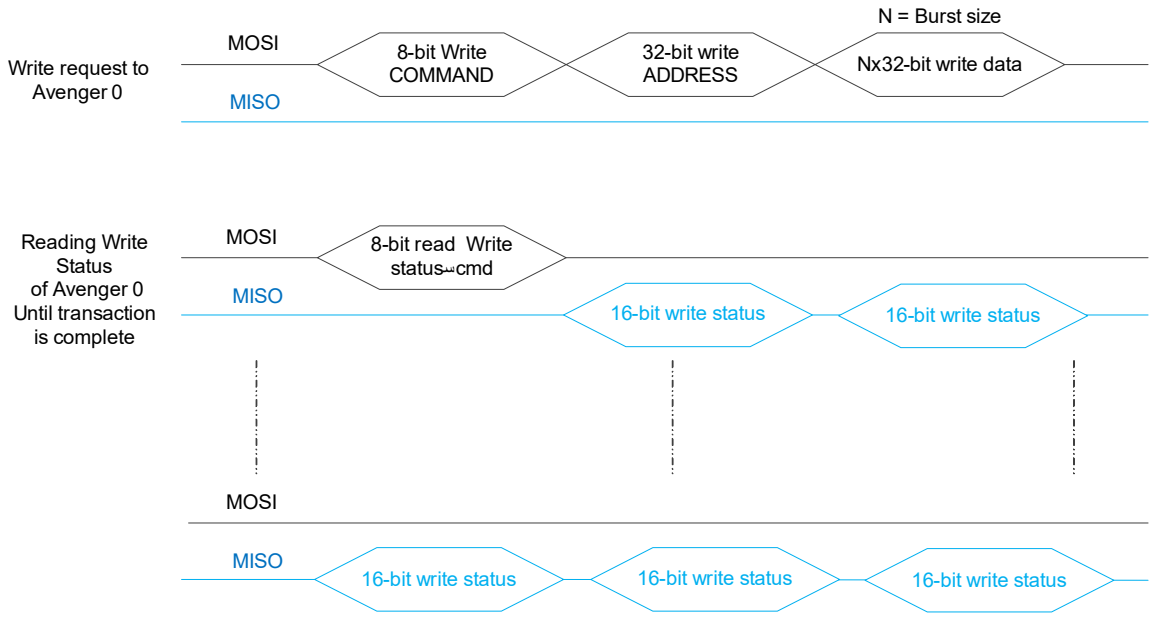
5.6.2.2.2 Slave Mode Normal Read

Out of reset, all eight status fields in the read status register are in an IDLE status. When a read request is received, the corresponding status field is updated to an INCOMPLETE status. When the read data is ready or if an error is reported, the status is updated to a FINISHED SUCCESSFULLY or a FINISHED WITH ERROR status respectively. This status is retained until the Master reads this status, after which it is cleared to IDLE status.

The status is implemented like a shift register. Every new request results in the status being left-shifted by two (with INCOMPLETE status). A burst of length N, is treated like N separate reads, and hence, results in the status being right-shifted by N*2(with INCOMPLETE status). In case the a burst read request results in the number of outstanding transactions crossing the limit of eight, the whole read request is discarded. The read status is not updated, that is, it remains IDLE. Only the SPI status register flags the error status.

In this case, the status of the transaction is incomplete in the status field, but the data is read, and the read data given out, is incorrect. A read operation is considered finished only after the read done status is conveyed to the master and master has read the data. Until the read data is given to the master, the status is retained in the read status register.

Figure 23: Slave Mode Normal Read



5.6.2.2.3 Slave Mode Fast Read

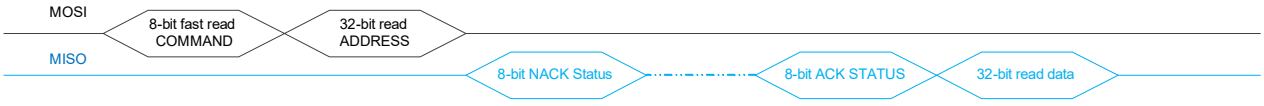
Fast mode (FM) read finishes in a single transaction. After the address field is sent the slave starts send NACK bytes, until the data is ready. Once the ready, it sends an ACK followed by 32-bit read data.

Fast mode does not support burst. It should not be done when there are outstanding transactions. If a fast read transaction is terminated in the middle of a transfer, the read data is lost.

This is the fastest way SPI can be used for a single read.

If a fast mode read is abandoned, the status and data are forever lost. An error is reported only using SPI status register.

Figure 24: Slave Mode Fast Read



5.6.2.2.4 Slave Mode Fast Write

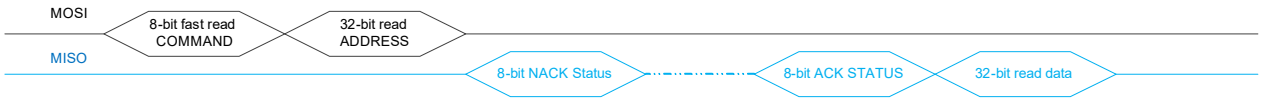
FM write finishes in a single transaction. After the address and 32-bit data fields are sent, the slave starts to send NACK bytes until the data is ready. Once ready, it sends ACK bytes.

Fast mode does not support burst. It should not be done when there are outstanding transactions. If a fast write transaction is terminated in the middle of a transfer, the action depends on the field being sent. If the write data is not fully received, the transaction is aborted unless the write data is received at SPI slave. The transaction happens but the status is lost.

This is the fastest way an SPI can be used for a single write.

If a fast-mode write transaction is aborted, the status is lost. The write may or may not happen on NIC based on the stage at which the transaction was aborted.

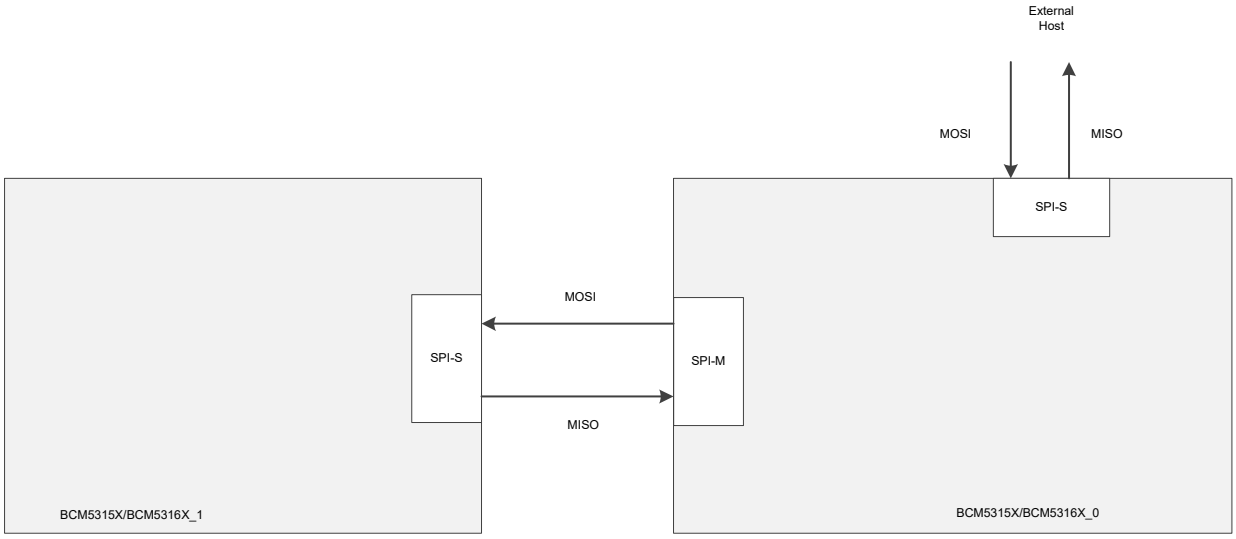
Figure 25: Slave Mode Fast Write



5.6.3 SPI Master

In cascaded mode, BCM53154/BCM53156/BCM53158_0 and BCM53154/BCM53156/BCM53158_1 are connected together using an SPI interface. SPI1 is an SPI Master-only interface; SPI2 is an SPI Slave-only interface. Figure 26 illustrates this scenario.

Figure 26: Block Diagram of SPI Connection for Cascading



5.6.3.1 SPI Master Operation

The BCM53154/BCM53156/BCM53158 supports the following SPI master operations:

5.6.3.1.1 Master Mode Normal Write

In a Normal Write operation, an 8-bit command, which specifies the operation to be performed and the size of write data in chunks of 32-bit words, is followed by 32-bit write address and write data.

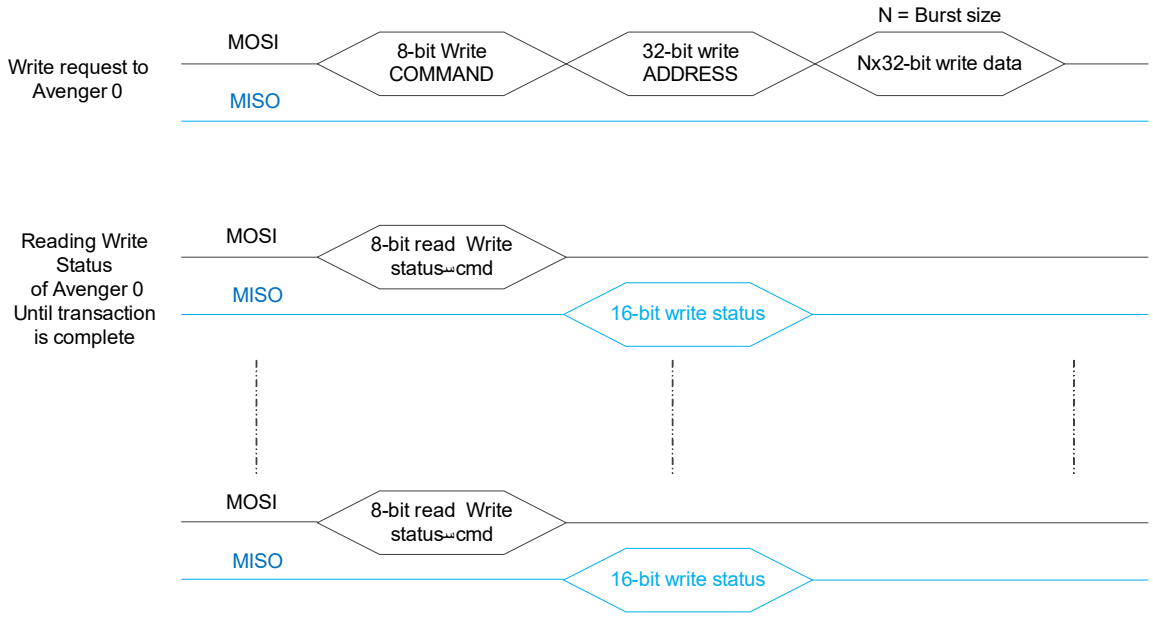
After the write data is sent, the master may choose to start sending another set of address/data in the same transaction.

Out of reset, all eight status fields in the status register are in an IDLE status. When a write request is received, the corresponding status field is updated to an INCOMPLETE status. When the write is done or if an error is reported, the status is updated to a FINISHED SUCCESSFULLY or a FINISHED WITH ERROR status, respectively. This status is retained until the Master reads this status, after which it is cleared to an IDLE status.

The status is implemented like a shift register. Every new request results in the status being left shifted by two (with INCOMPLETE status). A burst of length N, is treated like N separate writes, and hence, results in status being right shifted by N*2 (with INCOMPLETE status). In case the a burst write request result in the number of outstanding transactions crossing the limit of eight, the whole write request is discarded. The write status is not updated, that is, it remains IDLE. Only the SPI status register flags the error status.

A write operation is considered finished only after the write done status is conveyed to the master. Until the status is given to the master, the status is retained in the write status register.

Figure 27: Master Mode Normal Write



5.6.3.1.2 Master Mode Normal Read

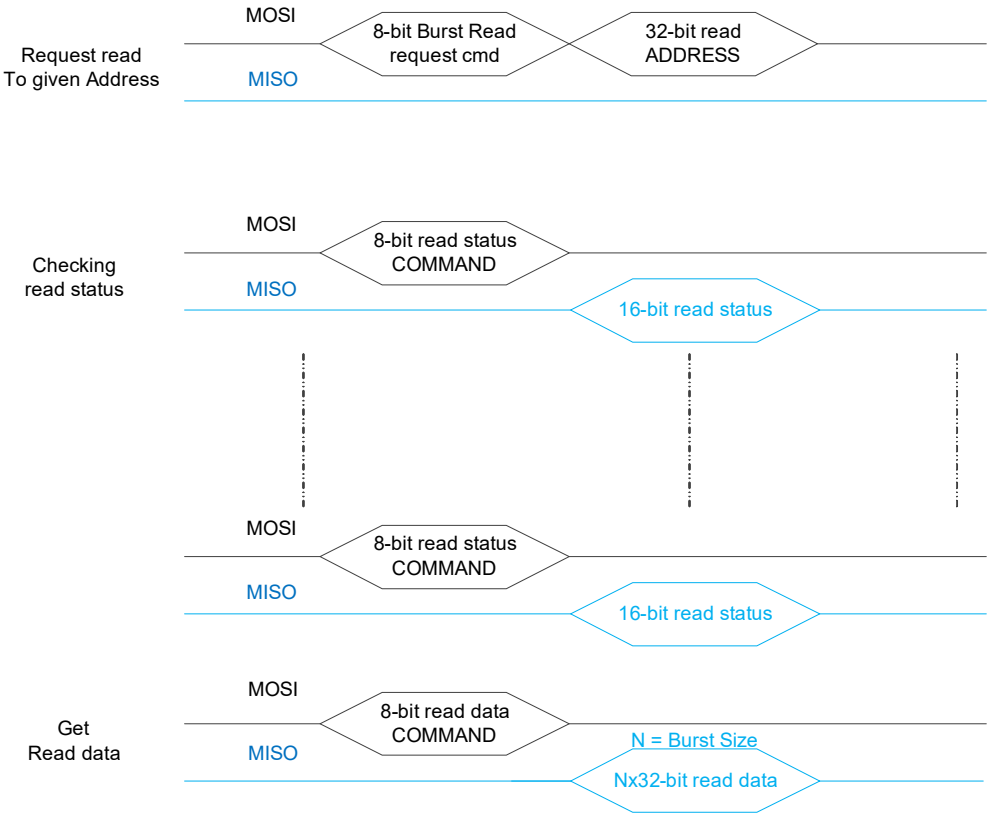
Out of reset, all eight status fields in the read status register are in an IDLE status. When a read request is received, the corresponding status field is updated to an INCOMPLETE status. When the read data is ready or if an error is reported, the status is updated to a FINISHED SUCCESSFULLY or a FINISHED WITH ERROR status respectively. This status is retained until the Master reads this status, after which it is cleared to an IDLE status.

The status is implemented like a shift register. Every new request results in the status being left shifted by two (with INCOMPLETE status). A burst of length N is treated like N separate reads, and hence, results in the status being right shifted by N*2 (with INCOMPLETE status). In case the a burst read request would result in the number of outstanding transactions crossing the limit of eight, the whole read request is discarded. The read status is not updated, that is, it remains IDLE. Only the SPI status register flags the error status.

In case the status of the transaction is incomplete in the status field but the data is read, the read data given out is incorrect. A read operation is considered finished only after the read done status is conveyed to the master and the master has read the data. Until the read data is given to the master, the status is retained in the read status register.

If the SPI Master has the capability to detect the read status live (without delay), it can choose to continue with the read status transaction and poll for the status, or if it is known that the status is ready, the master can use the read "read status + data" transaction, which can send data in the same transaction.

Figure 28: Master Mode Normal Read



5.6.4 Quad SPI Flash Interface

The BCM53154/BCM53156/BCM53158 offers a quad SPI interface and supports Execute in Place (XIP) as a boot source configured by a strapped option. The interface comprises six signal pins: chip select (SS), Flash clock (SCK), Data input/output (DATA0~3).

NOTE: EPROM and QSPI are both muxed in the same pins, therefore these two interfaces are exclusive.

5.6.5 MDC/MDIO Interface

The BCM53154/BCM53156/BCM53158 offers an MDC/MDIO interface (support both CL22 and CL45) for accessing the PHY registers. The PHY registers are accessed directly by using direct PHY addresses from 0x01~0x08.

NOTE: MDC/MDIO slave mode is for manufacturing testing only.

5.6.5.1 MDC/MDIO Interface Register Programming

The BCM53154/BCM53156/BCM53158 are designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM53154/BCM53156/BCM53158 sources a 2.5 MHz clock. Serial bidirectional data transmitted using the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM53154/BCM53156/BCM53158 and contains the following:

- **Preamble (PRE)**. To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- **Start of Frame** (**ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code** (**OP)**. A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address** (**PHYAD)**. A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address** (**REGAD)**. A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround** (**TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM53154/BCM53156/BCM53158 chip during these two bit times. When a read operation is being performed, the MDIO pin of the BCM53154/BCM53156/BCM53158 must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.
- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM53154/BCM53156/BCM53158. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Table 34 summarizes the complete management frame format.

Table 34: MII Management Frame Format

Operation	PRE	ST	OP	PHYAD	REGAD	TA	Data	Direction
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Driven by master Driven by slave
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to master

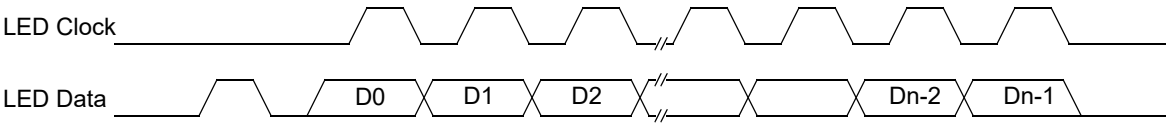
Table 35: PHY MDIO Address Map

MDIO Slave	MDIO Address
GPHY0-0	1
GPHY0-1	2
GPHY0-2	3
GPHY0-3	4
GPHY1-0	5
GPHY1-1	6
GPHY1-2	7
GPHY1-3	8
EAGLE PHY 0	9
EAGLE PHY 1	10
QSGMII/Combo PHY	11
Reserved for QSGMII	12–14

5.7 LED Interfaces

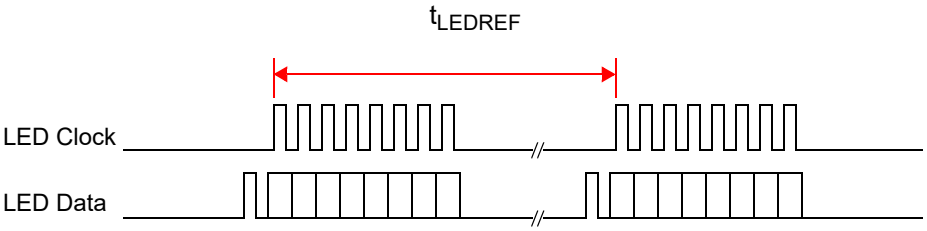
The CMICd provides two LED processors capable of retrieving status information from the ports in the device. After the status information has been retrieved and stored in the LED processor's memory, a user-created program is run that allows the LED process to build a serial bit-stream based on the LED status information. The BCM53154/BCM53156/BCM53158 splits the task of LED managements across the two LED processors, such that LED processor 0 is responsible for all of the Warpcore®-based and UNICORE-based ports, and LED processor 1 is responsible for the two Ethernet interfaces in the iProc and the Gigabit SerDes port. Each LED processor has a two-wire (clock and data) interface to control system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle (see Figure 29).

Figure 29: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically to refresh the LEDs (see Figure 30 on page 90).

Figure 30: LED Refresh Timing



5.8 Digital Voltage Regulator (LDO)

The BCM53154/BCM53156/BCM53158 LDO generates a 1.8V power supply. The 1.8V is used internally as an intermediate voltage level in 28 nm technology.

5.9 MFIO Interface

The BCM53154 offers a total of 16 MFIO (Multi-Function I/O) pins. The BCM53156/BCM53158 offers a total of nine MFIO pins. These MFIO pins can be programmable to operate in different function modes, such UART, GPIO, and so forth.

The following tables list the MFIO pins.

Table 36: MFIO Interface Pins (BCM53154)

Pins	Debug Mode = 0x01	Direction	Notes	GPIO Mode = 0x00	Direction	Notes	XFP Management Mode = 0x10	Direction	Notes	I²C Mode = 0x11	Direction
MFIO_0	uart_rxd	Input	Power on default (clkout can be any selected internal clock, for debug and test.)	GPIO_0	Inout	–	GPIO_0	Inout		GPIO_0	Inout
MFIO_1	uart_txd	Output		GPIO_1	Inout	–	clkout	Output	Test, debug	**SDA13**	Inout
MFIO_2	clkout	Output		GPIO_2	Inout	–	XFP0_Mod_ABS	Input	XFP0 interface signals	SDA12	Inout
MFIO_3	pwm0	Output		GPIO_3	Inout	–	XFP0_intr_n	Input		**SDA11**	Inout
MFIO_4	Reset_out	Output		GPIO_4	Inout	–	XFP0_TX_DIS	Output		SDA10	Inout
MFIO_5	pwm1	Output		GPIO_5	Inout	–	**XFP0_Mod_DeSel**	Output		SDA9	Inout
MFIO_6	pwm2	Output		GPIO_6	Inout	–	XFP0_RX_LOS	Input		SDA8	Inout
MFIO_7	pwm3	Output		GPIO_7	Inout	–	**XFP0_RST**	Output		SDA_gphy	Inout
MFIO_8	FRAME_SYNC_O	Output		GPIO_8	Inout	–	XFP0_Mod_NR	Input		SCL	Output
MFIO_9	FRAME_SYNC_I	Input		GPIO_9	Inout	Not bonded out on smallp ackage	XFP1_Mod_Desel	Output	XFP1 interface signals	**GPIO_9**	Inout
MFIO_10	GPHY_MUX_CLK1	Output		GPIO_10	Inout		**XFP1_intr_n**	Input		GPIO_10	Inout
MFIO_11	GPHY_MUX_VALID1	Output		GPIO_11	Inout		XFP1_TX_DIS	Output		GPIO_11	Inout
MFIO_12	GPIO_12	Input		GPIO_12	Inout		XFP1_Mod_ABS	Input		GPIO_12	Inout
MFIO_13	GPIO_13	Input		GPIO_13	Inout		**XFP1_RX_LOS**	Input		GPIO_13	Inout
MFIO_14	GPIO_14	Input		GPIO_14	Inout		XFP1_RST	Output		GPIO_14	Inout
MFIO_15	GPIO_15	Input		GPIO_15	Inout		XFP1_Mod_NR	Input		GPIO_15	Inout

NOTE:

1. Each MFIO function can be selected independently using CRU_CRU_MFIO_control_register (0x40200370).
2. The function of words in bold can be muxed to different functions for coexisting UART/I²C and both XFIs control signal problems as Errata (53112-5315X-5316X-ER102) description (AVR-ER 04 and AVR-ER 05) through register – CRU_CRU_MFIO_control_register_2 bit 31: MFIO_COMPATIBILITY_MODE in the B0 version.
3. All MFIO pins by default are in debug mode function pin after power on/reset.

Table 37: MFIO Muxing Function in the B0/B1 Chip for the 19x19 mm^2 Package (BCM53154)

Mode	MFIO_COMPATIBILITY_MODE	XFP Mode				I^{2}C Mode		
MFIO	Address: 0x40200374 Bit 31	MFIO_5	MFIO_7	MFIO_10	MFIO_13	MFIO_1	MFIO_3	MFIO_9
B0/B1	0 (default)	XFP0_Mod_DeSel	XFP0_RST	XFP1_intr_n	XFP1_RX_LOS	SDA13	SDA11	GPIO_9
	1	XFP1_intr_n	XFP1_RX_LOS	XFP0_Mod_DeSel	XFP0_RST	GPIO_1	SDA13	SDA11

Table 38: MFIO Interface Pins (BCM53156/BCM53158)

Pins	Debug Mode	Direction	Notes	GPIO Mode	Direction	Notes	XFP Management Mode	Direction	Notes	I^{2}C Mode	Direction
MFIO_0	uart_rxd	Input	Power on default (clkout can be any selected internal clock, for debug and test.)	GPIO_0	Inout	–	GPIO_0	Inout	–	GPIO_0	Inout
MFIO_1	uart_txd	Output		GPIO_1	Inout	–	clkout	Output	Test, debug	**SDA13**	Inout
MFIO_2	clkout	Output		GPIO_2	Inout	–	XFP0_Mod_ABS	Input	XFP0 interface signals	SDA12	Inout
MFIO_3	pwm0	Output		GPIO_3	Inout	–	XFP0_intr_n	Input		**SDA11**	Inout
MFIO_4	Reset_out	Output		GPIO_4	Inout	–	XFP0_TX_DIS	Output		SDA10	Inout
MFIO_5	pwm1	Output		GPIO_5	Inout	–	**XFP0_Mod_DeSel**	Output		SDA9	Inout
MFIO_6	pwm2	Output		GPIO_6	Inout	–	XFP0_RX_LOS	Input		SDA8	Inout
MFIO_7	pwm3	Output		GPIO_7	Inout	–	**XFP0_RST**	Output		SDA_gphy	Inout
MFIO_8	FRAME_SYNC_O	Inout		GPIO_8	Inout	–	XFP0_Mod_NR	Input		SCL	Output

NOTE:

1. Each MFIO function can be selected independently using CRU_CRU_MFIO_control_register (0x40200370).
2. The function of words in bold can be muxed to different functions for coexisting UART/I^{2}C and both XFIs control signal problems as Errata (53112-5315X-5316X-ER102) description (AVR-ER 04 and AVR-ER 05) through register – CRU_CRU_MFIO_control_register_2 bit 31: MFIO_COMPATIBILITY_MODE in the B0 version.

Table 39: MFIO Muxing Function in the B0/B1 Chip for the 13x13 mm^2 Package (BCM53156/BCM53158)

Mode	MFIO_COMPATIBILITY_MODE	XFP Mode		I^{2}C Mode	
MFIO	Address: 0x40200374 Bit 31	MFIO_5	MFIO_7	MFIO_1	MFIO_3
B0/B1	0 (default)	XFP0_Mod_DeSel	XFP0_RST	SDA13	SDA11
	1	XFP1_intr_n	XFP1_RX_LOS	GPIO_1	SDA13

Chapter 6: Hardware Signal Definitions

6.1 I/O Signal Types

Table 40 shows the conventions that are used to identify the I/O types. The I/O pin type is useful in referencing the DC pin characteristics.

Table 40: I/O Signal Type Definitions

Abbreviation	Description
XYZ	Active-low signal
3T	3.3V tolerant
A	Analog pin type
B	Bias pin type
CS	Continuously sampled
D	Digital pin type
DNC	Do not connect
GND	Ground
I	Input
Bi	Bidirectional
IPU	Input with internal pull-up
O3S	Tristated signal
ODO	Open-drain output
O	Output
PD	Internal pull-down
SOR	Sample on reset
PWR	Power pin supply
PU	Internal pull-up
XT	Crystal pin type

6.2 Signal Descriptions

6.2.1 13×13 mm^2 Package (BCM53156/BCM53158)

Table 41: Signal Descriptions (13×13 mm^2 Package)

Signal Name	Type and Default State	Description
PHY Interface		
TDP_PHY0_CH0	Bi	**TDP_PHY[#]_CH[#], TDN_PHY[#]_CH[#]** are transmit/receive pairs. n TRP/N_PHY[port number]_CH[channel number] for 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. In auto-negotiation and 10BASE-T and 100BASE-TX modes, the BCM53154/BCM53156/BCM53158 normally transmits on TRP/N_PHY[port number]_CH[0] and receives on TRD_PHY[port number]_CH[1].
TDN_PHY0_CH0	Bi	
TDP_PHY0_CH1	Bi	
TDN_PHY0_CH1	Bi	
TDP_PHY0_CH2	Bi	
TDN_PHY0_CH2	Bi	
TDP_PHY0_CH3	Bi	
TDN_PHY0_CH3	Bi	
TDP_PHY1_CH0	Bi	
TDN_PHY1_CH0	Bi	
TDP_PHY1_CH1	Bi	
TDN_PHY1_CH1	Bi	
TDP_PHY1_CH2	Bi	
TDN_PHY1_CH2	Bi	
TDP_PHY1_CH3	Bi	
TDN_PHY1_CH3	Bi	
TDP_PHY2_CH0	Bi	
TDN_PHY2_CH0	Bi	
TDP_PHY2_CH1	Bi	
TDN_PHY2_CH1	Bi	
TDP_PHY2_CH2	Bi	
TDN_PHY2_CH2	Bi	
TDP_PHY2_CH3	Bi	
TDN_PHY2_CH3	Bi	
TDP_PHY3_CH0	Bi	
TDN_PHY3_CH0	Bi	
TDP_PHY3_CH1	Bi	
TDN_PHY3_CH1	Bi	
TDP_PHY3_CH2	Bi	
TDN_PHY3_CH2	Bi	
TDP_PHY3_CH3	Bi	
TDN_PHY3_CH3	Bi	
TDP_PHY4_CH0	Bi	
TDN_PHY4_CH0	Bi	

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
TDP_PHY4_CH1	Bi	(Continued)
TDN_PHY4_CH1	Bi	
TDP_PHY4_CH2	Bi	
TDN_PHY4_CH2	Bi	
TDP_PHY4_CH3	Bi	
TDN_PHY4_CH3	Bi	
TDP_PHY5_CH0	Bi	
TDN_PHY5_CH0	Bi	
TDP_PHY5_CH1	Bi	
TDN_PHY5_CH1	Bi	
TDP_PHY5_CH2	Bi	
TDN_PHY5_CH2	Bi	
TDP_PHY5_CH3	Bi	
TDN_PHY5_CH3	Bi	
TDP_PHY6_CH0	Bi	
TDN_PHY6_CH0	Bi	
TDP_PHY6_CH1	Bi	
TDN_PHY6_CH1	Bi	
TDP_PHY6_CH2	Bi	
TDN_PHY6_CH2	Bi	
TDP_PHY6_CH3	Bi	
TDN_PHY6_CH3	Bi	
TDP_PHY7_CH0	Bi	
TDN_PHY7_CH0	Bi	
TDP_PHY7_CH1	Bi	
TDN_PHY7_CH1	Bi	
TDP_PHY7_CH2	Bi	
TDN_PHY7_CH2	Bi	
TDP_PHY7_CH3	Bi	
TDN_PHY7_CH3	Bi	
RESET/Clock		
RESET_L	I, Pu	**Hardware Reset Input**. Active low Schmitt-triggered input. Resets the BCM53154/BCM53156/BCM53158. Active low.
XTALP	I	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the BCM53154/BCM53156/BCM53158 by connecting a 25 MHz crystal between these two pins or by driving XTALP with a clock. When using a crystal, connect a loading capacitor from each pin to external 25 MHz oscillator GND.
XTALN	I	
XTAL_CML_P	O	Positive leg of the CML Driver Output from the internal XTAL circuit. Internal debug use only.
XTAL_CML_N	O	Negative leg of the CML Driver Output from the internal XTAL circuit. Internal debug use only.
PLL_TESTP/N	O	DNC, for internal use only.

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
RGMII Interface (for port 14)		
IMP_RXCLK	In, Pd	IMPRGMII Interface Receive Clock 125 MHz for 1000 Mb/s operation, 25 MHz for 100 Mb/s operation and 2.5 MHz for 10 Mb/s operation.
IMP_RXD_0	I, Pd	IMP port RGMII Receive Data Inputs. For 1000 Mb/s operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mb/s and 100 Mb/s modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK.
IMP_RXD_1	I, Pd	
IMP_RXD_2	I, Pd	
IMP_RXD_3	I, Pd	
IMP_RXDV	I, Pd	**IMP Port Receive Data Valid.** Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/management entity.
IMP_TXCLK	O, Pd	**IMP Port RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode (125 MHz for 1000 Mb/s operation, 25 MHz for 100 Mb/s operation, and 2.5 MHz for 10 Mb/s operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0].
IMP_TXD_0	O, Pd	**IMP Port RGMII Transmit Data Output.** For 1000 Mb/s operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mb/s and 100 Mb/s, data bits TXD[3:0] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor.
IMP_TXD_1	O, Pd	
IMP_TXD_2	O, Pd	
IMP_TXD_3	O, Pd	
IMP_TXEN	O, Pd	IMP Port RGMII Transmit Enable
QSGMII Interface for ports (BCM53158-Only)		
QSGMII_RDN0	I	QSGMII_Receive Pair
QSGMII_RDP0	I	
QSGMII_TDN0	O	QSGMII Transmit Pair
QSGMII_TDP0	O	
MDC/MDIO Interface (MDC/MDIO slave mode is for manufacturing testing only)		
MDC	Bi, Pd	**Management Data I/O.** In Master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers using the pseudo-PHY. See the MDC/MDIO interface for additional information.
MDIO	Bi, Pd	**Management Data Clock.** In master mode, this 2.5 MHz clock sourced by BCM53154/BCM53156/BCM53158 to the external PHY device. In Slave mode, it is sources by an external entity.
SPI Interfaces (SPI1 is an SPI master-only interface; SPI2 is an SPI slave-only interface.)		
SCK2 SCK1/en_eee	I, Pu O, Pu	**SPI Serial Clock.** The clock input to the BCM53154/BCM53156/BCM53158 SPI interface is supplied by the SPI master, which supports up to 25 MHz; sck1 is used as the strap pin for EN_EEE (Energy Efficient Ethernet). ■ 1'b0 – Disable EEE feature for switch MAC ■ 1'b1 – Enable EEE feature for switch MAC (default).
SS2 SS1/swd_jtag_sel	I, Pu O, Pu	**SPI Slave Select.** Active low signal that enables an SPI interface read or write operation. SS1 is also used as the strap pin for CM7DAP operation. ■ 1’b1 – CM7DAP is in JTAG mode ■ 1’b0 – CM7DAP is in SW mode

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
MISO2/boot_src0 MISO1	O, Pd I, Pd	**SPI Master-In/Slave-Out**. Output signal which transmits serial data during an SPI interface read operations. MISO2 is used as the strap pin for boot source selection 0. To set the boot source, use the values below: ■ 2'b00 – Reserved ■ 2'b01 – Reserved ■ 2'b10 – M7 boot from Flash ■ 2'b11 – Boot M7 from internal memory
MOSI2 MOSI1/cascading_config1	I, Pd O, Pd	**SPI Master-Out/Slave-In.** Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. MOSI1 is used as the strap pin for cascading_config1. To set the cascading_config[1:0] to below operation mode. ■ 2'b00 – Avenger standalone; hardware forwarding (unmanaged) ■ 2'b01 – Avenger cascading enabled; primary ■ 2'b10 – Avenger cascading enabled; secondary ■ 2'b11 – Avenger standalone; no hardware forwarding. **NOTE:** This signal is tristated during RESET.
JTAG Interface		
TMS	Bi	JTAG Mode Select Input.
TRST_L	Bi	**JTAG Test Reset**. Active low. Resets the JTAG controller. This signal must be pulled low during normal operation.
TCK	Bi	**JTAG Test Clock Input.** Clock Input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	Bi	**JTAG Test Data Input**. Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
TDO	Bi	**JTAG Test Data Output**. Serial data output to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
JTCE0, JTCE1	I	JTAG Capability; select as shown below: ■ 2b'00: DFT LVTAP ■ 2b'01: AVS ■ 2b'10: 8051 debug ■ 2b'11: M7 DAP
LED Interface **NOTE:** LED_[0-7][26][27]: The LED active state is the inverse of the state of strap setting. LED_[8-25]: The LED active state are always low.)		
LED_0/xtal_bypass	O, Pd	LED_0; LED_0 is also used as the strap pin for xtal bypass configuration. ■ 1'b1 – External clock is driven in XTAL pads ■ 1'b0 – Crystal is present on board to drive the XTAL pads ■ This strap goes to i_bypass pin of XTAL IP.
LED_1	O, Pd	LED1;
LED_2/xtal_freq_sel	O, Pd	LED2; LED_2 is also used as the strap pin for xtal frequency selection. ■ 1'b1 – 50 MHz XTAL clock ■ 1'b0 – 25 MHz XTAL clock
LED_3/enable_qspi	O, Pd	LED3;LED_3 is also used as the strap pin for QSPI selection. ■ 1'b1 – Reserved ■ 1'b0 – QSPI is connected or no connection in SPI0

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
LED_4/mdio_vol_sel	O, Pd	LED4; LED_4 is also used as the strap pin for MDIO voltage selection. ■ 1'b0 – 3.3V mode MDIO ■ 1'b1 – 1.2V mode MDIO
LED_5	O, Pd	LED5;
LED_6/mdio_master	O, Pu	LED6; LED_6 is also used as the strap pin for MDIO mode selection. ■ 1'b1 – Avenger is MDIO master ■ 1'b0 – Avenger is MDIO slave (Partial register access) ■ This strap pin must set to 1 for chip normal function and full register access.
LED_26_SCLK/ cascading_config0	O, Pd	LED_26_CLK is the LED Shift Clock. This clock is periodically active to enable LEDDATA to shift into external registers. LED_26_CLK is used as the strap pin for cascading_config0. To set the cascading_config[1:0] to below operation mode. ■ 2'b00 – Avenger stand-alone; hardware forwarding(unmanaged) ■ 2'b01 – Avenger cascading enabled ; primary ■ 2'b10 – Avenger cascading enabled; secondary ■ 2'b11 – Avenger stand-alone; no hardware forwarding.
LED_27_SDATA/boot_src1	O, Pd	LED_27_SDATA is Serial LED Data Output. Serial LED data for all ports is shifted out when LEDCLK is active. LED_27_SDATA is used as the strap pin for boot source selection 1. To set the boot source, use the values below. ■ 2'b00 – Reserved ■ 2'b01 – Reserved ■ 2'b10 – M7 boot from Flash ■ 2'b11 – Boot M7 from internal memory
QSPI Interface		
SS0	O	QUAD-SPI flash
DATA0	Bi	QUAD-SPI flash IO0
DATA1	BI	QUAD-SPI flash IO1
DATA2	BI	QUAD-SPI flash IO2
DATA3	BI	QUAD-SPI flash IO3
SCK0 /imp_vol_sel	O, Pd	QUAD-SPI flash; SCK0 is also used as the strap pin for IMP port voltage selection. ■ 1'b0 – IMP port works at 2.5V ■ 1'b1 – IMP port works at 1.5V
XFI Interface (XFI0 for port 13, XFI1 for port 12)		
NOTE: The BCM53156 only has XFI1 Port 12 (Pin# N1,N2,L1 and L2).		
XFI_TDP0	O	**XFI Transmit Serial Data, Port 0.** Serial data stream signals normally connected to an optical transmitter module. Internal 100Ω differential termination. Requires external A/C coupling.
XFI_TDN0	O	
XFI_TDP1	O	**XFI Transmit Serial Data, Port 1.** Serial data stream signals normally connected to an optical transmitter module. Internal 100Ω differential termination. Requires external A/C coupling.
XFI_TDN1	O	
XFI_RDP0	I	**XFI Receive Serial Data, Port 0.** Serial data stream signals normally connected to an optical receiver module. Internally biased with internal differential 100Ω termination.
XFI_RDN0	I	
XFI_RDP1	I	**XFI Receive Serial Data, Port 1.** Serial data stream signals normally connected to an optical receiver module. Internally biased with internal differential 100Ω termination.
XFI_RDN1	I	

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
XFI_REFCLKP/N	I	XFI reference clock, default the 156.25 MHz reference clock of SerDes will be generated by CRU internally. If the XFI needs a clock with less jitter than the internal system clock is providing; it can provide a clock externally by these two pins.
XFI_TESTP/N	O	DNC; for internal use only
REXT	O	External calibration resistor must connect 4.53 kΩ resistor to GND and place as close as possible to the BGA pin.
MFIO		
MFIO[8:0]	Bi	**MultiFunctional I/O.** For multiple functions and strap pin function for these pins. See Table 38 on page 92.
Interrupt		
INTR_L	O, Pu	**Interrupt.** This interrupt pin generates an interrupt based on the configuration in the Interrupt Enable register. It can be programmed to generate based on link status change of any port, or to generate an interrupt to a CPU entity when there is a packet(s) queued in the IMP transmit queue. This signal is active low.
Mode Selection		
TESTMODE0	I	Func/Test mode select. TESTMODE0 must be low for normal working mode.
TESTMODE1	I	
TESTMODE2	I	
TESTMODE3	I	
TESTMODE4	I	
Power Interface		
VDDC_1P0	PWR, In	1.0V Digital Core Power (AVS)
VDDO_3P3	PWR, In	3.3V Digital I/O
VSS	–	GND
VDDP_1P8_[1:0]	PWR, In	1.8V input for intermediate state for internal use. (The output is from LDO_VOUT.)
PLL_AVDD	PWR, In	1.8V for PLL
PHY_PLL_VDD1P0_1	PWR, In	1.0V for PHY 0~3 PLL
PHY_PLL_VDD1P0_2	PWR, In	1.0V for PHY 4~7 PLL
AVDD1P0_PHY_0	PWR, In	1.0V for GPHY I/O 0~3
AVDD1P0_PHY_4	PWR, In	1.0V for GPHY I/O 4~7
AVDD3P3_PHY_0	PWR, In	3.3V for GPHY I/O 0~3
AVDD3P3_PHY_4	PWR, In	3.3V for GPHY I/O 4~7
XTAL_AVDD	PWR, In	XTAL power supply 1.8V
BVDD3P3_1	PWR, In	3.3V for GPHY 0~3
BVDD3P3_2	PWR, In	3.3V for GPHY 4~7
SGMII_P_VDD1P0	PWR, In	QSGMII/SGMII Power Supply 1.0V
SGMII_R_VDD1P0	PWR, In	QSGMII/SGMII Power Supply 1.0V
XFI_P_VDD1P0	PWR, In	XFI Port Power Supply 1.0V
XFI_R_VDD1P0	PWR, In	XFI Port Power Supply 1.0V
MDIO_VDDO	PWR, In	3.3/1.2V I/O power for MDC/MDIO
MDIO_VDDP	PWR, In	1.8/1.2V I/O VDDP doe MDC/MDIO
IMP_VDDO	PWR, In	2.5V/1.5V I/O power for IMP port
IMP_VDDP	PWR, In	1.8V/1.5V I/O VDDP for IMP port

Table 41: Signal Descriptions (13×13 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
IMP_VOL_REF	PWR, In	GND/0.75V I/O Vref for IMP port
LDO Interface		
LDO_AVDD	PWR, In	3.3V for LDO power input
LDO_VOUT	PWR, Out	1.8V output from LDO. Maximum output current 300 mA.
Miscellaneous		
DNP	–	No physical ball (no solder mask)
NC	–	No Connect
PHY_RDC_[2:1]	–	6.04 kΩ resistor to GND is required.
REXT	–	External calibration resistor must connect 4.53 kΩ resistor to GND and place as close as possible to the BGA pin.
PVTMON_ADC PVTMON_DAC	O	Temperature and voltage monitor of internal analog DA/AD converter for internal use only; for internal use only. These two pins are needed to implement the AVS function for 1.0V core voltage. Refer to the Design Guide Application Note (5315X-5316X-AN1Xx) for more detailed information.

6.2.2 19×19 mm^2 Package (BCM53154)

Table 42: Signal Descriptions (19×19 mm^2 Package)

Signal Name	Type and Default State	Description
PHY Interface		
NOTE: The BCM53154 only has four GPHY interfaces (GPHY0 to GPHY 3).		
TDP_PHY0_CH0	Bi	**TDP_PHY[#]_CH[#], TDN_PHY[#]_CH[#]** are transmit/receive pairs. n TRP/N_PHY[port number]_CH[channel number] for 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. In auto-negotiation and 10BASE-T and 100BASE-TX modes, the normally transmits on TRP/N_PHY[port number]_CH[0] and receives on TRD_PHY[port number]_CH[1].
TDN_PHY0_CH0	Bi	
TDP_PHY0_CH1	Bi	
TDN_PHY0_CH1	Bi	
TDP_PHY0_CH2	Bi	
TDN_PHY0_CH2	Bi	
TDP_PHY0_CH3	Bi	
TDN_PHY0_CH3	Bi	
TDP_PHY1_CH0	Bi	
TDN_PHY1_CH0	Bi	
TDP_PHY1_CH1	Bi	
TDN_PHY1_CH1	Bi	
TDP_PHY1_CH2	Bi	
TDN_PHY1_CH2	Bi	
TDP_PHY1_CH3	Bi	
TDN_PHY1_CH3	Bi	
TDP_PHY2_CH0	Bi	
TDN_PHY2_CH0	Bi	

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
TDP_PHY2_CH1	Bi	
TDN_PHY2_CH1	Bi	
TDP_PHY2_CH2	Bi	
TDN_PHY2_CH2	Bi	
TDP_PHY2_CH3	Bi	
TDN_PHY2_CH3	Bi	
TDP_PHY3_CH0	Bi	
TDN_PHY3_CH0	Bi	
TDP_PHY3_CH1	Bi	
TDN_PHY3_CH1	Bi	
TDP_PHY3_CH2	Bi	
TDN_PHY3_CH2	Bi	
TDP_PHY3_CH3	Bi	
TDN_PHY3_CH3	Bi	
TDP_PHY4_CH0	Bi	
TDN_PHY4_CH0	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
DNP	Bi	
DNP	Bi	
DNP	Bi	
DNP	Bi	
RESET/Clock		
RESET_L	I, Pu	**Hardware Reset Input**. Active low Schmitt-triggered input. Resets the BCM53154/BCM53156/BCM53158. Active low.
XTALP	I	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the BCM53154/BCM53156/BCM53158 by connecting a 25 MHz crystal between these two pins or by driving XTALP with a clock. When using a crystal, connect a loading capacitor from each pin to external 25 MHz oscillator GND.
XTALN	I	
XTAL_CML_P	O	Positive leg of the CML Driver Output from the internal XTAL circuit. Internal debug use only.
XTAL_CML_N	O	Negative leg of the CML Driver Output from the internal XTAL circuit. Internal debug use only.
PLL_TESTP/N	O	DNC, for internal use only.
LCPLL_FREFP/N	O	DNC, for internal use only.
PLL_TVCO_[2:1]	O	DNC, for internal use only.
RGMII Interface (for port 14)		
IMP_RXCLK	In, Pd	IMPRGMII Interface Receive Clock 125 MHz for 1000 Mb/s operation, 25 MHz for 100 Mb/s operation and 2.5 MHz for 10 Mb/s operation.
IMP_RXD_0	I, Pd	IMP port RGMII Receive Data Inputs. For 1000 Mb/s operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mb/s and 100 Mb/s modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK.
IMP_RXD_1	I, Pd	
IMP_RXD_2	I, Pd	
IMP_RXD_3	I, Pd	
IMP_RXDV	I, Pd	**IMP port Receive Data Valid.** Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/management entity.
IMP_TXCLK	O, Pd	**IMP Port RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode (125 MHz for 1000 Mb/s operation, 25 MHz for 100 Mb/s operation, and 2.5 MHz for 10 Mb/s operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0].
IMP_TXD_0	O, Pd	**IMP Port RGMII Transmit Data Output.** For 1000 Mb/s operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mb/s and 100 Mb/s, data bits TXD[3:0] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor.
IMP_TXD_1	O, Pd	
IMP_TXD_2	O, Pd	
IMP_TXD_3	O, Pd	
IMP_TXEN	O, Pd	IMP Port RGMII Transmit Enable
SGMII Interface (for port 8)		
Q_SGMII_RDN0	I	QSGMII_Receive Pair
Q_SGMII_RDN0	I	
Q_SGMII_TDN0	O	QSGMII Transmit Pair
Q_SGMII_TDP0	O	
SGMII_REFCLKN	I	Differential clock input negative leg
SGMII_REFCLKP	I	Differential clock input positive leg
SGMII_TESTN	O	Differential clock output negative leg

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
SGMII_TESTP	O	Differential clock output positive leg
MDC/MDIO Interface (MDC/MDIO slave mode is for manufacturing testing only)		
MDC	Bi, Pd	**Management Data I/O.** In Master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers using the pseudo-PHY. See the MDC/MDIO interface for additional information.
MDIO	Bi, Pd	**Management Data Clock.** In master mode, this 2.5 MHz clock sourced by BCM53154/BCM53156/BCM53158 to the external PHY device. In Slave mode, it is sources by an external entity.
SPI Interfaces (SPI1 is an SPI master-only interface; SPI2 is an SPI slave-only interface.)		
SCK2 SCK1/en_eee	I, Pu O, Pu	**SPI Serial Clock.** The clock input to the BCM53154/BCM53156/BCM53158 SPI interface is supplied by the SPI master, which supports up to 25 MHz; sck1 is used as the strap pin for EN_EEE (Energy Efficient Ethernet). ■ 1'b0 – Disable EEE feature for switch MAC ■ 1'b1 – Enable EEE feature for switch MAC (default).
SS2 SS1/swd_jtag_sel	I, Pu O, Pu	**SPI Slave Select.** Active low signal that enables an SPI interface read or write operation. SS1 is also used as the strap pin for CM7DAP operation. ■ 1’b1 – CM7DAP is in JTAG mode ■ 1’b0 – CM7DAP is in SW mode
MISO2/boot_src0 MISO1	O, Pd I, Pd	**SPI Master-In/Slave-Out**. Output signal which transmits serial data during an SPI interface read operations. MISO2 is used as the strap pin for boot source selection 0. To set the boot source, use the values below: ■ 2’b00 – Reserved ■ 2’b01 – Reserved ■ 2’b10 – M7 boot from Flash ■ 2’b11 – Boot M7 from internal memory
MOSI2 MOSI1/cascading_config1	I, Pd O, Pd	**SPI Master-Out/Slave-In.** Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. MOSI1 is used as the strap pin for cascading_config1. To set the cascading_config[1:0] to below operation mode. ■ 2’b00 – Avenger standalone; hardware forwarding (unmanaged) ■ 2’b01 – Avenger cascading enabled; primary ■ 2’b10 – Avenger cascading enabled; secondary ■ 2’b11 – Avenger standalone; no hardware forwarding. **NOTE:** This signal is tristated during RESET.
JTAG Interface		
TMS	Bi	JTAG Mode Select Input.
TRST_L	Bi	**JTAG Test Reset**. Active low. Resets the JTAG controller. This signal must be pulled low during normal operation.
TCK	Bi	**JTAG Test Clock Input.** Clock Input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.
TDI	Bi	**JTAG Test Data Input**. Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
TDO	Bi	**JTAG Test Data Output**. Serial data output to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
JTCE0, JTCE1	I	JTAG Capability; select as shown below: ■ 2b'00: DFT LVTAP ■ 2b'01: AVS ■ 2b'10: 8051 debug ■ 2b'11: M7 DAP
LED Interface **NOTE:** LED_[0-7][26][27]: The LED active state is the inverse of the state of strap setting. LED_[8-25]: The LED active state are always low.)		
LED_0/xtal_bypass	O, Pd	LED_0; LED_0 is also used as the strap pin for xtal bypass configuration. ■ 1'b1 – External clock is driven in XTAL pads ■ 1'b0 – Crystal is present on board to drive the XTAL pads ■ This strap goes to i_bypass pin of XTAL IP.
LED_1	O, Pd	LED1;
LED_2/xtal_freq_sel	O, Pd	LED2; LED_2 is also used as the strap pin for xtal frequency selection. ■ 1'b1 – 50 MHz XTAL clock ■ 1'b0 – 25 MHz XTAL clock
LED_3/enable_qspi	O, Pd	LED3;LED_3 is also used as the strap pin for QSPI selection. ■ 1'b1 – Reserved ■ 1'b0 – QSPI is connected or no connection in SPI0
LED_4/mdio_vol_sel	O, Pd	LED4; LED_4 is also used as the strap pin for MDIO voltage selection. ■ 1'b0 – 3.3V mode MDIO ■ 1'b1 – 1.2V mode MDIO
LED_5	O, Pd	LED5;
LED_6/mdio_master	O, Pu	LED6; LED_6 is also used as the strap pin for MDIO mode selection. ■ 1'b1 – Avenger is MDIO master ■ 1'b0 – Avenger is MDIO slave (Partial register access) This strap pin must set to 1 for chip normal function and full register access.
LED_7/led_parallel_mode	O, Pd	LED7; LED_7 is also used as the strap pin for LED mode selection. ■ 1'b1 – LED is in parallel mode ■ 1'b0 – LED is in serial mode This strap selects led26/27 as serial led or parallel led.
LED_8	O, Pd	LED8
LED_9	O, Pd	LED9
LED_10	O, Pd	LED10
LED_11	O, Pd	LED11
LED_12	O, Pd	LED12
LED_13	O, Pd	LED13
LED_14	O, Pd	LED14
LED_15	O, Pd	LED15
LED_16	O, Pd	LED16
LED_17	O, Pd	LED17
LED_18	O, Pd	LED18
LED_19	O, Pd	LED19
LED_20	O, Pd	LED20
LED_21	O, Pd	LED21

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
LED_22	O, Pd	LED22
LED_23	O, Pd	LED23
LED_24	O, Pd	LED24
LED_25	O, Pd	LED25
LED_26_SCLK/ cascading_config0	O, Pd	LED_26_CLK is the LED Shift Clock. This clock is periodically active to enable LEDDATA to shift into external registers. LED_26_CLK is used as the strap pin for cascading_config0. To set the cascading_config[1:0] to below operation mode. ■ 2'b00 – Avenger stand-alone; hardware forwarding (unmanaged) ■ 2'b01 – Avenger cascading enabled; primary ■ 2'b10 – Avenger cascading enabled; secondary ■ 2'b11 – Avenger stand-alone; no hardware forwarding.
LED_27_SDATA/boot_src1	O, Pd	LED_27_SDATA is Serial LED Data Output. Serial LED data for all ports is shifted out when LEDCLK is active. LED_27_SDATA is used as the strap pin for boot source selection 1. To set the boot source, use the values below. ■ 2'b00 – Reserved ■ 2'b01 – Reserved ■ 2'b10 – M7 boot from flash ■ 2'b11 – Boot M7 from internal memory
I^{2}C Interface		
I2C_SCL	OD	BSC master clock
I2C_SDA_[13:8]	OD	BSC master data
QSPI Interface		
SS0	O	Quad-SPI flash
DATA0	Bi	Quad-SPI flash IO0
DATA1	BI	Quad-SPI flash IO1
DATA2	BI	Quad-SPI flash IO2
DATA3	BI	Quad-SPI flash IO3
SCK0/imp_vol_sel	O, Pd	Quad-SPI flash; SCK0 is also used as the strap pin for IMP port voltage selection. ■ 1'b0 – IMP port works at 2.5V ■ 1'b1 – IMP port works at 1.5V
MFIO		
MFIO[15:0]	Bi	**MultiFunctional I/O.** For multiple functions and strap pin function for these pins. See Table 36 on page 91.
Interrupt		
INTR_L	O, Pu	**Interrupt.** This interrupt pin generates an interrupt based on the configuration in the Interrupt Enable register. It can be programmed to generate based on link status change of any port, or to generate an interrupt to a CPU entity when there is a packet(s) queued in the IMP transmit queue. This signal is active low.
SyncE Interface		
SYNCE_REFCLKOUT	O	Recovered clock outputs from internal source. Can be selected from any of the switch internal cores. For details on mux selection, refer to 5315X-PG10X, CRU TS Core and CRU TS Top registers.
SYNCE_REFCLKOUT_VALID	O	Recovered clock output valid indicators.
SYNCE_RECOV_CLK [1:0]	I	Recovered clock inputs to DPLL function from external source.

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
SYNCE_RECOV_CLK_VALID[1:0]	I	Recovered clock inputs to DPLL function valid indicators.
SYNCIN_1588	I	Signal input be used to perform a Freq Sync with an External Source using the HW DPLL inside the Time-Sync Block of switch.
SYNCOUT_1588	O	Signal output from the Time-Sync Block that can be used for synchronization with the receiver of this signal.
NOTE: SYNCIN_1588 and SYNCOUT_1588 are used for Frequency and Phase Sync. These two pins can be used in conjunction with Frame_Sync_I(MFIO_9) and Frame_Sync_O(MFIO_8) for Phase alignment in addition to Frequency alignment, or they can be used alone (without Frame_Sync_In and Frame_Sync_Out) for freq and phase alignment but then the accuracy and convergence time of the SYNC "slave" to the SYNC "master" are lower than using SYNC + FRAME_SYNC.		
Mode Selection		
TESTMODE0	I	Func/Test mode select. TESTMODE0 must be low for normal working mode.
TESTMODE1	I	
TESTMODE2	I	
TESTMODE3	I	
TESTMODE4	I	
Power Interface		
VDDC_1P0	PWR, In	1.0V Digital Core Power (AVS)
VDDO_3P3	PWR, In	3.3V Digital I/O
VSS	–	GND
VDDP_1P8_[1:0]	PWR, In	1.8V input for intermediate state for internal use. (The output is from LDO_VOUT.)
PLL_AVDD	PWR, In	1.8V for PLL
PHY_PLL_VDD1P0_1	PWR, In	1.0V for PHY 0~3 PLL
PHY_PLL_VDD1P0_2	PWR, In	1.0V for PHY 4~7 PLL
AVDD1P0_PHY_0	PWR, In	1.0V for GPHY I/O 0~3
AVDD1P0_PHY_4	PWR, In	1.0V for GPHY I/O 4~7
AVDD3P3_PHY_0	PWR, In	3.3V for GPHY I/O 0~3
AVDD3P3_PHY_4	PWR, In	3.3V for GPHY I/O 4~7
XTAL_AVDD	PWR, In	XTAL power supply 1.8V
BVDD3P3_1	PWR, In	3.3V for GPHY 0~3
BVDD3P3_2	PWR, In	3.3V for GPHY 4~7
SGMII_P_VDD1P0	PWR, In	QSGMII/SGMII Power Supply 1.0V
SGMII_R_VDD1P0	PWR, In	QSGMII/SGMII Power Supply 1.0V
SGMII_T_VDD1P0	PWR, In	QSGMII/SGMII Power Supply 1.0V
XFI[0:1]_P_VDD1P0	PWR, In	XFI Port Power Supply 1.0V
XFI_T_R_VDD1P0	PWR, In	XFI Port Power Supply 1.0V
MDIO_VDDO	PWR, In	3.3/1.2V I/O power for MDC/MDIO
MDIO_VDDP	PWR, In	1.8/1.2V I/O VDDP doe MDC/MDIO
IMP_VDDO	PWR, In	2.5V/1.5V I/O power for IMP port
IMP_VDDP	PWR, In	1.8V/1.5V I/O VDDP for IMP port
IMP_VOL_REF	PWR, In	GND/0.75V I/O Vref for IMP port
LDO Interface		
LDO_AVDD	PWR, In	3.3V for LDO power input

Table 42: Signal Descriptions (19×19 mm^2 Package) (Continued)

Signal Name	Type and Default State	Description
LDO_VOUT	PWR, Out	1.8V output from LDO. Maximum output current 300 mA.
LDO_VSENSE	PWR, In	1.8V LDO sense in
Miscellaneous		
DNP	–	No physical ball (no solder mask)
NC	–	No Connect
PHY_RDC_[2:1]	–	6.04 kΩ resistor to GND is required.
REXT	–	External calibration resistor must connect 4.53 kΩ resistor to GND and place as close as possible to the BGA pin.
PVTMON_ADC PVTMON_DAC	O	Temperature and voltage monitor of internal analog DA/AD converter for internal use only; for internal use only. These two pins are needed to implement the AVS function for 1.0V core voltage. Refer to the Design Guide Application Note (5315X-5316X-AN1Xx) for more detailed information.

Chapter 7: Pin Assignment

7.1 Pin List by Pin Number (19×19 mm^2 Package) (BCM53154)

Ball No.	Ball Name
A1	VSS
A2	DNP
A3	DNP
A4	I2C_SCL
A5	VSS
A6	DNP
A7	DNP
A8	DNP
A9	DNP
A10	DNP
A11	DNP
A12	DNP
A13	DNP
A14	DNP
A15	TDN_PHY0_CH0
A16	TDP_PHY0_CH0
A17	DNP
A18	TDN_PHY1_CH3
A19	TDP_PHY1_CH3
A20	TDN_PHY2_CH0
A21	TDP_PHY2_CH0
A22	VSS
B1	DNP
B2	DNP
B3	TDN_PHY4_CH0
B4	I2C_SDA9
B5	I2C_SDA10
B6	DNP
B7	DNP
B8	DNP
B9	DNP
B10	DNP
B11	VSS
B12	DNP
B13	DNP
B14	VSS
B15	TDN_PHY0_CH1
B16	TDP_PHY0_CH1
B17	VSS
B18	TDN_PHY1_CH2
B19	TDP_PHY1_CH2
B20	VSS
B21	TDN_PHY2_CH1
B22	TDP_PHY2_CH1
C1	DNP
C2	DNP
C3	TDP_PHY4_CH0
C4	I2C_SDA11
C5	I2C_SDA12
C6	DNP
C7	DNP
C8	DNP
C9	DNP
C10	DNP
C11	PLL_TVCO_2
C12	DNP
C13	DNP
C14	VSS
C15	TDN_PHY0_CH2
C16	TDP_PHY0_CH2
C17	PHY_RDC1
C18	TDN_PHY1_CH1
C19	TDP_PHY1_CH1
C20	PLL_TVCO_1
C21	TDN_PHY2_CH2
C22	TDP_PHY2_CH2
D1	VSS
D2	VSS
D3	VSS
D4	DNP
D5	DNP
D6	VSS
D7	I2C_SDA13
D8	VSS
D9	DNP
D10	DNP
D11	VSS
D12	DNP
D13	DNP
D14	VSS
D15	TDN_PHY0_CH3
D16	TDP_PHY0_CH3
D17	VSS
D18	TDN_PHY1_CH0
D19	TDP_PHY1_CH0
D20	VSS
D21	TDN_PHY2_CH3
D22	TDP_PHY2_CH3
E1	DNP
E2	VSS
E3	XFI_RDN0DNP
E4	VSS
E5	DNP
E6	DNP
E7	I2C_SDA8
E8	VSS
E9	PHY_RDC2
E10	VSS
E11	PHY_PLL_VDD1P0_2
E12	AVDD1P0_PHY_4
E13	VSS
E14	VSS
E15	VSS
E16	VSS
E17	PHY_PLL_VDD1P0_1
E18	AVDD1P0_PHY_0
E19	TDN_PHY3_CH3
E20	TDN_PHY3_CH2
E21	TDN_PHY3_CH1
E22	TDP_PHY3_CH0
F1	DNP
F2	VSS
F3	DNP
F4	VSS
F5	DNP
F6	VSS
F7	DNP
F8	DNP
F9	DNP
F10	DNP
F11	DNP
F12	DNP
F13	DNP
F14	DNP
F15	DNP
F16	DNP
F17	DNP
F18	VSS
F19	TDP_PHY3_CH3
F20	TDP_PHY3_CH2
F21	TDP_PHY3_CH1
F22	TDN_PHY3_CH0
G1	VSS
G2	VSS
G3	VSS
G4	VSS
G5	VSS
G6	DNP
G7	VDDC_1P0
G8	VDDC_1P0
G9	VSS
G10	BVDD3P3_2
G11	VSS
G12	VSS
G13	VDDC_1P0
G14	VDDC_1P0
G15	VSS

Ball No.	Ball Name
G16	BVDD3P3_1
G17	DNP
G18	VSS
G19	VSS
G20	VSS
G21	VSS
G22	DNP
H1	DNP
H2	VSS
H3	DNP
H4	VSS
H5	DNP
H6	DNP
H7	VSS
H8	VSS
H9	VSS
H10	AVDD3P3_PHY_4
H11	AVDD3P3_PHY_4
H12	VSS
H13	VSS
H14	VSS
H15	VSS
H16	AVDD3P3_PHY_0
H17	DNP
H18	LED_1
H19	LED_0
H20	LED_3
H21	LED_2
H22	LED_4
J1	DNP
J2	VSS
J3	DNP
J4	VSS
J5	DNP
J6	DNP
J7	XFI0_P_VDD1P0
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VSS

Ball No.	Ball Name
J14	VSS
J15	VSS
J16	AVDD3P3_PHY_0
J17	DNP
J18	LED_5
J19	LED_7
J20	LED_6
J21	LED_8
J22	LED_9
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K5	XFI_T_R_VDD1P0
K6	DNP
K7	XFI1_P_VDD1P0
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K14	VSS
K15	VSS
K16	VSS
K17	DNP
K18	LED_10
K19	LED_11
K20	LED_12
K21	LED_13
K22	DNP
L1	SGMII_RDN3
L2	VSS
L3	SGMII_TDN3
L4	VSS
L5	SGMII_REFCLKN
L6	DNP
L7	VSS
L8	VSS
L9	VDDP_1P8
L10	VDDC_1P0
L11	VSS

Ball No.	Ball Name
L12	VSS
L13	VDDO_3P3
L14	VDDO_3P3
L15	VSS
L16	VSS
L17	DNP
L18	LED_14
L19	LED_15
L20	LED_16
L21	LED_17
L22	LED_18
M1	SGMII_RDP3
M2	VSS
M3	SGMII_TDP3
M4	VSS
M5	SGMII_REFCLKP
M6	DNP
M7	REXT
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
M16	VDDC_1P0
M17	DNP
M18	LED_19
M19	LED_20
M20	LED_21
M21	LED_22
M22	LED_23
N1	VSS
N2	VSS
N3	VSS
N4	SGMII_TESTN
N5	TESTMODE_0
N6	DNP
N7	VSS
N8	VSS
N9	VSS

Ball No.	Ball Name
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VDDC_1P0
N17	DNP
N18	LED_24
N19	LED_25
N20	VSS
N21	MFIO15
N22	DNP
P1	SGMII_TDN2
P2	VSS
P3	SGMII_RDN2
P4	SGMII_TESTP
P5	TESTMODE_1
P6	DNP
P7	SGMII_P_VDD1P0
P8	VSS
P9	VSS
P10	VSS
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P17	DNP
P18	JTCE_0
P19	INTR_L
P20	MFIO14
P21	MFIO13
P22	MFIO12
R1	SGMII_TDP2
R2	VSS
R3	SGMII_RDP2
R4	VSS
R5	VDDC_1P0
R6	DNP
R7	VSS

Ball No.	Ball Name
R8	VSS
R9	VSS
R10	VDDP_1P8
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	IMP_VDDP
R16	VDDC_1P0
R17	DNP
R18	JTCE_1
R19	RESET_L
R20	MFIO11
R21	MFIO10
R22	MFIO9
T1	VSS
T2	SGMII_T_VDD1P0
T3	SGMII_R_VDD1P0
T4	VSS
T5	TESTMODE_2
T6	DNP
T7	TESTMODE_3
T8	PLL_AVDD
T9	TESTMODE_4
T10	VSS
T11	VDDC_1P0
T12	VDDC_1P0
T13	VDDC_1P0
T14	VDDC_1P0
T15	IMP_VDDO
T16	VDDC_1P0
T17	DNP
T18	TDI
T19	MFIO8
T20	MFIO7
T21	MFIO6
T22	DNP
U1	SGMII_TDN1
U2	VSS
U3	VSS
U4	VSS
U5	LCPLL_FREFN

Ball No.	Ball Name
U6	DNP
U7	DNP
U8	DNP
U9	DNP
U10	DNP
U11	DNP
U12	DNP
U13	DNP
U14	DNP
U15	DNP
U16	DNP
U17	DNP
U18	TDO
U19	MFIO5
U20	MFIO4
U21	MFIO3
U22	MFIO2
V1	SGMII_TDP1
V2	VSS
V3	SGMII_RDN1
V4	VSS
V5	LCPLL_FREFP
V6	VSS
V7	LDO_AVDD
V8	LDO_VOUT
V9	SFP8_TX_FAULT
V10	SFP8_TX_DISABLE
V11	SFP8_LOS
V12	SFP8_MOD_DEF0
V13	SFP9_TX_FAULT
V14	MDIO_VDDP
V15	MDIO_VDDO
V16	SCK2
V17	MOSI2
V18	TCK
V19	TRST_L
V20	TMS
V21	MFIO1
V22	MFIO0
W1	VSS
W2	VSS
W3	SGMII_RDP1

Ball No.	Ball Name
W4	VSS
W5	PLL_TESTN
W6	VSS
W7	LDO_VSENSE
W8	PVTMON_ADC
W9	SFP9_TX_DISABLE
W10	SFP9_LOS
W11	SFP9_MOD_DEF0
W12	SFP10_TX_FAULT
W13	SFP10_TX_DISABLE
W14	MDC
W15	MDIO
W16	MISO2
W17	SS2
W18	VSS
W19	IMP_VOL_REF
W20	IMP_RXD0
W21	IMP_RXCLK
W22	DNP
Y1	Q_SGMII_TDN0
Y2	VSS
Y3	VSS
Y4	VSS
Y5	PLL_TESTP
Y6	VSS
Y7	VSS
Y8	PVTMON_DAC
Y9	SFP10_LOS
Y10	SFP10_MOD_DEF0
Y11	SFP11_TX_FAULT
Y12	SYNCE_REFCLKOUT_VALID
Y13	SFP11_TX_DISABLE
Y14	VSS
Y15	DATA3
Y16	DATA2
Y17	MISO1
Y18	SS1
Y19	IMP_RXDV
Y20	IMP_RXD1
Y21	IMP_RXD2

Ball No.	Ball Name
Y22	IMP_RXD3
AA1	Q_SGMII_TDP0
AA2	VSS
AA3	Q_SGMII_RDN0
AA4	VSS
AA5	XTAL_CML_P
AA6	XTAL_AVDD
AA7	VSS
AA8	VSS
AA9	SYNCIN_1588
AA10	SYNCE_RECOV_CLK_VALID0
AA11	SYNCE_RECOV_CLK0
AA12	SYNCE_REFCLKOUT

Ball No.	Ball Name
AA13	SFP11_LOS
AA14	SFP11_MOD_DEF0
AA15	DATA1
AA16	SS0
AA17	MOSI1
AA18	LED_26_SCLK
AA19	IMP_TXEN
AA20	IMP_TXD1
AA21	IMP_TXD3
AA22	IMP_TXCLK
AB1	VSS
AB2	VSS
AB3	Q_SGMII_RDP0

Ball No.	Ball Name
AB4	VSS
AB5	XTAL_CML_N
AB6	XTALN
AB7	XTALP
AB8	VSS
AB9	SYNCOUT_1588
AB10	DNP
AB11	SYNCE_RECOV_CLK1
AB12	SYNCE_RECOV_CLK_VALID1
AB13	DNP
AB14	SCK0
AB15	DATA0

Ball No.	Ball Name
AB16	DNP
AB17	SCK1
AB18	LED_27_SDATA
AB19	DNP
AB20	IMP_TXD0
AB21	IMP_TXD2
AB22	VSS

7.2 Pin List by Pin Name (19×19 mm^2 Package) (BCM53154)

Ball No.	Ball Name
E18	AVDD1P0_PHY_0
E12	AVDD1P0_PHY_4
H16	AVDD3P3_PHY_0
J16	AVDD3P3_PHY_0
H10	AVDD3P3_PHY_4
H11	AVDD3P3_PHY_4
G16	BVDD3P3_1
G10	BVDD3P3_2
AB15	DATA0
AA15	DATA1
Y16	DATA2
Y15	DATA3
A8	DNP
A11	DNP
A14	DNP
A17	DNP
D4	DNP
D5	DNP
E6	DNP
F7	DNP
F8	DNP
F9	DNP
F10	DNP
F11	DNP
F12	DNP
F13	DNP
F14	DNP
F15	DNP
F16	DNP
F17	DNP
G6	DNP
G17	DNP
G22	DNP
H6	DNP
H17	DNP
J6	DNP
J17	DNP
K6	DNP
K17	DNP
K22	DNP
L6	DNP
L17	DNP
M6	DNP
M17	DNP
N6	DNP
N17	DNP
N22	DNP
P6	DNP
P17	DNP
R6	DNP
R17	DNP
T6	DNP
T17	DNP
T22	DNP
U6	DNP
U7	DNP
U8	DNP
U9	DNP
U10	DNP
U11	DNP
U12	DNP
U13	DNP
U14	DNP
U15	DNP
U16	DNP
U17	DNP
W22	DNP
AB10	DNP
AB13	DNP
AB16	DNP
AB19	DNP
A4	I2C_SCL
B5	I2C_SDA10
C4	I2C_SDA11
C5	I2C_SDA12
D7	I2C_SDA13
E7	I2C_SDA8
B4	I2C_SDA9
W21	IMP_RXCLK
W20	IMP_RXD0
Y20	IMP_RXD1
Y21	IMP_RXD2
Y22	IMP_RXD3
Y19	IMP_RXDV
AA22	IMP_TXCLK
AB20	IMP_TXD0
AA20	IMP_TXD1
AB21	IMP_TXD2
AA21	IMP_TXD3
AA19	IMP_TXEN
T15	IMP_VDDO
R15	IMP_VDDP
W19	IMP_VOL_REF
P19	INTR_L
P18	JTCE_0
R18	JTCE_1
U5	LCPLL_FREFN
V5	LCPLL_FREFP
V7	LDO_AVDD
V8	LDO_VOUT
W7	LDO_VSENSE
H19	LED_0
H18	LED_1
K18	LED_10
K19	LED_11
K20	LED_12
K21	LED_13
L18	LED_14
L19	LED_15
L20	LED_16
L21	LED_17
L22	LED_18
M18	LED_19
H21	LED_2
M19	LED_20
M20	LED_21
M21	LED_22
M22	LED_23
N18	LED_24
N19	LED_25
AA18	LED_26_SCLK
AB18	LED_27_SDATA
H20	LED_3
H22	LED_4
J18	LED_5
J20	LED_6
J19	LED_7
J21	LED_8
J22	LED_9
W14	MDC
W15	MDIO
V15	MDIO_VDDO
V14	MDIO_VDDP
V22	MFIO0
V21	MFIO1
R21	MFIO10
R20	MFIO11
P22	MFIO12
P21	MFIO13
P20	MFIO14
N21	MFIO15
U22	MFIO2
U21	MFIO3
U20	MFIO4
U19	MFIO5
T21	MFIO6
T20	MFIO7
T19	MFIO8
R22	MFIO9
Y17	MISO1
W16	MISO2
AA17	MOSI1
V17	MOSI2
E17	PHY_PLL_VDD1P0_1
E11	PHY_PLL_VDD1P0_2
C17	PHY_RDC1
E9	PHY_RDC2
T8	PLL_AVDD
W5	PLL_TESTN
Y5	PLL_TESTP
C20	PLL_TVCO_1
C11	PLL_TVCO_2
W8	PVTMON_ADC

Ball No.	Ball Name
Y8	PVTMON_DAC
AA3	Q_SGMII_RDN0
AB3	Q_SGMII_RDP0
Y1	Q_SGMII_TDN0
AA1	Q_SGMII_TDP0
R19	RESET_L
M7	REXT
AB14	SCK0
AB17	SCK1
V16	SCK2
Y9	SFP10_LOS
Y10	SFP10_MOD_DEF0
W13	SFP10_TX_DISABLE
W12	SFP10_TX_FAULT
AA13	SFP11_LOS
AA14	SFP11_MOD_DEF0
Y13	SFP11_TX_DISABLE
Y11	SFP11_TX_FAULT
V11	SFP8_LOS
V12	SFP8_MOD_DEF0
V10	SFP8_TX_DISABLE
V9	SFP8_TX_FAULT
W10	SFP9_LOS
W11	SFP9_MOD_DEF0
W9	SFP9_TX_DISABLE
V13	SFP9_TX_FAULT
P7	SGMII_P_VDD1P0
T3	SGMII_R_VDD1P0
V3	SGMII_RDN1
P3	SGMII_RDN2
L1	SGMII_RDN3
W3	SGMII_RDP1
R3	SGMII_RDP2
M1	SGMII_RDP3
L5	SGMII_REFCLKN
M5	SGMII_REFCLKP
T2	SGMII_T_VDD1P0
U1	SGMII_TDN1
P1	SGMII_TDN2
L3	SGMII_TDN3
V1	SGMII_TDP1

Ball No.	Ball Name
R1	SGMII_TDP2
M3	SGMII_TDP3
N4	SGMII_TESTN
P4	SGMII_TESTP
AA16	SS0
Y18	SS1
W17	SS2
AA10	SYNCE_RECOV_CLK_VALID0
AB12	SYNCE_RECOV_CLK_VALID1
AA11	SYNCE_RECOV_CLK0
AB11	SYNCE_RECOV_CLK1
AA12	SYNCE_REFCLKOUT
Y12	SYNCE_REFCLKOUT_VALID
AA9	SYNCIN_1588
AB9	SYNCOUT_1588
V18	TCK
T18	TDI
A15	TDN_PHY0_CH0
B15	TDN_PHY0_CH1
C15	TDN_PHY0_CH2
D15	TDN_PHY0_CH3
D18	TDN_PHY1_CH0
C18	TDN_PHY1_CH1
B18	TDN_PHY1_CH2
A18	TDN_PHY1_CH3
A20	TDN_PHY2_CH0
B21	TDN_PHY2_CH1
C21	TDN_PHY2_CH2
D21	TDN_PHY2_CH3
F22	TDN_PHY3_CH0
E21	TDN_PHY3_CH1
E20	TDN_PHY3_CH2
E19	TDN_PHY3_CH3
B3	TDN_PHY4_CH0
C1	DNP
B1	DNP
A3	DNP
A6	DNP

Ball No.	Ball Name
B6	DNP
C6	DNP
C8	DNP
D9	DNP
C9	DNP
B9	DNP
A9	DNP
A12	DNP
B12	DNP
C12	DNP
D12	DNP
U18	TDO
A16	TDP_PHY0_CH0
B16	TDP_PHY0_CH1
C16	TDP_PHY0_CH2
D16	TDP_PHY0_CH3
D19	TDP_PHY1_CH0
C19	TDP_PHY1_CH1
B19	TDP_PHY1_CH2
A19	TDP_PHY1_CH3
A21	TDP_PHY2_CH0
B22	TDP_PHY2_CH1
C22	TDP_PHY2_CH2
D22	TDP_PHY2_CH3
E22	TDP_PHY3_CH0
F21	TDP_PHY3_CH1
F20	TDP_PHY3_CH2
F19	TDP_PHY3_CH3
C3	TDP_PHY4_CH0
C2	DNP
B2	DNP
A2	DNP
A7	DNP
B7	DNP
C7	DNP
B8	DNP
D10	DNP
C10	DNP
B10	DNP
A10	DNP
A13	DNP
B13	DNP

Ball No.	Ball Name
C13	DNP
D13	DNP
N5	TESTMODE_0
P5	TESTMODE_1
T5	TESTMODE_2
T7	TESTMODE_3
T9	TESTMODE_4
V20	TMS
V19	TRST_L
G7	VDDC_1P0
G8	VDDC_1P0
G13	VDDC_1P0
G14	VDDC_1P0
L10	VDDC_1P0
M16	VDDC_1P0
N16	VDDC_1P0
R5	VDDC_1P0
R16	VDDC_1P0
T11	VDDC_1P0
T12	VDDC_1P0
T13	VDDC_1P0
T14	VDDC_1P0
T16	VDDC_1P0
L13	VDDO_3P3
L14	VDDO_3P3
L9	VDDP_1P8
R10	VDDP_1P8
A1	VSS
A5	VSS
A22	VSS
B11	VSS
B14	VSS
B17	VSS
B20	VSS
C14	VSS
D1	VSS
D2	VSS
D3	VSS
D6	VSS
D8	VSS
D11	VSS
D14	VSS

Ball No.	Ball Name
D17	VSS
D20	VSS
E2	VSS
E4	VSS
E8	VSS
E10	VSS
E13	VSS
E14	VSS
E15	VSS
E16	VSS
F2	VSS
F4	VSS
F6	VSS
F18	VSS
G1	VSS
G2	VSS
G3	VSS
G4	VSS
G5	VSS
G9	VSS
G11	VSS
G12	VSS
G15	VSS
G18	VSS
G19	VSS
G20	VSS
G21	VSS
H2	VSS
H4	VSS
H7	VSS
H8	VSS
H9	VSS
H12	VSS
H13	VSS
H14	VSS
H15	VSS
J2	VSS
J4	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS

Ball No.	Ball Name
J12	VSS
J13	VSS
J14	VSS
J15	VSS
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K14	VSS
K15	VSS
K16	VSS
L2	VSS
L4	VSS
L7	VSS
L8	VSS
L11	VSS
L12	VSS
L15	VSS
L16	VSS
M2	VSS
M4	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
N1	VSS
N2	VSS

Ball No.	Ball Name
N3	VSS
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N20	VSS
P2	VSS
P8	VSS
P9	VSS
P10	VSS
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
R2	VSS
R4	VSS
R7	VSS
R8	VSS
R9	VSS

Ball No.	Ball Name
R11	VSS
R12	VSS
R13	VSS
R14	VSS
T1	VSS
T4	VSS
T10	VSS
U2	VSS
U3	VSS
U4	VSS
V2	VSS
V4	VSS
V6	VSS
W1	VSS
W2	VSS
W4	VSS
W6	VSS
W18	VSS
Y2	VSS
Y3	VSS
Y4	VSS
Y6	VSS
Y7	VSS
Y14	VSS
AA2	VSS
AA4	VSS

Ball No.	Ball Name
AA7	VSS
AA8	VSS
AB1	VSS
AB2	VSS
AB4	VSS
AB8	VSS
AB22	VSS
E3	DNP
H3	DNP
F3	DNP
J3	DNP
E5	DNP
F5	DNP
K5	XFI_T_R_VDD1P0
E1	DNP
H1	DNP
F1	DNP
J1	DNP
H5	DNP
J5	DNP
J7	XFI0_P_VDD1P0
K7	XFI1_P_VDD1P0
AA6	XTAL_AVDD
AB5	XTAL_CML_N
AA5	XTAL_CML_P
AB6	XTALN
AB7	XTALP

7.3 Pin List by Pin Number (13×13 mm^2) (BCM53156/BCM53158)

Ball No.	Ball Name
A1	VSS
A2	TDN_PHY5_CH3
A3	TDN_PHY5_CH2
A4	TDN_PHY5_CH1
A5	TDN_PHY5_CH0
A6	TDP_PHY6_CH0
A7	TDP_PHY6_CH1
A8	TDP_PHY6_CH2
A9	TDP_PHY6_CH3
A10	TDN_PHY7_CH3
A11	TDN_PHY7_CH2

Ball No.	Ball Name
A12	TDN_PHY7_CH1
A13	TDN_PHY7_CH0
A14	TDP_PHY0_CH0
A15	TDP_PHY0_CH1
A16	TDP_PHY0_CH2
A17	TDN_PHY0_CH3
A18	TDP_PHY1_CH3
A19	VSS
B1	TDN_PHY4_CH3
B2	TDP_PHY5_CH3
B3	TDP_PHY5_CH2

Ball No.	Ball Name
B4	TDP_PHY5_CH1
B5	TDP_PHY5_CH0
B6	TDN_PHY6_CH0
B7	TDN_PHY6_CH1
B8	TDN_PHY6_CH2
B9	TDN_PHY6_CH3
B10	TDP_PHY7_CH3
B11	TDP_PHY7_CH2
B12	TDP_PHY7_CH1
B13	TDP_PHY7_CH0
B14	TDN_PHY0_CH0

Ball No.	Ball Name
B15	TDN_PHY0_CH1
B16	TDN_PHY0_CH2
B17	TDP_PHY0_CH3
B18	TDN_PHY1_CH3
B19	TDN_PHY1_CH2
C1	TDP_PHY4_CH3
C2	TDN_PHY4_CH2
C3	TDP_PHY4_CH2
C4	PHY_RDC2
C5	AVDD3P3_PHY_4
C6	AVDD3P3_PHY_4

Ball No.	Ball Name
C7	VSS
C8	VSS
C9	VSS
C10	VSS
C11	VSS
C12	VSS
C13	VSS
C14	AVDD3P3_PHY_0
C15	VSS
C16	PHY_RDC1
C17	TDP_PHY1_CH1
C18	TDN_PHY1_CH1
C19	TDP_PHY1_CH2
D1	DNP
D2	TDN_PHY4_CH1
D3	TDP_PHY4_CH1
D4	VSS
D5	BVDD3P3_2
D6	VSS
D7	VSS
D8	PHYPLL_VDD1P0_2
D9	AVDD1P0_PHY_4
D10	VSS
D11	AVDD1P0_PHY_0
D12	PHYPLL_VDD1P0_1
D13	VSS
D14	BVDD3P3_1
D15	AVDD3P3_PHY_0
D16	VSS
D17	TDN_PHY1_CH0
D18	TDP_PHY1_CH0
D19	DNP
E1	TDN_PHY4_CH0
E2	TDP_PHY4_CH0
E3	VSS
E4	VSS
E5	VSS
E6	DNP
E7	DNP
E8	DNP
E9	DNP
E10	DNP

Ball No.	Ball Name
E11	DNP
E12	DNP
E13	DNP
E14	DNP
E15	DNP
E16	TDN_PHY2_CH1
E17	TDP_PHY2_CH1
E18	TDP_PHY2_CH0
E19	TDN_PHY2_CH0
F1	VSS
F2	VSS
F3	VSS
F4	XFI_P_VDD1P0
F5	DNP
F6	VDDC_1P0
F7	VSS
F8	VDDC_1P0
F9	VSS
F10	VDDC_1P0
F11	VDDC_1P0
F12	VDDC_1P0
F13	VSS
F14	VSS
F15	DNP
F16	VSS
F17	TDN_PHY2_CH3
F18	DNP
F19	DNP
G1	XFI_TDP0
G2	XFI_TDN0
G3	VSS
G4	XFI_TESTP
G5	DNP
G6	VDDC_1P0
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	VSS
G13	VSS
G14	LED_5

Ball No.	Ball Name
G15	DNP
G16	LED_0
G17	TDP_PHY2_CH3
G18	TDN_PHY2_CH2
G19	TDP_PHY2_CH2
H1	VSS
H2	VSS
H3	VSS
H4	XFI_TESTN
H5	DNP
H6	VSS
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VSS
H13	VSS
H14	LED_6
H15	DNP
H16	LED_1
H17	TDN_PHY3_CH3
H18	TDP_PHY3_CH3
H19	DNP
J1	XFI_RDN0
J2	XFI_RDP0
J3	VSS
J4	XFI_R_VDD1P0
J5	DNP
J6	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VSS
J14	VSS
J15	DNP
J16	LED_2
J17	TDN_PHY3_CH2
J18	TDP_PHY3_CH2

Ball No.	Ball Name
J19	TDN_PHY3_CH1
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K5	DNP
K6	VSS
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K14	VSS
K15	DNP
K16	LED_3
K17	TDP_PHY3_CH0
K18	TDN_PHY3_CH0
K19	TDP_PHY3_CH1
L1	XFI_TDN1
L2	XFI_TDP1
L3	VSS
L4	XFI_REFCLKP
L5	DNP
L6	VDDP_1P8
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VSS
L14	VDDO_3P3
L15	DNP
L16	LED_4
L17	VSS
L18	VSS
L19	DNP
M1	VSS
M2	VSS
M3	VSS

Ball No.	Ball Name
M4	XFI_REFCLKN
M5	DNP
M6	VDDP_1P8
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M14	VDDO_3P3
M15	DNP
M16	VDDC_1P0
M17	MFIO8
M18	MFIO4
M19	MFIO3
N1	XFI_RDP1
N2	XFI_RDN1
N3	VSS
N4	TESTMODE_0
N5	DNP
N6	VSS
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	DNP
N16	VDDC_1P0
N17	MFIO7
N18	MFIO5
N19	MFIO2
P1	VSS
P2	VSS
P3	VSS
P4	SGMII_P_VDD1P0
P5	DNP
P6	REXT
P7	VSS

Ball No.	Ball Name
P8	VDDC_1P0
P9	VDDC_1P0
P10	VDDC_1P0
P11	VSS
P12	JTCE_0
P13	JTCE_1
P14	VSS
P15	DNP
P16	MFIO6
P17	MFIO0
P18	MFIO1
P19	DNP
R1	QSGMII_RDP0
R2	QSGMII_RDN0
R3	TESTMODE_1
R4	SGMII_R_VDD1P0
R5	DNP
R6	DNP
R7	DNP
R8	DNP
R9	DNP
R10	DNP
R11	DNP
R12	DNP
R13	DNP
R14	DNP
R15	DNP
R16	INTR_L
R17	IMP_VDDO
R18	IMP_VDDP
R19	IMP_VOL_REF
T1	VSS
T2	VSS
T3	TESTMODE_2
T4	TESTMODE_3
T5	VSS
T6	LDO_VOUT
T7	LDO_AVDD
T8	VSS
T9	VDDC_1P0
T10	MDIO_VDDO
T11	MDIO_VDDP

Ball No.	Ball Name
T12	VDDC_1P0
T13	VDDC_1P0
T14	TDI
T15	TMS
T16	RESET_L
T17	IMP_RXDV
T18	IMP_TXD3
T19	IMP_TXCLK
U1	QSGMII_TDN0
U2	QSGMII_TDP0
U3	VSS
U4	XTAL_CML_P
U5	PLL_AVDD
U6	XTAL_AVDD
U7	PVTMON_ADC
U8	TESTMODE_4
U9	MDC
U10	MDIO
U11	MOSI1
U12	MOSI2
U13	SS2
U14	TDO
U15	TCK
U16	IMP_RXD1

Ball No.	Ball Name
U17	IMP_RXD3
U18	IMP_TXD2
U19	DNP
V1	VSS
V2	VSS
V3	VSS
V4	XTAL_CML_N
V5	VSS
V6	VSS
V7	PVTMON_DAC
V8	DATA0
V9	DATA2
V10	SCK0
V11	SS1

Ball No.	Ball Name
V12	SCK1
V13	MISO2
V14	TRST_L
V15	LED_26_SLED_CLK
V16	IMP_RXD0
V17	IMP_RXD2
V18	IMP_TXD1
V19	IMP_TXD0
W1	VSS
W2	PLL_TESTN
W3	PLL_TESTP
W4	VSS
W5	XTALN

Ball No.	Ball Name
W6	XTALP
W7	VSS
W8	DATA1
W9	DATA3
W10	DNP
W11	SS0
W12	MISO1
W13	DNP
W14	SCK2
W15	LED_27_SLED_DATA
W16	DNP
W17	IMP_RXCLK
W18	IMP_TXEN
W19	VSS

7.4 Pin List by Pin Name (13×13 mm^2) (BCM53156/BCM53158)

Ball No.	Ball Name
D11	AVDD1P0_PHY_0
D9	AVDD1P0_PHY_4
C14	AVDD3P3_PHY_0
D15	AVDD3P3_PHY_0
C5	AVDD3P3_PHY_4
C6	AVDD3P3_PHY_4
D14	BVDD3P3_1
D5	BVDD3P3_2
V8	DATA0
W8	DATA1
V9	DATA2
W9	DATA3
D1	DNP
D19	DNP
E6	DNP
E7	DNP
E8	DNP
E9	DNP
E10	DNP
E11	DNP
E12	DNP
E13	DNP
E14	DNP
E15	DNP
F5	DNP
F15	DNP
F18	DNP
F19	DNP
G5	DNP
G15	DNP
H5	DNP
H15	DNP
H19	DNP
J5	DNP
J15	DNP
K5	DNP
K15	DNP
L5	DNP
L15	DNP
L19	DNP
M5	DNP

Ball No.	Ball Name
M15	DNP
N5	DNP
N15	DNP
P5	DNP
P15	DNP
P19	DNP
R5	DNP
R6	DNP
R7	DNP
R8	DNP
R9	DNP
R10	DNP
R11	DNP
R12	DNP
R13	DNP
R14	DNP
R15	DNP
U19	DNP
W10	DNP
W13	DNP
W16	DNP
W17	IMP_RXCLK
V16	IMP_RXD0
U16	IMP_RXD1
V17	IMP_RXD2
U17	IMP_RXD3
T17	IMP_RXDV
T19	IMP_TXCLK
V19	IMP_TXD0
V18	IMP_TXD1
U18	IMP_TXD2
T18	IMP_TXD3
W18	IMP_TXEN
R17	IMP_VDDO
R18	IMP_VDDP
R19	IMP_VOL_REF
R16	INTR_L
P12	JTCE_0
P13	JTCE_1
T7	LDO_AVDD
T6	LDO_VOUT

Ball No.	Ball Name
G16	LED_0
H16	LED_1
J16	LED_2
V15	LED_26_SLED_CLK
W15	LED_27_SLED_DATA
K16	LED_3
L16	LED_4
G14	LED_5
H14	LED_6
U9	MDC
U10	MDIO
T10	MDIO_VDDO
T11	MDIO_VDDP
P17	MFIO0
P18	MFIO1
N19	MFIO2
M19	MFIO3
M18	MFIO4
N18	MFIO5
P16	MFIO6
N17	MFIO7
M17	MFIO8
W12	MISO1
V13	MISO2
U11	MOSI1
U12	MOSI2
C16	PHY_RDC1
C4	PHY_RDC2
D12	PHYPLL_VDD1P0_1
D8	PHYPLL_VDD1P0_2
U5	PLL_AVDD
W2	PLL_TESTN
W3	PLL_TESTP
U7	PVTMON_ADC
V7	PVTMON_DAC
R2	QSGMII_RDN0
R1	QSGMII_RDP0
U1	QSGMII_TDN0
U2	QSGMII_TDP0
T16	RESET_L

Ball No.	Ball Name
P6	REXT
V10	SCK0
V12	SCK1
W14	SCK2
P4	SGMII_P_VDD1P0
R4	SGMII_R_VDD1P0
W11	SS0
V11	SS1
U13	SS2
U15	TCK
T14	TDI
B14	TDN_PHY0_CH0
B15	TDN_PHY0_CH1
B16	TDN_PHY0_CH2
A17	TDN_PHY0_CH3
D17	TDN_PHY1_CH0
C18	TDN_PHY1_CH1
B19	TDN_PHY1_CH2
B18	TDN_PHY1_CH3
E19	TDN_PHY2_CH0
E16	TDN_PHY2_CH1
G18	TDN_PHY2_CH2
F17	TDN_PHY2_CH3
K18	TDN_PHY3_CH0
J19	TDN_PHY3_CH1
J17	TDN_PHY3_CH2
H17	TDN_PHY3_CH3
E1	TDN_PHY4_CH0
D2	TDN_PHY4_CH1
C2	TDN_PHY4_CH2
B1	TDN_PHY4_CH3
A5	TDN_PHY5_CH0
A4	TDN_PHY5_CH1
A3	TDN_PHY5_CH2
A2	TDN_PHY5_CH3
B6	TDN_PHY6_CH0
B7	TDN_PHY6_CH1
B8	TDN_PHY6_CH2
B9	TDN_PHY6_CH3
A13	TDN_PHY7_CH0
A12	TDN_PHY7_CH1

Ball No.	Ball Name
A11	TDN_PHY7_CH2
A10	TDN_PHY7_CH3
U14	TDO
A14	TDP_PHY0_CH0
A15	TDP_PHY0_CH1
A16	TDP_PHY0_CH2
B17	TDP_PHY0_CH3
D18	TDP_PHY1_CH0
C17	TDP_PHY1_CH1
C19	TDP_PHY1_CH2
A18	TDP_PHY1_CH3
E18	TDP_PHY2_CH0
E17	TDP_PHY2_CH1
G19	TDP_PHY2_CH2
G17	TDP_PHY2_CH3
K17	TDP_PHY3_CH0
K19	TDP_PHY3_CH1
J18	TDP_PHY3_CH2
H18	TDP_PHY3_CH3
E2	TDP_PHY4_CH0
D3	TDP_PHY4_CH1
C3	TDP_PHY4_CH2
C1	TDP_PHY4_CH3
B5	TDP_PHY5_CH0
B4	TDP_PHY5_CH1
B3	TDP_PHY5_CH2
B2	TDP_PHY5_CH3
A6	TDP_PHY6_CH0
A7	TDP_PHY6_CH1
A8	TDP_PHY6_CH2
A9	TDP_PHY6_CH3
B13	TDP_PHY7_CH0
B12	TDP_PHY7_CH1
B11	TDP_PHY7_CH2
B10	TDP_PHY7_CH3
N4	TESTMODE_0
R3	TESTMODE_1
T3	TESTMODE_2
T4	TESTMODE_3
U8	TESTMODE_4
T15	TMS
V14	TRST_L

Ball No.	Ball Name
F6	VDDC_1P0
F8	VDDC_1P0
F10	VDDC_1P0
F11	VDDC_1P0
F12	VDDC_1P0
G6	VDDC_1P0
M16	VDDC_1P0
N16	VDDC_1P0
P8	VDDC_1P0
P9	VDDC_1P0
P10	VDDC_1P0
T9	VDDC_1P0
T12	VDDC_1P0
T13	VDDC_1P0
L14	VDDO_3P3
M14	VDDO_3P3
L6	VDDP_1P8
M6	VDDP_1P8
A1	VSS
A19	VSS
C7	VSS
C8	VSS
C9	VSS
C10	VSS
C11	VSS
C12	VSS
C13	VSS
C15	VSS
D4	VSS
D6	VSS
D7	VSS
D10	VSS
D13	VSS
D16	VSS
E3	VSS
E4	VSS
E5	VSS
F1	VSS
F2	VSS
F3	VSS
F7	VSS
F9	VSS

Ball No.	Ball Name
F13	VSS
F14	VSS
F16	VSS
G3	VSS
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	VSS
G13	VSS
H1	VSS
H2	VSS
H3	VSS
H6	VSS
H7	VSS
H8	VSS
H9	VSS

Ball No.	Ball Name
H10	VSS
H11	VSS
H12	VSS
H13	VSS
J3	VSS
J6	VSS
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VSS
J14	VSS
K1	VSS
K2	VSS
K3	VSS
K4	VSS
K6	VSS
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K14	VSS
L3	VSS
L7	VSS
L8	VSS
L9	VSS
L10	VSS
L11	VSS

Ball No.	Ball Name
L12	VSS
L13	VSS
L17	VSS
L18	VSS
M1	VSS
M2	VSS
M3	VSS
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
N3	VSS
N6	VSS
N7	VSS
N8	VSS
N9	VSS
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
P1	VSS
P2	VSS
P3	VSS
P7	VSS
P11	VSS
P14	VSS
T1	VSS
T2	VSS
T5	VSS

Ball No.	Ball Name
T8	VSS
U3	VSS
V1	VSS
V2	VSS
V3	VSS
V5	VSS
V6	VSS
W1	VSS
W4	VSS
W7	VSS
W19	VSS
F4	XFI_P_VDD1P0
J4	XFI_R_VDD1P0
J1	XFI_RDN0
N2	XFI_RDN1
J2	XFI_RDP0
N1	XFI_RDP1
M4	XFI_REFCLKN
L4	XFI_REFCLKP
G2	XFI_TDN0
L1	XFI_TDN1
G1	XFI_TDP0
L2	XFI_TDP1
H4	XFI_TESTN
G4	XFI_TESTP
U6	XTAL_AVDD
V4	XTAL_CML_N
U4	XTAL_CML_P
W5	XTALN
W6	XTALP

7.5 Ball Map (19×19 mm^2 Package) (BCM53154)

Figure 31: Ball Map (19×19 mm^2 Package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	DNP	DNP	I2C_SCL	VSS	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	TDN_PHY0_CH0	TDP_PHY0_CH0	DNP	TDN_PHY1_CH3	TDP_PHY1_CH3	TDN_PHY2_CH0	TDP_PHY2_CH0	VSS	A
B	DNP	DNP	DNP	I2C_SDA9	I2C_SDA10	DNP	DNP	DNP	DNP	DNP	VSS	DNP	DNP	VSS	TDN_PHY0_CH1	TDP_PHY0_CH1	VSS	TDN_PHY1_CH2	TDP_PHY1_CH2	VSS	TDN_PHY2_CH1	TDP_PHY2_CH1	B
C	DNP	DNP	DNP	I2C_SDA11	I2C_SDA12	DNP	DNP	DNP	DNP	DNP	PLL_TVCO_2	DNP	DNP	VSS	TDN_PHY0_CH2	TDP_PHY0_CH2	PHY_RDC1	TDN_PHY1_CH1	TDP_PHY1_CH1	PLL_TVCO_1	TDN_PHY2_CH2	TDP_PHY2_CH2	C
D	VSS	VSS	VSS	DNP	DNP	VSS	I2C_SDA13	VSS	DNP	DNP	VSS	DNP	DNP	VSS	TDN_PHY0_CH3	TDP_PHY0_CH3	VSS	TDN_PHY1_CH0	TDP_PHY1_CH0	VSS	TDN_PHY2_CH3	TDP_PHY2_CH3	D
E	DNP	VSS	DNP	VSS	DNP	DNP	I2C_SDA8	VSS	PHY_RDC2	VSS	PHY_PLL_VDD1P0_2	AVDD1P0_PHY_4	VSS	VSS	VSS	VSS	PHY_PLL_VDD1P0_1	AVDD1P0_PHY_0	TDN_PHY3_CH3	TDN_PHY3_CH2	TDN_PHY3_CH1	TDP_PHY3_CH0	E
F	DNP	VSS	DNP	VSS	DNP	VSS	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	VSS	TDP_PHY3_CH3	TDP_PHY3_CH2	TDP_PHY3_CH1	TDN_PHY3_CH0	F
G	VSS	VSS	VSS	VSS	VSS	DNP	VDDC_1P0	VDDC_1P0	VSS	BVDD3P3_2	VSS	VSS	VDDC_1P0	VDDC_1P0	VSS	BVDD3P3_1	DNP	VSS	VSS	VSS	VSS	DNP	G
H	DNP	VSS	DNP	VSS	DNP	DNP	VSS	VSS	VSS	AVDD3P3_PHY_4	AVDD3P3_PHY_4	VSS	VSS	VSS	VSS	AVDD3P3_PHY_0	DNP	LED_1	LED_0	LED_3	LED_2	LED_4	H
J	DNP	VSS	DNP	VSS	DNP	DNP	XFI0_P_VDD1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD3P3_PHY_0	DNP	LED_5	LED_7	LED_6	LED_8	LED_9	J
K	VSS	VSS	VSS	VSS	XFI_T_R_VDD1P0	DNP	XFI1_P_VDD1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DNP	LED_10	LED_11	LED_12	LED_13	DNP	K
L	DNP	VSS	DNP	VSS	SGMII_REFCLKN	DNP	VSS	VSS	VDDP_1P8	VDDC_1P0	VSS	VSS	VDDO_3P3	VDDO_3P3	VSS	VSS	DNP	LED_14	LED_15	LED_16	LED_17	LED_18	L
M	DNP	VSS	DNP	VSS	SGMII_REFCLKP	DNP	REXT	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC_1P0	DNP	LED_19	LED_20	LED_21	LED_22	LED_23	M
N	VSS	VSS	VSS	SGMII_TESTN	TESTMODE_0	DNP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDC_1P0	DNP	LED_24	LED_25	VSS	MFIO15	DNP	N
P	DNP	VSS	DNP	SGMII_TESTP	TESTMODE_1	DNP	SGMII_P_VDD1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DNP	JTCE_0	INTR_L	MFIO14	MFIO13	MFIO12	P
R	DNP	VSS	DNP	VSS	VDDC_1P0	DNP	VSS	VSS	VSS	VDDP_1P8	VSS	VSS	VSS	VSS	IMP_VDDP	VDDC_1P0	DNP	JTCE_1	RESET_L	MFIO11	MFIO10	MFIO9	R
T	VSS	SGMII_T_VDD1P0	SGMII_R_VDD1P0	VSS	TESTMODE_2	DNP	TESTMODE_3	PLL_AVDD	TESTMODE_4	VSS	VDDC_1P0	VDDC_1P0	VDDC_1P0	VDDC_1P0	IMP_VDDO	VDDC_1P0	DNP	TDI	MFIO8	MFIO7	MFIO6	DNP	T
U	DNP	VSS	VSS	VSS	LCPLL_FREFN	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	TDO	MFIO5	MFIO4	MFIO3	MFIO2	U
V	DNP	VSS	DNP	VSS	LCPLL_FREFP	VSS	LDO_AVDD	LDO_VOUT	SFP8_TX_FAULT	SFP8_TX_DISABLE	SFP8_LOS	SFP8_MOD_DEF0	SFP9_TX_FAULT	MDIO_VDDP	MDIO_VDDO	SCK2	MOSI2	TCK	TRST_L	TMS	MFIO1	MFIO0	V
W	VSS	VSS	DNP	VSS	PLL_TESTN	VSS	LDO_VSENSE	PVTMON_ADC	SFP9_TX_DISABLE	SFP9_LOS	SFP9_MOD_DEF0	SFP10_TX_FAULT	SFP10_TX_DISABLE	MDC	MDIO	MISO2	SS2	VSS	IMP_VOL_REF	IMP_RXD0	IMP_RXCLK	DNP	W
Y	Q_SGMII_TDN0	VSS	VSS	VSS	PLL_TESTP	VSS	VSS	PVTMON_DAC	SFP10_LOS	SFP10_MOD_DEF0	SFP11_TX_FAULT	SYNCE_REFCLKOUT_VALID	SFP11_TX_DISABLE	VSS	DATA3	DATA2	MISO1	SS1	IMP_RXDV	IMP_RXD1	IMP_RXD2	IMP_RXD3	Y
AA	Q_SGMII_TDP0	VSS	Q_SGMII_RDN0	VSS	XTAL_CML_P	XTAL_AVDD	VSS	VSS	SYNCIN_1588	SYNCE_RECOV_CLK_VALID0	SYNCE_RECOV_CLK0	SYNCE_REFCLKOUT	SFP11_LOS	SFP11_MOD_DEF0	DATA1	SS0	MOSI1	LED_26_SCLK	IMP_TXEN	IMP_TXD1	IMP_TXD3	IMP_TXCLK	AA
AB	VSS	VSS	Q_SGMII_RDP0	VSS	XTAL_CML_N	XTALN	XTALP	VSS	SYNCOUT_1588	DNP	SYNCE_RECOV_CLK1	SYNCE_RECOV_CLK_VALID1	DNP	SCK0	DATA0	DNP	SCK1	LED_27_SDATA	DNP	IMP_TXD0	IMP_TXD2	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

7.6 Ball Map (13×13 mm^2 Package) (BCM53156/BCM53158)

Figure 32: Ball Map (13×13 mm^2 Package)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	VSS	TDN_PHY5_CH3	TDN_PHY5_CH2	TDN_PHY5_CH1	TDN_PHY5_CH0	TDP_PHY6_CH0	TDP_PHY6_CH1	TDP_PHY6_CH2	TDP_PHY6_CH3	TDN_PHY7_CH3	TDN_PHY7_CH2	TDN_PHY7_CH1	TDN_PHY7_CH0	TDP_PHY0_CH0	TDP_PHY0_CH1	TDP_PHY0_CH2	TDP_PHY0_CH3	TDP_PHY1_CH3	VSS	A
B	TDN_PHY4_CH3	TDP_PHY5_CH3	TDP_PHY5_CH2	TDP_PHY5_CH1	TDP_PHY5_CH0	TDN_PHY6_CH0	TDN_PHY6_CH1	TDN_PHY6_CH2	TDN_PHY6_CH3	TDP_PHY7_CH3	TDP_PHY7_CH2	TDP_PHY7_CH1	TDP_PHY7_CH0	TDN_PHY0_CH0	TDN_PHY0_CH1	TDN_PHY0_CH2	TDN_PHY0_CH3	TDN_PHY1_CH3	TDN_PHY1_CH2	B
C	TDP_PHY4_CH3	TDN_PHY4_CH2	TDP_PHY4_CH2	PHY_RDC2	AVDD3P3_PHY_4	AVDD3P3_PHY_4	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AVDD3P3_PHY_0	VSS	PHY_RDC1	TDP_PHY1_CH1	TDN_PHY1_CH1	TDP_PHY1_CH2	C
D	DNP	TDN_PHY4_CH1	TDP_PHY4_CH1	VSS	BVDD3P3_2	VSS	VSS	PHYPLL_VDD1P0_2	AVDD1P0_PHY_4	VSS	AVDD1P0_PHY_0	PHYPLL_VDD1P0_1	VSS	BVDD3P3_1	AVDD3P3_PHY_0	VSS	TDN_PHY1_CH0	TDP_PHY1_CH0	DNP	D
E	TDN_PHY4_CH0	TDP_PHY4_CH0	VSS	VSS	VSS	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	TDN_PHY2_CH1	TDP_PHY2_CH1	TDP_PHY2_CH0	TDN_PHY2_CH0	E
F	VSS	VSS	VSS	XFI_P_VDD1P0	DNP	VDDC_1P0	VSS	VDDC_1P0	VSS	VDDC_1P0	VDDC_1P0	VDDC_1P0	VSS	VSS	DNP	VSS	TDN_PHY2_CH3	DNP	DNP	F
G	XFI_TDP0	XFI_TDN0	VSS	XFI_TESTP	DNP	VDDC_1P0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	LED_5	DNP	LED_0	TDP_PHY2_CH3	TDN_PHY2_CH2	TDP_PHY2_CH2	G
H	VSS	VSS	VSS	XFI_TESTN	DNP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	LED_6	DNP	LED_1	TDN_PHY3_CH3	TDP_PHY3_CH3	DNP	H
J	XFI_RDN0	XFI_RDP0	VSS	XFI_R_VDD1P0	DNP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DNP	LED_2	TDN_PHY3_CH2	TDP_PHY3_CH2	TDN_PHY3_CH1	J
K	VSS	VSS	VSS	VSS	DNP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DNP	LED_3	TDP_PHY3_CH0	TDN_PHY3_CH0	TDP_PHY3_CH1	K
L	XFI_TDN1	XFI_TDP1	VSS	XFI_REFCLKP	DNP	VDDP_1P8	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_3P3	DNP	LED_4	VSS	VSS	DNP	L
M	VSS	VSS	VSS	XFI_REFCLKN	DNP	VDDP_1P8	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_3P3	DNP	VDDC_1P0	MFIO8	MFIO4	MFIO3	M
N	XFI_RDP1	XFI_RDN1	VSS	TESTMODE_0	DNP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DNP	VDDC_1P0	MFIO7	MFIO5	MFIO2	N
P	VSS	VSS	VSS	SGMII_P_VDD1P0	DNP	REXT	VSS	VDDC_1P0	VDDC_1P0	VDDC_1P0	VSS	JTCE_0	JTCE_1	VSS	DNP	MFIO6	MFIO0	MFIO1	DNP	P
R	QSGMII_RDP0	QSGMII_RDN0	TESTMODE_1	SGMII_R_VDD1P0	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	DNP	INTR_L	IMP_VDDO	IMP_VDDP	IMP_VOL_REF	R
T	VSS	VSS	TESTMODE_2	TESTMODE_3	VSS	LDO_VOUT	LDO_AVDD	VSS	VDDC_1P0	MDIO_VDDO	MDIO_VDDP	VDDC_1P0	VDDC_1P0	TDI	TMS	RESET_L	IMP_RXDV	IMP_TXD3	IMP_TXCLK	T
U	QSGMII_TDN0	QSGMII_TDP0	VSS	XTAL_CML_P	PLL_AVDD	XTAL_AVDD	PVTMON_ADC	TESTMODE_4	MDC	MDIO	MOSI1	MOSI2	SS2	TDO	TCK	IMP_RXD1	IMP_RXD3	IMP_TXD2	DNP	U
V	VSS	VSS	VSS	XTAL_CML_N	VSS	VSS	PVTMON_DAC	DATA0	DATA2	SCK0	SS1	SCK1	MISO2	TRST_L	LED_26_SLED_CLK	IMP_RXD0	IMP_RXD2	IMP_TXD1	IMP_TXD0	V
W	VSS	PLL_TESTN	PLL_TESTP	VSS	XTALN	XTALP	VSS	DATA1	DATA3	DNP	SS0	MISO1	DNP	SCK2	LED_27_SLED_DATA	DNP	IMP_RXCLK	IMP_TXEN	VSS	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Chapter 8: Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 43: Absolute Maximum Ratings[a]

Parameter	Symbol	Min.	Max.	Unit
3.3V Supply Voltage	VDDO_3P3, AVDD3P3_PHY0, AVDD3P3_PHY1 AVDD3P3_PHY2, AVDD3P3_PHY3, BVDD3P3 LDO_AVDD, MDIO_VDDO[b]	–0.5	+3.63	V
2.5V Supply Voltage	IMP_VDDO[c]	–0.5	+2.75	V
1.5V Supply Voltage	IMP_VDDO[c], IMP_VDDP[c]	–0.5	+1.65	V
1.8V Supply Voltage	VDDP_1P8, OTP_VDD, AVDD_PVTMON, PLL_VDD1P8, XTAL_VDD1P8, UPI_VDD18 UPI_VDD18_int IMP_VDDP[c], MDIO_VDDP[b]	–0.5	+1.98	V
1.2V Supply Voltage	DDR_VDDO, DDR_VDDO_CK MDIO_VDDO[b],MDIO_VDDP[b]	–0.5	+1.32	V
1.0V Supply Voltage	VDDC_1P0, AVDD1P0_PHY0, AVDD1P0_PHY1 AVDD1P0_PHY2, AVDD1P0_PHY3, PHYPLL_VDD1P0, QSGMII_P_R_VDD1P0 QSGMII_T_VDD1P0, XFI_P_R_VDD1P0 XFI_T_VDD1P0, RESCAL_pad_i_VDD1p0	–0.5	+1.1	V
Maximum Junction Temperature	T_{J_MAX}	–	+110	°C
Commercial Ambient Temperature (Operating)	T_A	0	+70	°C
Industrial Ambient Temperature (Operating)	T_A	–40	+85	°C
Operating Humidity	–	–	+85	%
Storage Temperature	T_{STG}	–40	+125	°C
Storage Humidity	–	–	60	%

a. These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at maximum conditions for extended periods may adversely affect long-term reliability of the device.

b. MDC/MDIO for 3.3V/1.2V.

c. RGMII interface for 2.5V/1.5V.

8.2 Recommended Operating Conditions and DC Characteristics

NOTE: Refer to *BCM53154/BCM53156/BCM53158 Hardware Design Guide* for more information on voltage tolerances and power supplies decoupling.

NOTE: The voltage tolerances are ±3% on 1.0V/1.05V and ±5% on all other supplies. The 1.0V ±3% does not apply to VDDC_1P0 (AVS). The actual voltage level and tolerance on the VDDC_1P0 supply is controlled by AVS. AVS is required for the device to operate properly and the voltage range is 0.85V to 1.10V.

Table 44: Recommended Operating Conditions

Symbol	Nominal Value	Description
DVDD	1.0V	1.0V core power (AVS)
AVDD0P9_PHY0	1.0V	1.0V analog power (GPHY)
AVDD0P9_PHY1	1.0V	
AVDD0P9_PHY2	1.0V	
AVDD0P9_PHY3	1.0V	
PHYPLL_VDD0P9	1.0V	1.0V PLL power for GPHY
QSGMII_P_R_VDD1P0	1.0V	1.0V power supply for QSGMII
QSGMII_T_VDD1P0	1.0V	
XFI_P_R_VDD1P0	1.0V	1.0V power supply for Eagle
XFI_T_VDD1P0	1.0V	
RESCAL_pad_i_VDD1p0	1.0V	1.0V power for RESCAL (non-AVS)
UPI_VDD18_int	1.8V	1.8V power for UPI
UPI_VDD18	1.8V	
PLL_VDD1P8	1.8V	1.8V System PLL power (for both PLL1 and LCPLL)
AVDD_PVTMON	1.8V	1.8V pvtmon power supply
XTAL_VDD1P8	1.8V	1.8V power for XTAL
OTP_VDD	1.8V	1.8V OTP power
VDDP_1P8	1.8V	1.8V general I/O VDDP power
MDIO_VDDP	1.8/1.2V	1.8V/1.2V I/O VDDP doe MDC/MDIO
RGMII_VDDP	1.8V/1.5V	1.8V/1.5V I/O VDDP for WAN port
MDIO_VDDO	3.3/1.2V	3.3/1.2V I/O power for MDC/MDIO
VDDO_3P3	3.3V	3.3V general I/O power
AVDD3P3_PHY0	3.3V	3.3V analog power (GPHY)
AVDD3P3_PHY1	3.3V	
AVDD3P3_PHY2	3.3V	
AVDD3P3_PHY3	3.3V	
BVDD3P3	3.3V	3.3V BIAS power for GPHY
LDO_AVDD	3.3V	3.3V power for LDO
RGMII_VDDO	2.5V/1.5V	2.5V/1.5V I/O power for WAN port (PAD_wan_*)

8.2.1 Standard 3.3V Signals

These specifications apply to all 3.3V signals, such as Serial Flash, MII, MFIO, I^2C, MDC/MDIO, SyncE pins, JTAG interfaces, and reset pins.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	–	–0.3	–	3.63	V
Input low voltage	V_{IL}	–	–	–	0.8	V
Input high voltage	V_{IH}	–	2.0	–	–	V
Output low voltage	V_{OL}	IOL = 4 mA	–	–	0.4	V
Output low current	I_{OL}	VOL = 0.4V	4.0	–	–	mA
Output high voltage	V_{OH}	IOH = –4 mA	2.4	–	–	V

8.2.2 Standard 2.5V Signals

These specifications apply to all 2.5V signals, such as RGMII interface.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	–	–0.3	–	2.75	V
Input low voltage	V_{IL}	–	–	–	0.8	V
Input high voltage	V_{IH}	–	1.7	–	–	V
Output low voltage	V_{OL}	–	–	–	0.4	V
Output high voltage	V_{OH}	–	2.0	–	–	V

8.2.3 REFCLK Input Timing

Table 45: REFCLK Input Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
25 MHz Crystal (XTALP/N Input)					
Frequency	C_{freq}	–	25	–	MHz
Frequency tolerance (at 25°C ± 3°C)	–	–15	–	+15	ppm
Frequency stability (over operating temperature)	–	–15	–	+15	ppm
Aging	–	–5	–	+5	ppm
ESR	–	–	–	15	ohm
Total tolerance (includes overall condition, fundamental accuracy, aging , and stability over temperature)	–	–50	–	+50	ppm
25 MHz Oscillator (XTALP Single-End CMOS Input)					
Frequency	C_{freq}	–	25	–	MHz
Bypass CMOS clock amplitude (V_{pk})	Bypass clock CMOS swing	1.4	–	1.89	Vpk
Input CMOS V_{IH}	Minimum value interpreted as logic 1	1.4	–	–	V
Input CMOS V_{IL}	Maximum value interpreted as logic 0	–	–	200	mV

Table 45: REFCLK Input Timing (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Duty cycle	–	45	–	55	%
Total tolerance (includes overall condition, fundamental accuracy, aging, and stability over temperature)	–	–50	–	+50	ppm
RMS jitter (noise bandwidth: 10 kHz to 5 MHz)	–	–	0.444	0.651	ps
RMS jitter (noise bandwidth: 10 kHz to 1 MHz)	–	–	0.281	0.392	ps
Transition time (10% to 90%)	Bypass CMOS clock transition time	–	–	500	ps
XFI Reference Clock (XFI_REFCLKP/N Differential Input)					
Frequency	C_{freq}	–	156.25	–	MHz
Accuracy	–	–50	–	+50	ppm
RMS jitter	–	–	–	0.7	ps
Rise/fall time (20% ~ 80%)	T_r/T_f	–	200	300	ps

8.2.4 SGMII DC Characteristics

Table 46: SGMII DC Characteristics

Parameter	Symbol	Min.	Max.	Unit
Output differential voltage SOUT±	V_{OD}	400	1200	mV
Input Voltage range SGIN±	V_{IN}	50	1000	mV
Input differential threshold SGIN±	V_{ID}	–	50	mV

8.2.5 SGMII Transmit Timing

Table 47: SGMII Transmit Timing

Parameter	Symbol	Min.	Max.	Unit
Fall time (20% to 80%) SGOUT±	T_F	100	200	ps
Rise time (20% to 80%) SGOUT±	T_R	100	200	ps

8.2.6 QSGMII Transmitter

Table 48: QSGMII Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud Rate	T_{Baud}	-	5.000	–	Gsym/s
Output Differential Voltage (into floating Load R_{load}=100 ohm)	T_{DIFF}	400	-	1200	mVppd
Differential Resistance	T_{RD}	80	100	120	Ohms
Recommended Output Rise and Fall Time (20% to 80%)	T_R/ T_F	30	–	–	ps
Transmitter Common-Mode Noise	TN_{CM}	–	–	5% of T_{DIFF}	mVppd
Output Current Short	T_{IS}	–	100	mA	–
Output Common-Mode Voltage	T_{CM}	735	–	1135	–

Table 48: QSGMII Transmitter (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Amplitude	–	–	–	–	–

8.2.7 QSGMII Receiver

Table 49: QSGMII Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud Rate	R_{Baud}	–	5.0	–	Gsym/s
Output Differential Voltage (into floating Load R_{load}=100 ohm)	R_{DIFF}	100	–	750	mVppd

8.2.8 XFI Transmitter Performance Specification

Figure 33: XFI Far-End Eye Mask

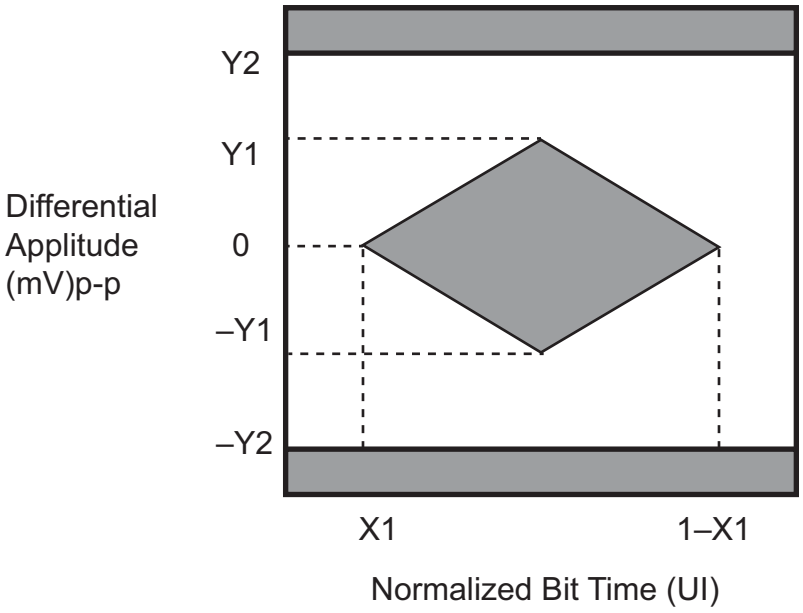


Table 50: XFI Far-End Eye Mask

Parameter	Min.	Typ.	Max.	Unit
Nominal VCO center frequency	–	10.3125	–	–
Total jitter	–	–	0.61	–
Total non-EQJ jitter	–	–	0.41	–
Eye mask X1	–	–	0.305	UI
Eye mask Y1	60	–	–	mV
Eye mask Y1	–	–	410	mV

8.2.9 XFI Transmitter DC Characteristics

Table 51: XFI Transmitter DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage, differential	V_{od1V}	0.5	1.0	1.1	V_{ptpd}
Output voltage, common mode	V_{ocm}	–	0.5	–	V
Output voltage fall time (20% to 80%)	t_{fall}	24	–	47	ps
Output voltage rise time (20% to 80%)	t_{rise}	24	–	47	ps

8.2.10 XFI Receiver Input Performance Specification

Table 52: XFI Receiver Input Performance Specification

Parameter	Min.	Typ.	Max.	Unit
Total jitter	–	–	0.65	UI
Total non-EQJ jitter	–	–	0.45	UI
Eye mask X1	–	–	0.325	UI
Eye mask Y1	55	–	–	mV
Eye mask Y2	–	–	525	mV

8.2.11 XFI Receiver DC Characteristics

Table 53: XFI Receiver DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage, differential	V_{id}	85	–	1600	mVppd
Input voltage, common mode	V_{CM-RX}	400	750	1100	mV
Input voltage, peak	V_{max-RX}	0	–	1500	mV

8.2.12 RGMII Pin Operation at 2.5V VDDO_RGMII

Table 54: RGMII Pin Operation at 2.5V VDDO_RGMII

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage, RGMII pin	V_{IH}	1.70	OVDD_RGMII	V	–
Input low voltage, RGMII pin	V_{IL}	–0.30	+0.70	V	–
Output high voltage, RGMII pin	V_{OH}	2.0	–	V	I_{OH} = –1 mA
Output low voltage, RGMII pin	V_{OL}	–	0.4	V	I_{OL} = 1 mA

8.2.13 RGMII Pin Operation at 1.5V VDDO_RGMII

Table 55: RGMII Pin Operation at 1.5V VDDO_RGMII

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage, RGMII pin	V_{IH}	0.5xOVDD_RGMII+0.1	OVDD_RGMII	V	HSTL

Table 55: RGMII Pin Operation at 1.5V VDDO_RGMII (Continued)

Parameter	Symbol	Min.	Max.	Unit	Condition
Input low voltage, RGMII pin	V_{IL}	–0.30	0.5xOVDD_RGMII-0.1	V	HSTL
Output high voltage, RGMII pin	V_{OH}	OVDD_RGMII-0.4	–	V	HSTL
Output low voltage, RGMII pin	V_{OL}	–	0.4	V	HSTL

8.3 Power Consumption

8.3.1 Power Consumption

Table 56: BCM53158X Estimated Power Consumption

Measured Power Consumption							
Symbol	**Part**	**Power Rail**	**Conditions**	**Min.**	**Typical**	**Max.**	**Unit**
Blocks	BCM53158	Core VDD	Measured	–	–	1.923667	W
		1V Analog	Measured	–	–	0.775333	W
		3.3V	Measured	–	–	1.862	W
		2.5V	Measured	–	–	0.081	W
		1.8V	Measured	–	–	0.100667	W
Total			Measured	–	–	4.742667	W
This maximum power consumption was measured with below worst case conditions: ■ 33G full traffic running with all interfaces ■ Junction Temperature (T_j) at 110°C ■ AVS running for VDDC_1P0							

Table 57: BCM53156 Estimated Power Consumption

Symbol	Part	Power Rail	Conditions	Min.	Typical	Max.	Unit
Current	BCM53156	3.3V	Estimated	–	320.495	343.295	mA
		1.8V	Estimated	–	64.331	78.311	mA
		1.0V digital core	Estimated	–	1961.130	2266.250	mA
		1.0V analog	Estimated	–	657.810	764.726	mA
Power			Estimated	–	3792.370	4304.809	mW
This power consumption was estimated with the following conditions: ■ Full traffic running with all interfaces. ■ Junction Temperature (Tj) at 110°C for Max case and 25°C for typical case. ■ VDDC_1P0 = 1.05V In others power rails: +5% for a max case and normal value for a typical case.							

Table 58: BCM53154 Estimated Power Consumption

Measured Power Consumption							
Symbol	**Part**	**Power Rail**	**Conditions**	**Min.**	**Typical**	**Max.**	**Unit**

Table 58: BCM53154 Estimated Power Consumption (Continued)

Measured Power Consumption							
Blocks	BCM53154	Core VDD	Measured	–	–	1.557	W
		1V Analog	Measured	–	–	0.462	W
		3.3V	Measured	–	–	1.112	W
		2.5V	Measured	–	–	0.082	W
		1.8V	Measured	–	–	0.098	W
Total			Measured	–	–	3.311	W

This maximum power consumption was measured with below worst case conditions:

- 33G full traffic running with all interfaces
- Junction Temperature (T_j) at 110°C
- AVS running for VDDC_1P0

Chapter 9: Timing Characteristics

9.1 Reset and Clock Timing

Figure 34: Reset and Clock Timing

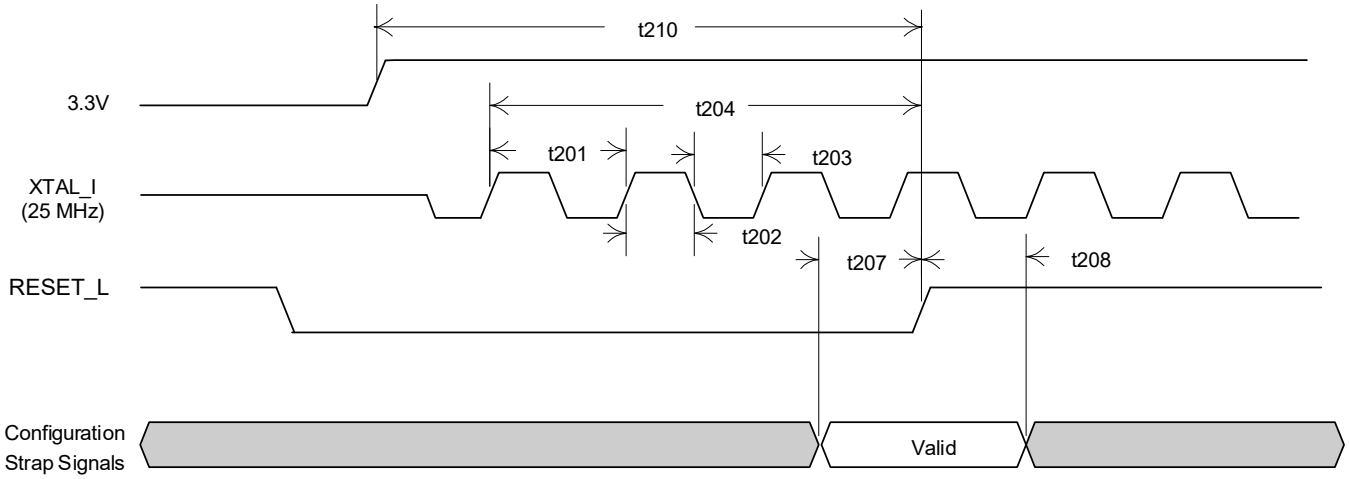


Table 59: Reset and Clock Timing

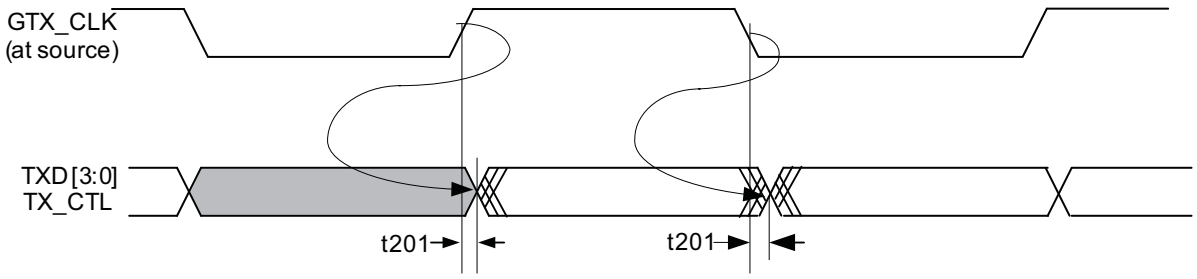
Parameter	Description	Minimum	Typical	Maximum	Unit
t201	XTAL_P frequency	–	25.0000	–	MHz
t202	XTAL_P high time	–	20	–	ns
t203	XTAL_P low time	–	20	–	ns
t204	RESET_L low pulse duration	80	100	–	ms
t207	Configuration valid setup to RESET_L rising	50	–	–	ns
t208	Configuration valid hold from RESET_L rising	120	–	–	ns
t210	Reset low hold time after power supplies stabilize	100	–	–	ms

9.2 RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

9.2.1 RGMII Output Timing (Normal Mode)

Figure 35: RGMII Output Timing (Normal Mode)



NOTE: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

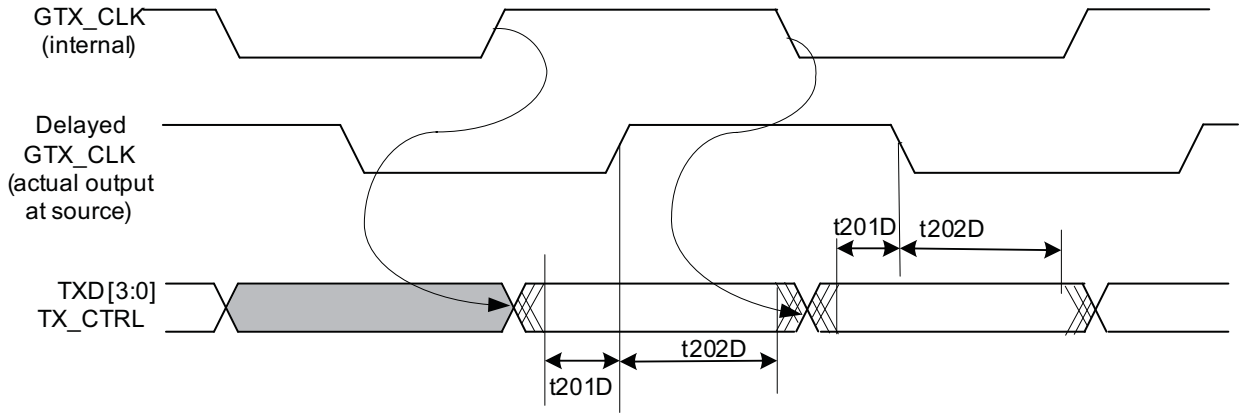
Table 60: RGMII Output Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TskewT: Data to clock output skew	t201	–500 (1000M)	0	+500 (1000M)	ps
TskewT: Data to Clock at 1.5V mode	t201	–750 (1000M)	0	+500 (1000M)	ps
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

NOTE: The output timing in 10/100M operation is always as specified in the delayed mode.

9.2.2 RGMII Output Timing (Delayed Mode)

Figure 36: RGMII Output Timing (Delayed Mode)



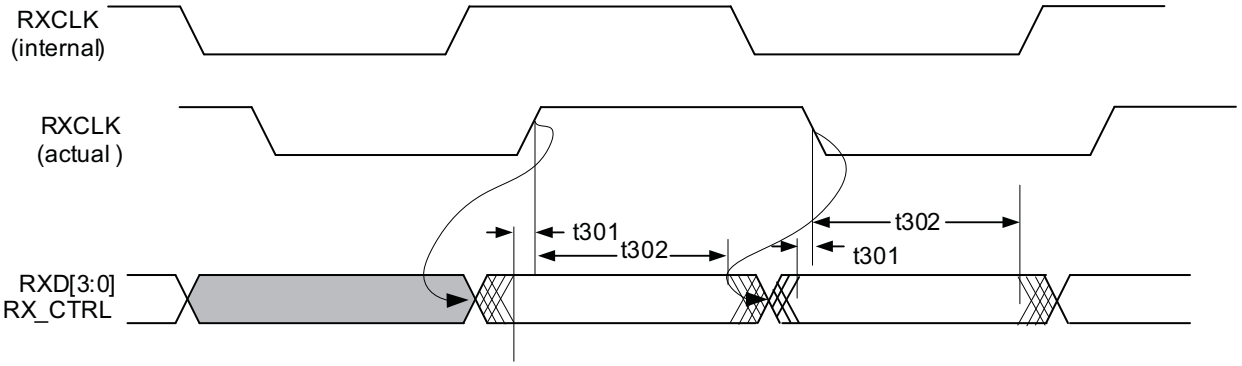
NOTE: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 61: RGMII Output Timing (Delayed Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MII1_TXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_TXC clock period (100M mode)	–	36	40	44	ns
MII1_TXC clock period (10M mode)	–	360	400	440	ns
TsetupT Data valid to clock transition: Available setup time at the output source (delayed mode)	t201D	1.2 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (delayed mode)	t202D	1.2 (all speeds)	2.0	–	ns
TsetupT Data valid to clock transition: Available setup time at the output source (1.5V mode)	t201D	1.0 (all speeds)	2.0	–	ns
TholdT Clock transition to data valid: Available hold time at the output source (1.5V mode)	t202D	1.0 (all speeds)	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

9.2.3 RGMII Input Timing (Normal Mode)

Figure 37: RGMII Input Timing (Normal Mode)



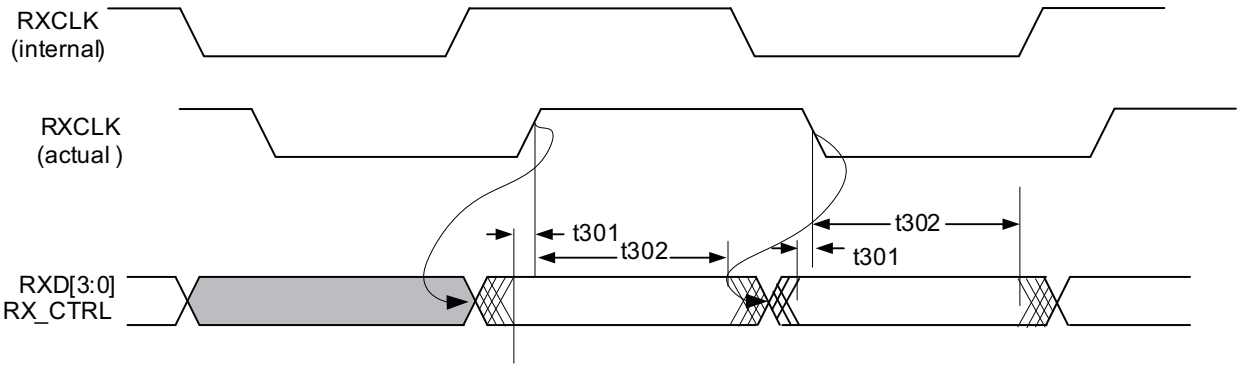
NOTE: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 62: RGMII Input Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MII1_RXC clock period (1000M mode)	–	7.2	8	8.8	ns
MII1_RXC clock period (100M mode)	–	36	40	44	ns
MII1_RXC clock period (10M mode)	–	360	400	440	ns
TsetupR Input setup time: Valid data to clock	t301	1.0	2.0	–	ns
TholdR Input hold time: Clock to valid data	t302	1.0	2.0	–	ns
Duty cycle for 1000M (GE)	–	45	50	55	%
Duty cycle for 10/100M (FE)	–	40	50	60	%

9.2.4 RGMII Input Timing (Delayed Mode)

Figure 38: RGMII Input Timing (Delayed Mode)



NOTE: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

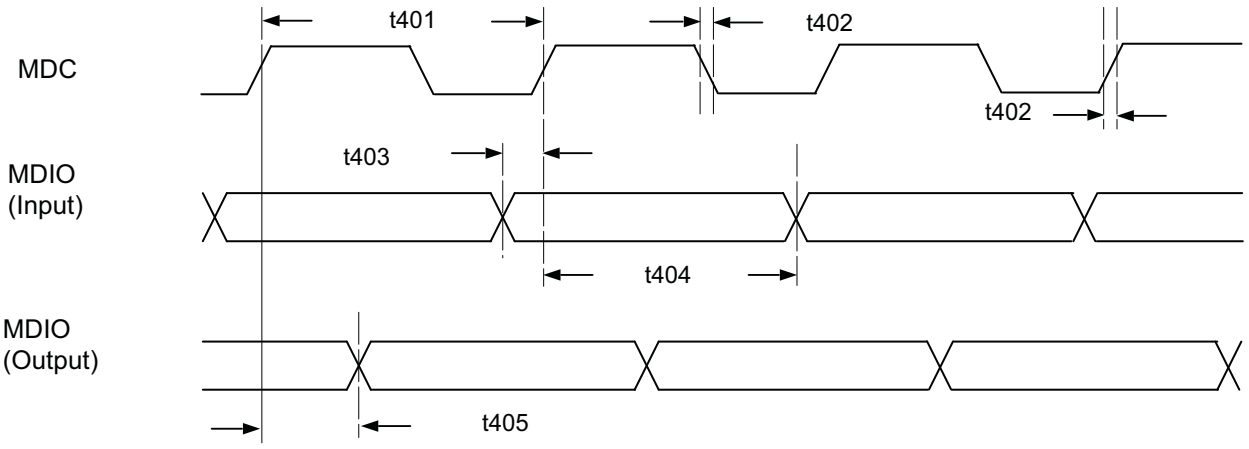
Table 63: RGMII Input Timing (Delayed Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
TsetupR Input setup time (delayed mode)	t301D	–1.0 (1000M)	–	–	ns
		–1.0 (10/100M)	–	–	ns
TholdR Input hold time (delayed mode)	t302D	3.0 (1000M)	–	–	ns
		9.0 (10/100M)	–	–	ns

9.3 MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.

Figure 39: MDC/MDIO Timing (Slave Mode)



NOTE: Advanced timing extracted from statistical data. It may or may not reflect the true timing of the device.

Table 64: MDC/MDIO Timing (Slave Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MDC cycle time	t401	80	–	–	ns
MDC high/low	–	30	–	–	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	7.5	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC rising	t405	0	–	45	ns

NOTE: MDC/MDIO slave mode is for manufacturing testing only.

Figure 40: MDC/MDIO Timing (Master Mode)

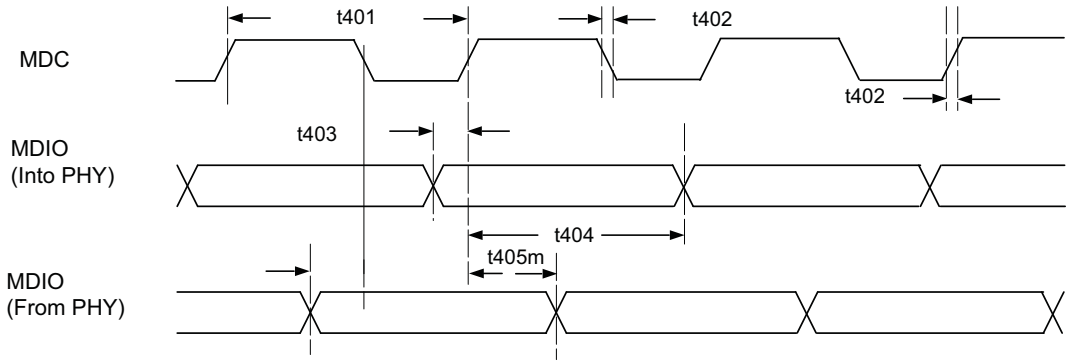


Table 65: MDC/MDIO Timing (Master Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
MDC cycle time	t401	400	–	–	ns
MDC high/low	–	160	–	240	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	20	–	–	ns
MDIO input hold time from MDC rising	t404	7.5	–	–	ns
MDIO output delay from MDC rising	t405	0	–	30	ns

9.4 Serial Flash Timing

Figure 41: Serial Flash Timing Diagram

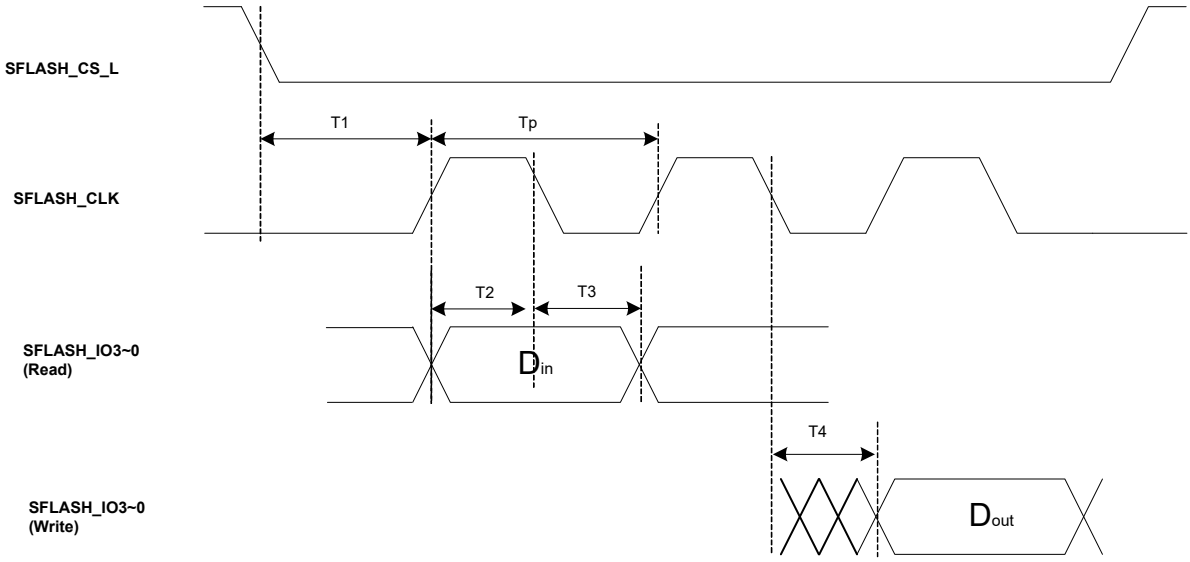


Table 66: Serial Flash Timing

Parameter	Descriptions	Min.	Typ.	Max.	Unit
f_{FREQ}	SFlash_CLK frequency	–	–	62.5	MHz
t_P	Cycle time: SFLASH_CLK period	16	–	–	ns
t_1	Delay time: SFLASH_CS_L low to SFLASH_CLK rising edge	–	1	–	t_P
t_2	Input Setup time: SFLASH_IOx valid to SFLASH_CLK falling edge	10	–	–	ns
t_3	Input Hold time: SFLASH_CLK falling edge to SFLASH_IOx invalid	0	–	–	ns
t_4	Output valid time: SFLASH_IOx valid to SFLASH_CLK rising edge	6	–	–	ns

9.5 SPI Interface Timing

9.5.1 BCM53154/BCM53156/BCM53158 SPI-1 Master Interface Timing (A1)

Figure 42: SPI-1 Timing, SS Asserted During SCK Low

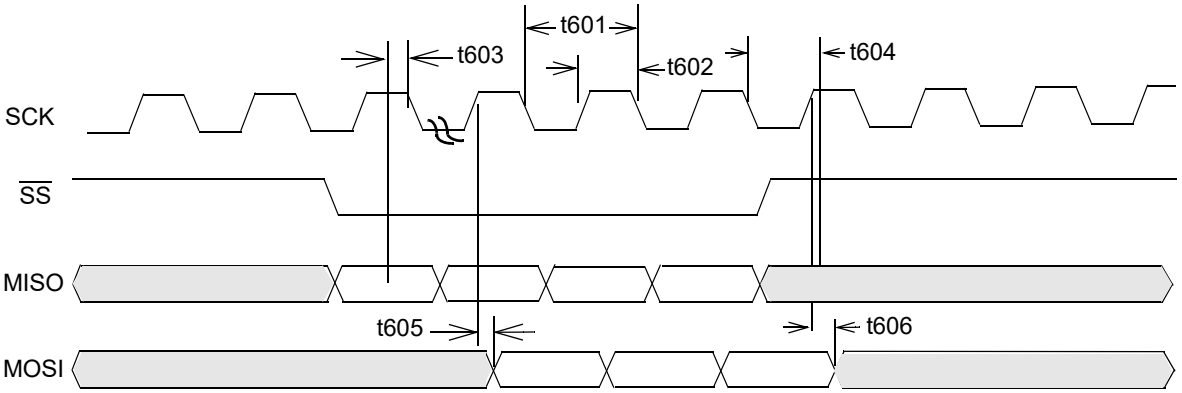


Table 67: SPI-1 Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
t601	SCK Clock Period	40	–	–	ns
t602	SCK High/Low Time	–	–	–	ns
t603	MISO to SCK Setup Time	7	–	–	ns
t604	MISO to SCK Hold Time	0	–	–	ns
t605	SCK to MOSI Valid	–	–	6	ns
t606	SCK to MOSI Invalid	0	–	–	ns

9.5.2 BCM53154/BCM53156/BCM53158 SPI-2 Slave Interface Timing (A1)

Figure 43: SPI-2 Timing, SS Asserted During SCK Low

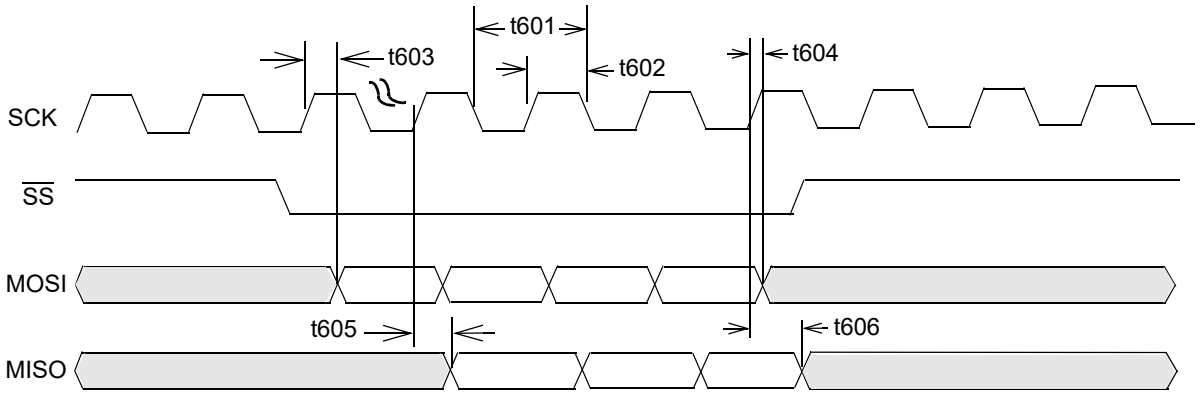


Table 68: SPI-2 Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
t601	SCK Clock Period	40	–	–	ns
t602	SCK High/Low Time	–	–	–	ns
t603	MOSI to SCK Setup Time	5	–	–	ns
t604	MOSI to SCK Hold Time	3	–	–	ns
t605	SCK to MISO Valid	–	–	7	ns
t606	SCK to MISO Invalid	0	–	–	ns

9.5.3 BCM53154/BCM53156/BCM53158 SPI-1 Master Interface Timing (B0)

Figure 44: SPI-1 Timing, $\overline{SS}$ Asserted During SCK High

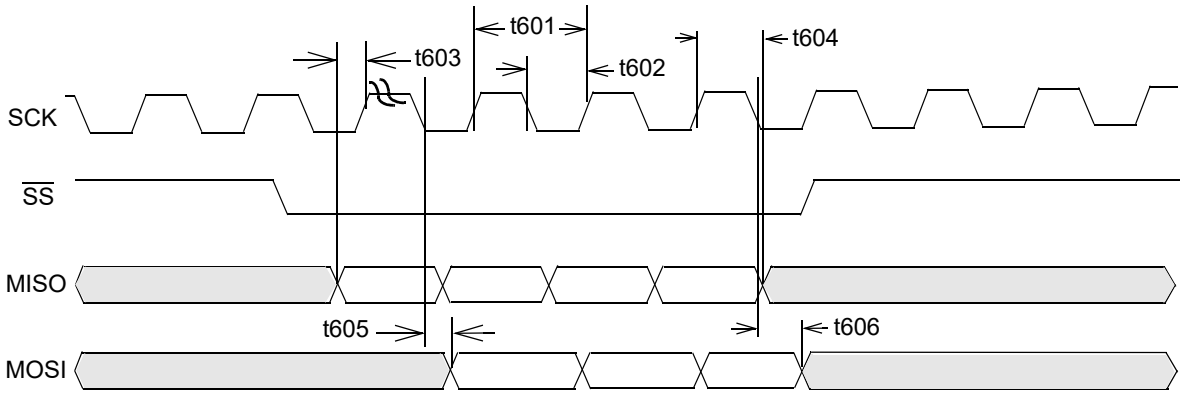


Table 69: SPI-1 Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
t601	SCK Clock Period	40	–	–	ns
t602	SCK High/Low Time	–	–	–	ns
t603	MISO to SCK Setup Time	7	–	–	ns
t604	MISO to SCK Hold Time	0	–	–	ns
t605	SCK to MOSI Valid	–	–	6	ns
t606	SCK to MOSI Invalid	0	–	–	ns

9.5.4 BCM53154/BCM53156/BCM53158 SPI-2 Slave Interface Timing (B0)

Figure 45: SPI-2 Timing, $\overline{SS}$ Asserted During SCK High

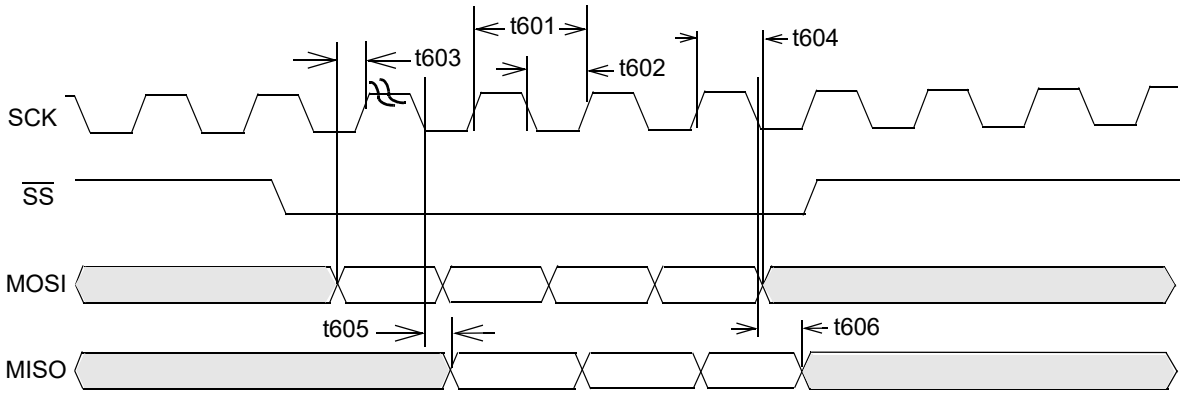


Table 70: SPI-2 Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
t601	SCK Clock Period	40	–	–	ns
t602	SCK High/Low Time	–	–	–	ns
t603	MOSI to SCK Setup Time	5	–	–	ns
t604	MOSI to SCK Hold Time	3	–	–	ns
t605	SCK to MISO Valid	–	–	7	ns
t606	SCK to MISO Invalid	0	–	–	ns

9.6 JTAG Interface

JTAG timing is synchronous to the JTAG_TCK clock.

Figure 46: JTAG Interface

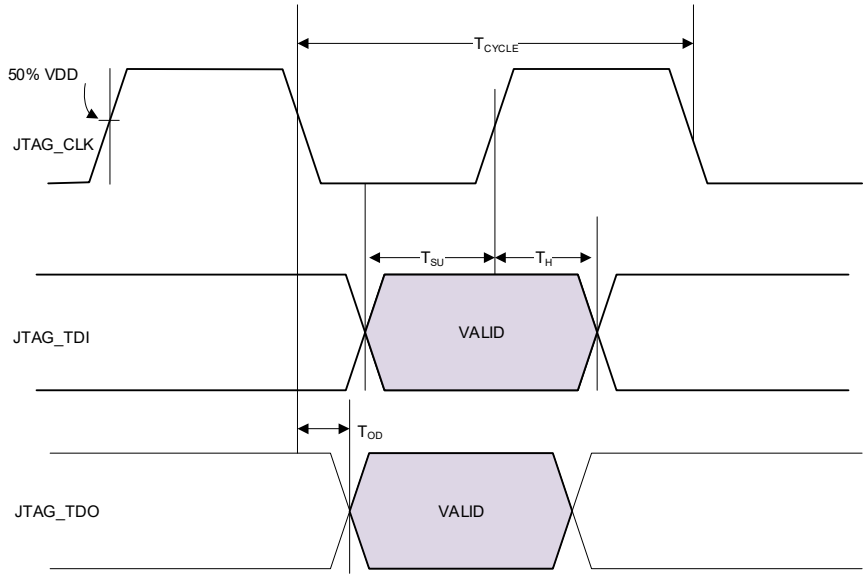


Table 71: JTAG Interface

Parameter	Description	Min.	Typ.	Max.	Unit
TCYCLE	JTAG Cycle Time	50	–	–	ns
TSU	Input Setup Time	12.5	–	–	ns
TH	Input Hold Time	12.5	–	–	ns
TOD	Output Delay Time Measured from Falling Edge of JTAG_TCK	–	–	22	ns

9.7 BSC Timing

Figure 47: BSC Interface

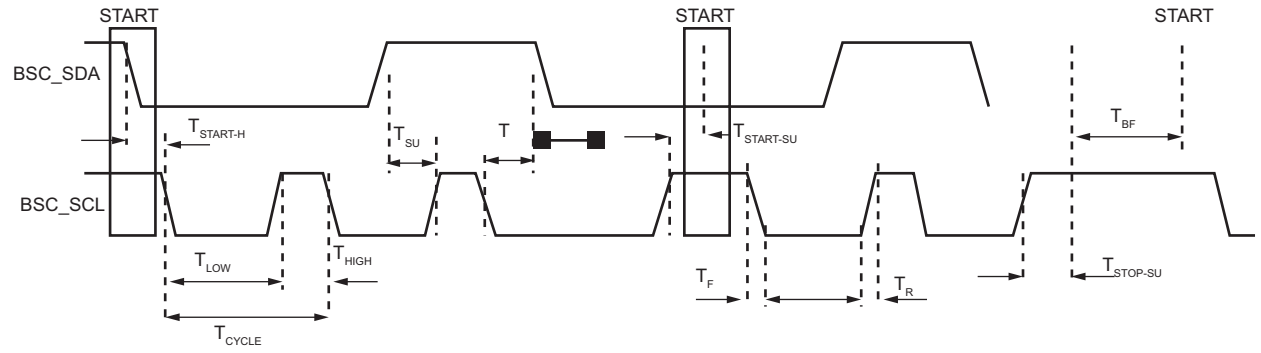


Table 72: BSC Interface

Parameter	Description	Min.	Typ.	Max.	Unit
TCYCLE	BSC_SCL Cycle Time	10	–	100	ns

Table 72: BSC Interface (Continued)

Parameter	Description	Min.	Typ.	Max.	Unit
T_{LOW}	BSC_SCL Low Time	4.7	–	–	ns
T_{HIGH}	BSC_SCL High Time	4.0	–	–	ns
T_H	Data Hold Time	300	–	–	ns
T_{SU}	Data Setup Time	250	–	–	ns
T_R	Rise Time (Clock and Data, see note below)	–	–	1000	ns
T_F	Fall Time (Clock and Data)	–	–	300	ns
$T_{START-H}$	Hold Time, START, or Repeated START	4.0	–	–	ns
$T_{START-SU}$	Setup Time, Repeated START	4.7	–	–	ns
$T_{STOP-SU}$	Setup Time, STOP	4.0	–	–	ns
T_{BF}	Bus Free Time Between STOP and START	4.7	–	–	ns

NOTE:

- BSC_SCL and BSC_SDA are open-collector outputs. The rise time is dependent on the strength of the external pull-up resistor, which is recommended to be chosen to meet the rise time requirement.
- BSC = Broadcom Serial Controller master mode only. It is compatible with I^2C standard. I^2C is copyrighted by Philips/NXP.

9.8 Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

Figure 48: LEDCLK/LEDDATA Timing

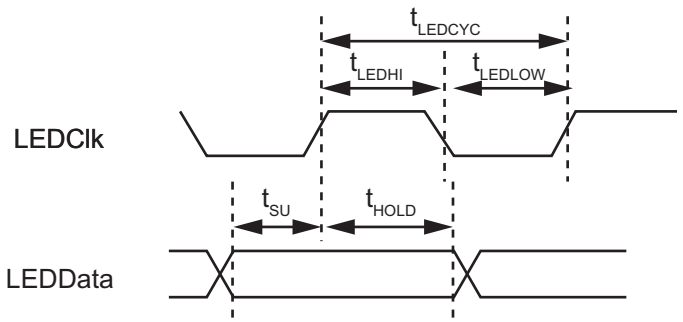


Figure 49: LEDClk/LEDData Refresh Interval

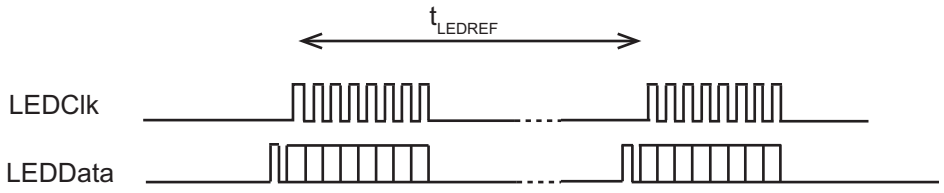


Table 73: Serial LED Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{LEDCYC}	LED clock period	–	200	–	ns
t_{LEDHI}	LED clock high-pulse width	70	100	130	ns
t_{LEDLOW}	LED clock low-pulse width	70	100	130	ns
t_{SU}	LED data setup time	50	90	–	ns
t_{HOLD}	LED data hold time	50	90	–	ns
t_{LEDREF}	LED refresh period	–	30	–	ms

9.9 SGMII/SerDes Timing

Figure 50: SGMII/SerDes Interface Output Timing

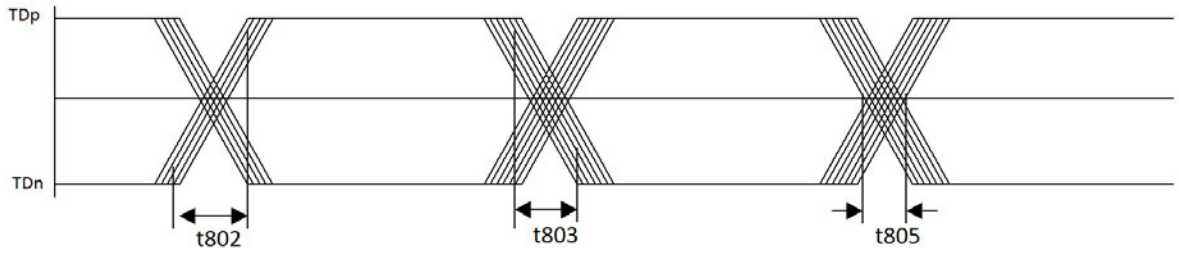


Table 74: SGMII/SerDes Interface Output Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t801	Transmit Data Signaling Speed	–	1.25	–	Gbaud
t802	Transmit Data Rise Time (20% to 80%)	100	–	200	ps
t803	Transmit Data Fall Time (20% to 80%)	100	–	200	ps
t805	Transmit Data Total Jitter	–	–	0.25	UI

Figure 51: SGMII/SerDes Interface Input Timing

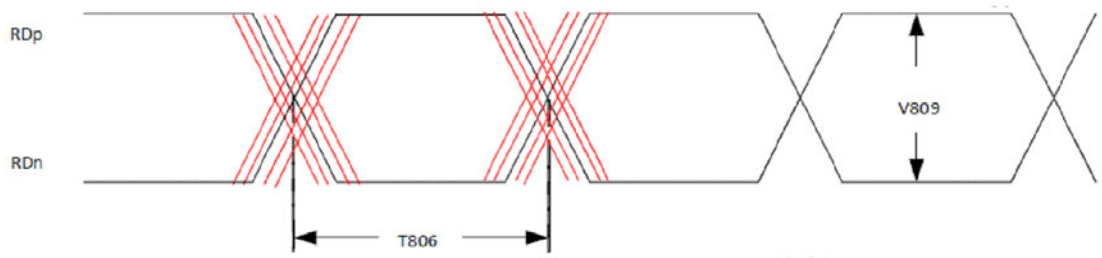


Table 75: SGMII/SerDes Interface Input Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t806	Receive Data Signaling Speed	–	3.125	–	Gbaud
v809	Receive Data Differential Input (pk-pk)	0.1	–	2.0	V

9.10 2.5GE/SerDes Timing

Figure 52: 2.5GE/SerDes Interface Output Timing

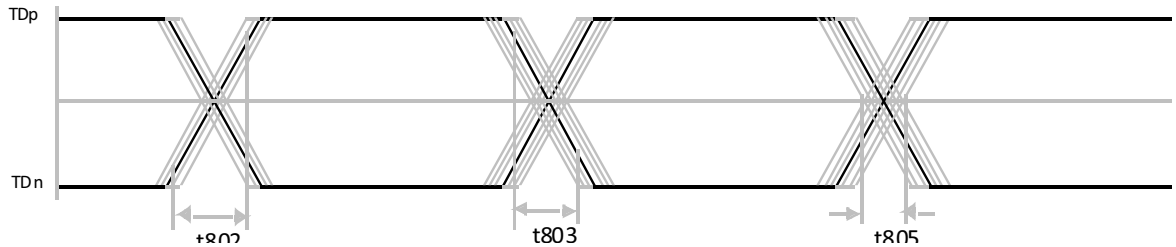


Table 76: 2.5GE/SerDes Interface Output Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t801	Transmit Data Signaling Speed	–	3.125	–	Gbaud
t802	Transmit Data Rise Time (20% to 80%)	30	–	130	ps
t803	Transmit Data Fall Time (20% to 80%)	30	–	130	ps
t805	Transmit Data Total Jitter	–	–	0.35	UI
T_{SKEW}	Transmit Differential Skew	–	–	0.15	ps

Figure 53: 2.5GE/SerDes Interface Input Timing

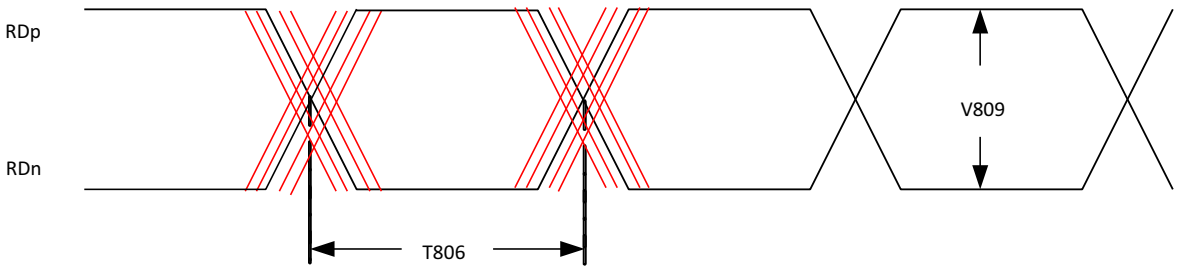


Table 77: 2.5GE/SerDes Interface Input Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t806	Receive Data Signaling Speed	–	3.125	–	Gbaud
v809	Receive Data Differential Input (pk-pk)	–	–	1.6	V

9.11 Synchronous Ethernet Interface

TBD

Chapter 10: Thermal Characteristics

10.1 BCM53156/58 Package with Heat Sink (35×35×15 mm^3)

Table 78: 13x13 mm^2 Package with External Heat Sink 35x35x15 mm^3, 2s2p PCB, T_A = 50°C, P = 4.566W

Device power dissipation, P (W)		4.566				
Ambient air temperature, T_A (°C)		50.0				
θ_{JA} in still air (°C/W)		13.74				
θ_{JB} (°C/W)		10.68				
θ_{JC} (°C/W)		4.25				
2s2p board, 35x5x15 mm^3 estHS						
Package Thermal Performance Curve						
Air Velocity		**$T_{J, MAX}$**	**T_T**	**$\theta_{JA/JMA}$**	**Ψ_{JT}**	**$\Psi_{JB, AVG}$**
m/s	**ft/min**	**(°C)**	**(°C)**	**(°C/W)**	**(°C/W)**	**(°C/W)**
0	0	112.7	99.6	13.74	2.88	6.80
0.5	98.4	100.7	87.1	11.11	2.99	6.22
1	196.9	95.1	81.2	9.87	3.04	5.97
2	393.7	90.8	76.8	8.94	3.08	5.78
3	590.6	88.7	74.5	8.47	3.10	5.68

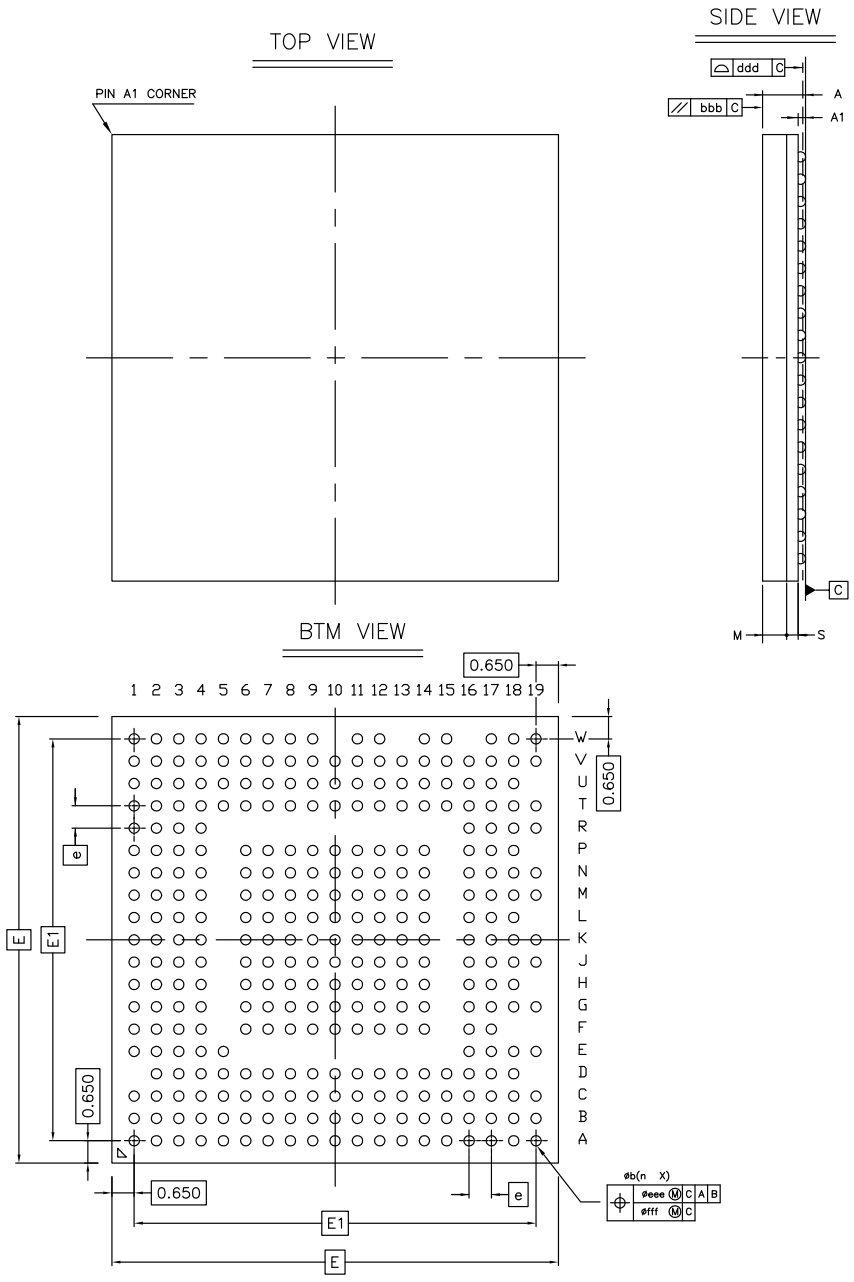
10.2 BCM53154 Package with Heat Sink Package with Heat Sink (45×45×15 mm^3)

Table 79: 19x19 mm^2 Package with External Heat Sink 45x45x15 mm^3, 2s2p PCB, T_A = 50°C, P = 4.651W

Device power dissipation, P (W)		TBD				
Ambient air temperature, T_A (°C)		TBD				
θ_{JA} in still air (°C/W) with external heat sink		TBD				
$\theta_{JB/AVG}$ (°C/W)		TBD				
θ_{JC} (°C/W)		TBD				
2s2p board, 45x45x15 mm^3 estHS						
Package Thermal Performance Curve						
Air Velocity		**$T_{J, MAX}$**	**T_T**	**$\theta_{JA, JMA}$**	**Ψ_{JT}**	**$\Psi_{JB, AVG}$**
m/s	**ft/min**	**(°C)**	**(°C)**	**(°C/W)**	**(°C/W)**	**(°C/W)**
0	TBD	TBD	TBD	TBD	TBD	TBD
0.5	TBD	TBD	TBD	TBD	TBD	TBD
1	TBD	TBD	TBD	TBD	TBD	TBD
2	TBD	TBD	TBD	TBD	TBD	TBD
3	TBD	TBD	TBD	TBD	TBD	TBD

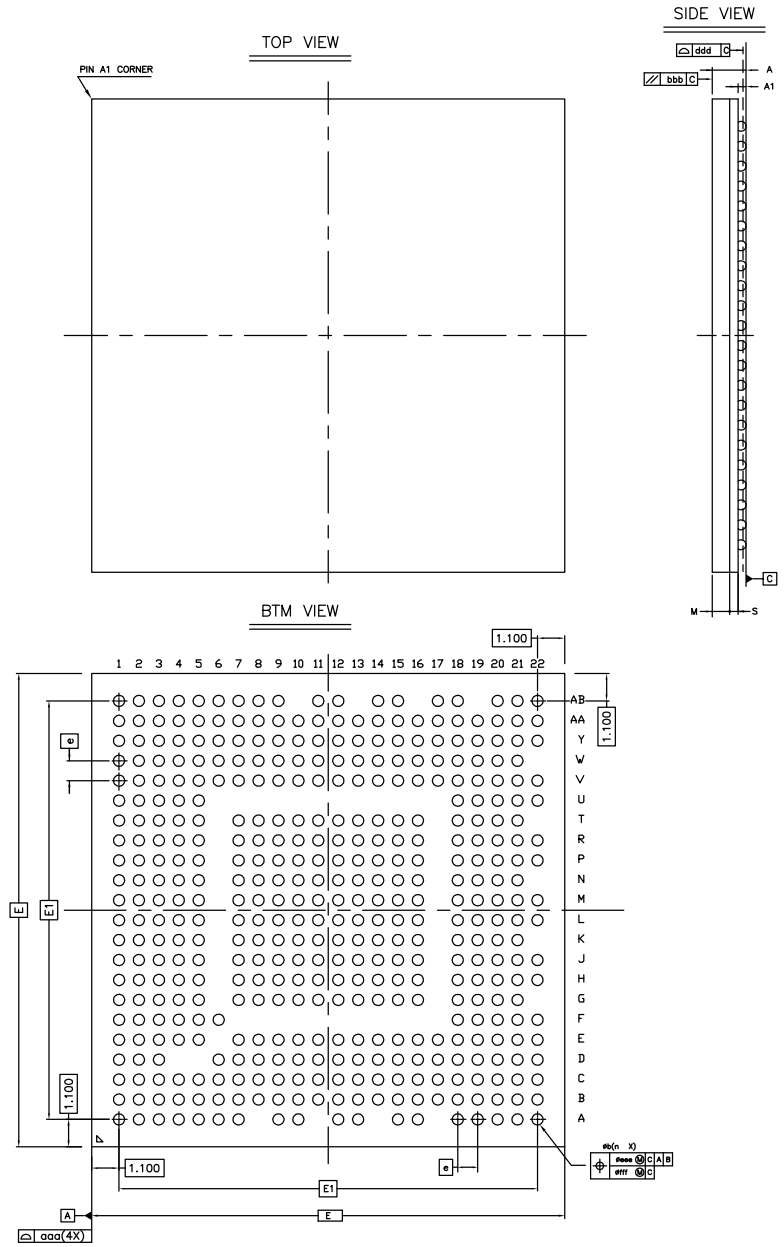
Chapter 11: Mechanical Information

Figure 54: BCM53156/BCM53158 13×13 mm^2 Mechanical Information



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			LFBGA		
Body Size:	X	E	13.000		
	Y	D	13.000		
Ball Pitch :		e	0.650		
Total Thickness :		A	1.167	1.252	1.337
Mold Thickness :		M	0.700 Ref.		
Substrate Thickness :		S	0.332 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.170		0.270
Ball Width :		b	0.260	–	0.360
Package Edge Tolerance :		aaa	0.050		
Mold Parallelism :		bbb	0.200		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	311		
Edge Ball Center to Center :	X	E1	11.700		
	Y	D1	11.700		

Figure 55: BCM53154 19×19 mm^2 Mechanical Information



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			LFBGA		
Body Size:	X	E	19.000		
	Y	D	19.000		
Ball Pitch :		e	0.800		
Total Thickness :		A	1.267	1.352	1.437
Mold Thickness :		M	0.700 Ref.		
Substrate Thickness :		S	0.332 Ref.		
Ball Diameter :			0.400		
Stand Off :		A1	0.270		0.370
Ball Width :		b	0.380	–	0.480
Package Edge Tolerance :		aaa	0.075		
Mold Parallelism :		bbb	0.200		
Coplanarity:		ddd	0.120		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	425		
Edge Ball Center to Center :	X	E1	16.800		
	Y	D1	16.800		

Chapter 12: Ordering Information

Table 80: Ordering Information

Part Number	Operational Mode	Package	Ambient
BCM53154MB1ILFBG	Managed	19×19 mm^2, 425-pin FBGA	–40°C to +85°C
BCM53156XUB1KFBG	Unmanaged	13x13 mm^2, 311-pin FBGA	0°C to 70°C
BCM53156XMB1KFBG	Managed	13x13 mm^2, 311-pin FBGA	0°C to 70°C
BCM53158XUB1KFBG	Unmanaged	13x13 mm^2, 311-pin FBGA	0°C to 70°C
BCM53158XPB1KFBG	Port Extender	13x13 mm^2, 311-pin FBGA	0°C to 70°C
BCM53158XMB1KFBG	Managed	13x13 mm^2, 311-pin FBGA	0°C to 70°C

Revision History

53154-53156-53158-DS114; March 20, 2020

Updated:

- Figure 6, Unmanaged Applications – Updated figure
- Figure 8, High-Speed Unmanaged – Updated figure
- Figure 9, Unmanaged Cascade 24+2 Blocking – Updated figure
- Figure 11, Web-Managed Stand-Alone Configuration – Updated figure
- Figure 12, Web-Managed with External Optics – Updated figure
- Figure 13, Web-Managed Configuration with Cascading – Updated figure
- Figure 15, Managed Stand-Alone Configuration – Updated figure
- Figure 16, Managed-Cascaded Configuration – Updated figure

53154-53156-53158-DS113; February 4, 2020

Updated:

- Table 1, BCM53112/BCM5315X/BCM5316X Operational Modes – Updated footnote C.

53154-53156-53158-DS112; December 6, 2019

Updated:

- Table 42, REFCLK Input Timing

53154-53156-53158-DS111; December 3, 2019

Updated:

- Signal Descriptions (13×13 mm2 Package) – Update XTALP definition
- Signal Descriptions (19×19 mm2 Package) – Update XTALP definition
- Reset and Clock Timing – Updated t204 values

53154-53156-53158-DS110; May 29, 2019

Updated:

- Figure 14, Managed Configurations
- MFIO Interface

53154-53156-53158-DS109; January 18, 2019

Updated:

- Table 1, BCM53112/BCM5315X/BCM5316X Operational Modes

53154-53156-53158-DS108; January 2, 2019

Updated:

- Table 3, BCM5315X Family Features
- Table 43, Signal Descriptions (13×13 mm2 Package)

53154-53156-53158-DS107; August 20, 2018

Updated:

- Table 1, BCM53112/BCM5315X/BCM5316X Operational Modes
- Table 43, Signal Descriptions (13×13 mm2 Package)

53154-53156-53158-DS106; August 2, 2018

Updated:

- Signal Descriptions
- Pin Assignment

53154-53156-53158-DS105; May 17, 2018

Updated:

- Table 3, BCM5315X Family Features
- Ordering Information
- MDC/MDIO Timing

Added:

- BCM53154 Package with Heat Sink Package with Heat Sink (45×45×15 mm3)

53156-53158-DS104; April 4, 2018

Updated:

- Table 1, BCM53156/BCM53158 Operational Modes
- Table 2, BCM53156/BCM53158 Family Features
- Table 13, Receive MIB Counters (per port)
- Table 14, Transmit MIB Counters
- Table 39, Signal Descriptions (13×13 mm2 Package)
- Table 52, RGMII Pin Operation at 1.5V VDDO_RGMII
- SPI Interface Timing
- Figure 53, BCM53156/BCM53158 13×13 mm2 Mechanical Information
- Table 75, Ordering Information

Added:

- Electrical Characteristics

53156_53158-DS103; September 29, 2017

Updated:

- Table 1, BCM53112/BCM5315X/BCM5316X Operational Modes
- Table 3, BCM5315X Family Features
- Table 42, Signal Descriptions (13×13 mm Package)
- Table 44, Absolute Maximum Ratings
- “Recommended Operating Conditions and DC Characteristics” on page 146
- “SPI Interface Timing” on page 157
- Table 79, 13x13 mm Package with External Heat Sink 35x35x15 mm, 2s2p PCB, TA = 50°C, P = 4.566W

53156_53157_53158-DS102-R; April 17, 2017

Updated:

- Section 12: “Ordering Information,” on page 142

53156_53157_53158-DS101-R; March 31, 2017

Updated:

- Table 1: “BCM53161/2 Operational Modes,” on page 12
- Table 2: “BCM53156/7/8 Family Features,” on page 16
- “Robo 2 Switch Core Abstraction Libraries” on page 77
- “SPI Slave” on page 84
- “Recommended Operating Conditions and DC Characteristics” on page 120
- Table 66: “SGMII/SerDes Interface Output Timing,” on page 138
- Table 72: “13 x 13 mm Package with External Heat Sink 35 x 35 x 15 mm, 2s2p PCB, TA = 50° C, P = 4.566W,” on page 148

53156_53157_53158-DS100-R; December 1, 2016

Initial release.

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