- **Supports PCI Local Bus Specification 2.1 and PCI-to-PCI Bridge Specification 1.0**
- **3.3-V Core Logic With Universal PCI Interfaces Compatible With 3.3-V and 5-V PCI Signaling Environments**
- **Supports Two 32-Bit, 33-MHz PCI Buses**
- **Provides Internal Arbitration for Up to Six Secondary Bus Masters With Programmable Control**
- **Provides Six Secondary PCI Bus Clock Outputs**
- **Supports Burst Transfers to Maximize Data Throughput on Both PCI Buses**
- **Provides Two Extension Windows**
- **EEPROM Interface for Loading Texas Instruments (TI™) Subsystem ID and Subsystem Vendor ID**
- **Four Primary and Four Secondary General-Purpose I/Os**
- **Independent Read and Write Buffers for Each Direction**
- **Secondary Positive Decode**
- **Predictable Latency: Compliant With PCI Local Bus Specification 2.1**
- **External Arbiter Option**
- **Provides Concurrent Operation**
- **Serial IRQ Bridging**
- **Propagates Bus Locking**
- **Supports PCI Clock Run**
- **Secondary Bus Driven Low During Reset**
- **Docking Connect Detects**
- **PCI Local Bus Specification 2.0-Compliant Device Optimization**
- **Advanced Submicron, Low-Power CMOS Technology**
- **Provides VGA/Palette Memory and I/O, and Subtractive Decoding Options**
- **Packaged in 176-Pin Plastic Quad Flatpack**

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## description

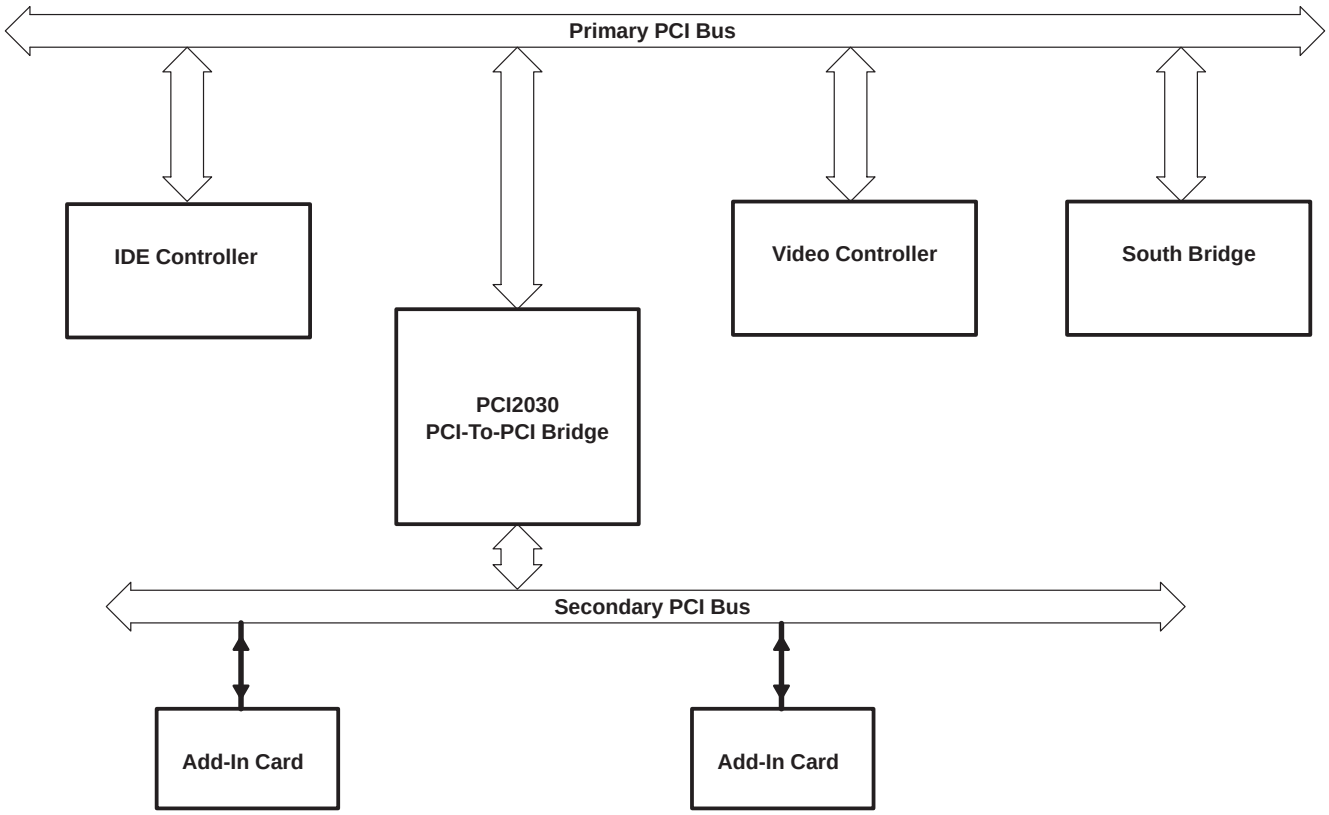
The TI PCI2030 PCI-to-PCI bridge provides a high-performance connection path between two peripheral component interconnect (PCI) buses. Transactions can occur between a master on one PCI bus and a target on another PCI bus. The bridge supports burst-mode transfers to maximize data throughput, and the two bus traffic paths through the bridge act independently.

The PCI2030 bridge is compliant with the PCI Local Bus Specification 2.1, and can be used to overcome the electrical loading limit of ten devices per PCI bus by creating hierarchical buses. Furthermore, add-in cards requiring multiple PCI devices can use the bridge to overcome the electrical loading limit of one PCI device per slot.

The PCI2030 bridge is also compliant with the PCI-to-PCI Bridge Specification 1.0, and implements many additional features that make it an ideal solution for bridging two PCI buses. It can be configured for subtractive decoding, and negative decoding can be disabled on the secondary interface. Two extension windows are also included for special decoding purposes. The serial- and parallel-port addresses can also be programmed for positive decoding on the primary interface. The bridge implements many other features, listed above, that add performance and flexibility.

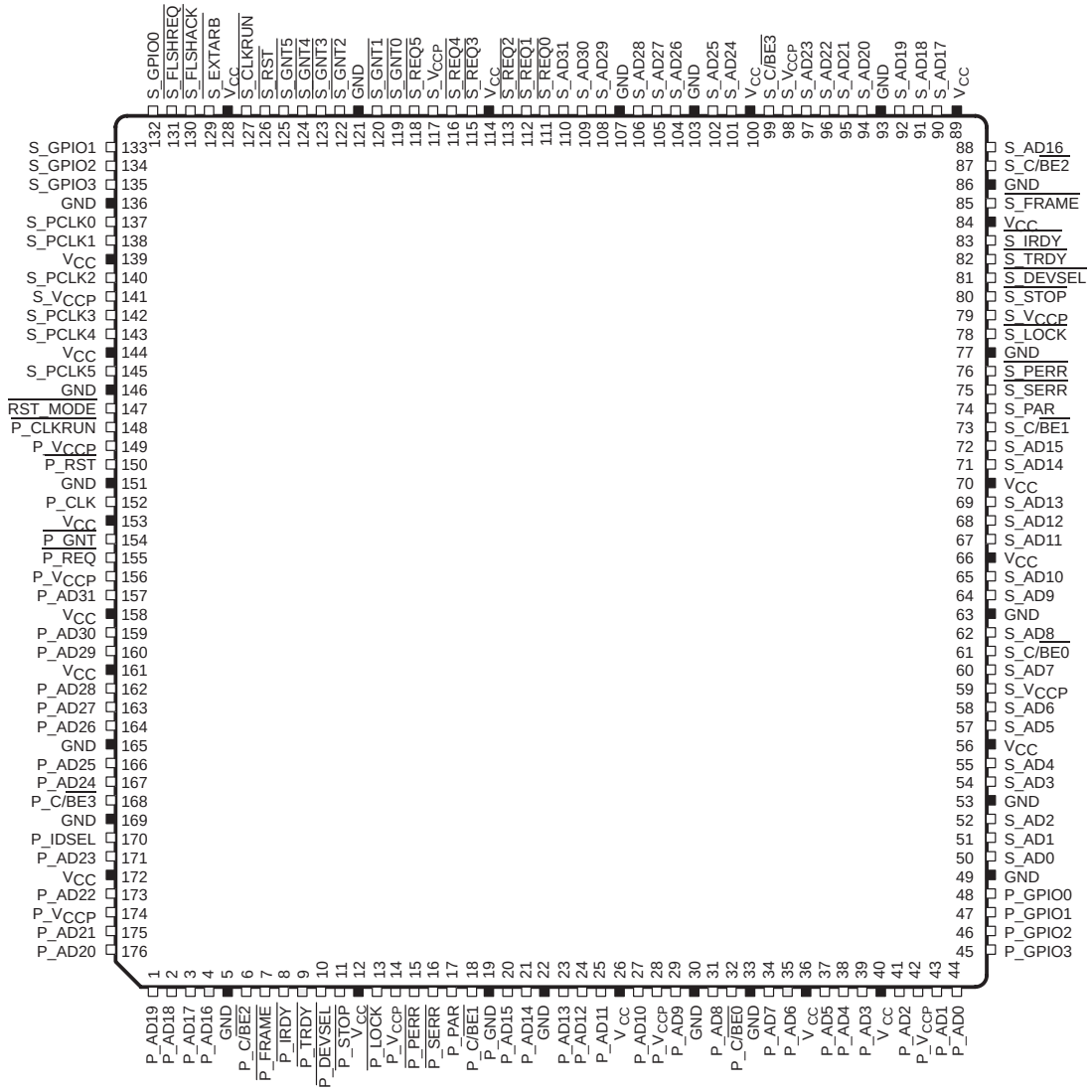
An advanced CMOS process is utilized to achieve low system-power consumption while operating at PCI clock rates up to 33 MHz.

## system block diagram



## terminal assignments

**PGF PACKAGE**
**(TOP VIEW)**



## Terminal Functions

### primary PCI system

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| P_CLK | 152 | I | Primary PCI bus clock. P_CLK provides timing for all transactions on the primary PCI bus. All primary PCI signals are sampled at rising edge of P_CLK. |
| $\overline{\text{R\_RST}}$ | 150 | I | PCI reset. When the primary PCI bus reset is asserted, $\overline{\text{P\_RST}}$ causes the bridge to 3-state all output buffers and reset all internal registers. When asserted, the device is completely nonfunctional. During $\overline{\text{P\_RST}}$, the secondary interface is driven low. After $\overline{\text{P\_RST}}$ is deasserted, the bridge is in its default state. |

### primary PCI address and data

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| P_AD31 | 157 | I/O | Primary address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, P_AD31–P_AD0 contain a 32-bit address or other destination information. During the data phase, P_AD31–P_AD0 contain data. |
| P_AD30 | 159 | | |
| P_AD29 | 160 | | |
| P_AD28 | 162 | | |
| P_AD27 | 163 | | |
| P_AD26 | 164 | | |
| P_AD25 | 166 | | |
| P_AD24 | 167 | | |
| P_AD23 | 171 | | |
| P_AD22 | 173 | | |
| P_AD21 | 175 | | |
| P_AD20 | 176 | | |
| P_AD19 | 1 | | |
| P_AD18 | 2 | | |
| P_AD17 | 3 | | |
| P_AD16 | 4 | | |
| P_AD15 | 20 | | |
| P_AD14 | 21 | | |
| P_AD13 | 23 | | |
| P_AD12 | 24 | | |
| P_AD11 | 25 | | |
| P_AD10 | 27 | | |
| P_AD9 | 29 | | |
| P_AD8 | 31 | | |
| P_AD7 | 34 | | |
| P_AD6 | 35 | | |
| P_AD5 | 37 | | |
| P_AD4 | 38 | | |
| P_AD3 | 39 | | |
| P_AD2 | 41 | | |
| P_AD1 | 43 | | |
| P_AD0 | 44 | | |
| P_C/$\overline{\text{BE3}}$ | 168 | I/O | Primary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, P_C/$\overline{\text{BE3}}$–P_C/$\overline{\text{BE0}}$ define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. P_C/$\overline{\text{BE0}}$ applies to byte 0 (P_AD7–P_AD0), P_C/$\overline{\text{BE1}}$ applies to byte 1 (P_AD15–P_AD8), P_C/$\overline{\text{BE2}}$ applies to byte 2 (P_AD23–P_AD16), and P_C/$\overline{\text{BE3}}$ applies to byte 3 (P_AD31–P_AD24). |
| P_C/$\overline{\text{BE2}}$ | 6 | | |
| P_C/$\overline{\text{BE1}}$ | 18 | | |
| P_C/$\overline{\text{BE0}}$ | 32 | | |
| $\overline{\text{P\_CLKRUN}}$ | 148 | I/O | Primary PCI bus clock run. $\overline{\text{P\_CLKRUN}}$ is used by the central resource to request permission to stop the PCI clock or to slow it down. |

## Terminal Functions (Continued)

### primary PCI interface control

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| P_DEVSEL | 10 | I/O | Primary device select. The bridge asserts P_DEVSEL to claim a PCI cycle as the target device. As a PCI initiator on the primary bus, the bridge monitors P_DEVSEL until a target responds. If no target responds before time-out occurs, then the bridge terminates the cycle with an initiator abort. |
| P_FRAME | 7 | I/O | Primary cycle frame. P_FRAME is driven by the initiator of a primary bus cycle. P_FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When P_FRAME is deasserted, the primary bus transaction is in the final data phase. |
| P_GNT | 154 | I | Primary bus grant to bridge. P_GNT is driven by the primary PCI bus arbiter to grant the bridge access to the primary PCI bus after the current data transaction has completed. P_GNT may or may not follow a primary bus request, depending on the primary bus parking algorithm. |
| P_GPIO3<br>P_GPIO2<br>P_GPIO1<br>P_GPIO0 | 45<br>46<br>47<br>48 | I/O | Primary bus general-purpose I/O terminals. These terminals are provided for general input/output use in system design. |
| P_IDSEL | 170 | I | Initialization device select. P_IDSEL selects the bridge during configuration space accesses. P_IDSEL can be connected to one of the upper 24 PCI address lines on the primary PCI bus.<br>Note: There is no IDSEL signal interfacing the secondary PCI bus; thus, the entire configuration space of the bridge can only be accessed from the primary bus. |
| P_IRDY | 8 | I/O | Primary initiator ready. P_IRDY indicates the primary bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until P_IRDY and P_TRDY are both sampled asserted, wait states are inserted. |
| P_LOCK | 13 | I/O | Primary PCI bus lock. P_LOCK is used to lock the primary bus and gain exclusive access as an initiator. |
| P_PAR | 17 | I/O | Primary parity. In all primary bus read and write cycles, the bridge calculates even parity across the P_AD and P_C/BE buses. As an initiator during PCI write cycles, the bridge outputs this parity indicator with a one-P_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the initiator's parity indicator; a misdemeanor can result in a parity error assertion (P_PERR). |
| P_PERR | 15 | I/O | Primary parity error indicator. P_PERR is driven by a primary bus PCI device to indicate that calculated parity does not match P_PAR when P_PERR is enabled through bit 6 of the command register. |
| P_REQ | 155 | O | Primary PCI bus request. P_REQ is asserted by the bridge to request access to the primary PCI bus as an initiator. |
| P_SERR | 16 | O | Primary system error. Output pulsed from the bridge when enabled through the command register indicating a system error has occurred. The bridge need not be the target of the primary PCI cycle to assert P_SERR. When bit 6 is enabled in the bridge control register, P_SERR will also pulse, indicating that a system error has occurred on one of the subordinate buses downstream from the bridge. |
| P_STOP | 11 | I/O | Primary cycle stop signal. P_STOP is driven by a PCI target to request the initiator to stop the current primary bus transaction. P_STOP is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers. |
| RST_MODE | 147 | I | If RST_MODE is asserted during P_RST, it causes S_RST to be asserted and the secondary clocks to be turned off. |
| P_TRDY | 9 | I/O | Primary target ready. P_TRDY indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of P_CLK where both P_IRDY and P_TRDY are asserted. Until both P_IRDY and P_TRDY are asserted, wait states are inserted. |

## Terminal Functions (Continued)

### secondary PCI system

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| S_PCLK5<br>S_PCLK4<br>S_PCLK3<br>S_PCLK2<br>S_PCLK1<br>S_PCLK0 | 145<br>143<br>142<br>140<br>138<br>137 | O | Secondary PCI bus clock. Provides timing for all transactions on the secondary PCI bus. All secondary PCI signals are sampled at the rising edge of S_CLK5–S_CLK0. |
| $\overline{\text{S\_CLKRUN}}$ | 127 | I/O | Secondary PCI bus clock run. $\overline{\text{S\_CLKRUN}}$ is output by the bridge to indicate that S_CLK will be stopped. $\overline{\text{S\_CLKRUN}}$ is driven by secondary bus PCI devices to request that S_CLK be stopped. |
| $\overline{\text{S\_EXTARB}}$ | 129 | I | Secondary external arbiter enable. When $\overline{\text{S\_EXTARB}}$ is asserted, the secondary external arbiter is enabled. When the external arbiter is enabled, $\overline{\text{S\_REQ0}}$ is reconfigured as a secondary bus grant input to the bridge and $\overline{\text{S\_GNT0}}$ is reconfigured as a secondary bus master request to the external arbiter on the secondary bus. |
| $\overline{\text{S\_RST}}$ | 126 | O | Secondary PCI reset. $\overline{\text{S\_RST}}$ is a logical OR of $\overline{\text{P\_RST}}$ and the state of the secondary bus reset bit of the bridge control register. $\overline{\text{S\_RST}}$ is asynchronous with respect to the state of the secondary interface CLK signal. |

## Terminal Functions (Continued)

### secondary PCI address and data

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| S_AD31 | 110 | I/O | Secondary address/data bus. These signals make up the multiplexed PCI address and data bus on the secondary interface. During the address phase of a secondary bus PCI cycle, S_AD31–S_AD0 contain a 32-bit address or other destination information. During the data phase, S_AD31–S_AD0 contain data. |
| S_AD30 | 109 | | |
| S_AD29 | 108 | | |
| S_AD28 | 106 | | |
| S_AD27 | 105 | | |
| S_AD26 | 104 | | |
| S_AD25 | 102 | | |
| S_AD24 | 101 | | |
| S_AD23 | 97 | | |
| S_AD22 | 96 | | |
| S_AD21 | 95 | | |
| S_AD20 | 94 | | |
| S_AD19 | 92 | | |
| S_AD18 | 91 | | |
| S_AD17 | 90 | | |
| S_AD16 | 88 | | |
| S_AD15 | 72 | | |
| S_AD14 | 71 | | |
| S_AD13 | 69 | | |
| S_AD12 | 68 | | |
| S_AD11 | 67 | | |
| S_AD10 | 65 | | |
| S_AD9 | 64 | | |
| S_AD8 | 62 | | |
| S_AD7 | 60 | | |
| S_AD6 | 58 | | |
| S_AD5 | 57 | | |
| S_AD4 | 55 | | |
| S_AD3 | 54 | | |
| S_AD2 | 52 | | |
| S_AD1 | 51 | | |
| S_AD0 | 50 | | |
| S_C/$\overline{BE3}$ | 99 | I/O | Secondary bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a secondary bus PCI cycle, S_C/$\overline{BE3}$–S_C/$\overline{BE0}$ define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. S_C/$\overline{BE0}$ applies to byte 0 (S_AD7–S_AD0), S_C/$\overline{BE1}$ applies to byte 1 (S_AD15–S_AD8), S_C/$\overline{BE2}$ applies to byte 2 (S_AD23–S_AD16), and S_C/$\overline{BE3}$ applies to byte 3 (S_AD31–S_AD24). |
| S_C/$\overline{BE2}$ | 87 | | |
| S_C/$\overline{BE1}$ | 73 | | |
| S_C/$\overline{BE0}$ | 61 | | |
| $\overline{S\_DEVSEL}$ | 81 | I/O | Secondary device select. The bridge asserts $\overline{S\_DEVSEL}$ to claim a PCI cycle as the target device. As a PCI initiator on the secondary bus, the bridge monitors $\overline{S\_DEVSEL}$ until a target responds. If no target responds before timeout occurs, then the bridge terminates the cycle with an initiator abort. |
| $\overline{S\_FRAME}$ | 85 | I/O | Secondary cycle frame. $\overline{S\_FRAME}$ is driven by the initiator of a secondary bus cycle. $\overline{S\_FRAME}$ is asserted to indicate that a bus transaction is beginning and data transfers continue while $\overline{S\_FRAME}$ is asserted. When $\overline{S\_FRAME}$ is deasserted, the secondary bus transaction is in the final data phase. |
| $\overline{S\_GNT5}$ | 125 | O | Secondary bus grant to the bridge. The bridge provides internal arbitration and these signals are used to grant potential secondary PCI bus masters access to the bus. Seven potential initiators (including the bridge) can be located on the secondary PCI bus.<br>When the internal arbiter is disabled, $\overline{S\_GNT0}$ is reconfigured as an external secondary bus request signal for the bridge. |
| $\overline{S\_GNT4}$ | 124 | | |
| $\overline{S\_GNT3}$ | 123 | | |
| $\overline{S\_GNT2}$ | 122 | | |
| $\overline{S\_GNT1}$ | 120 | | |
| $\overline{S\_GNT0}$ | 119 | | |

## Terminal Functions (Continued)

### secondary PCI interface control

| TERMINAL NAME | TERMINAL NO. | I/O TYPE | FUNCTION |
|---|---|---|---|
| S_GPIO3<br>S_GPIO2<br>S_GPIO1<br>S_GPIO0 | 135<br>134<br>133<br>132 | I/O | Secondary general-purpose I/O terminals. These terminals are provided for general-purpose input/output use in system design. |
| $\overline{\text{S\_IRDY}}$ | 83 | I/O | Secondary initiator ready. $\overline{\text{S\_IRDY}}$ indicates the secondary bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both $\overline{\text{S\_IRDY}}$ and $\overline{\text{S\_TRDY}}$ are asserted; until $\overline{\text{S\_IRDY}}$ and $\overline{\text{S\_TRDY}}$ are asserted, wait states are inserted. |
| $\overline{\text{S\_LOCK}}$ | 78 | I/O | Secondary lock $\overline{\text{S\_LOCK}}$ is used to lock the secondary bus and gain exclusive access as an initiator. |
| S_PAR | 74 | I/O | Secondary parity. In all secondary bus read and write cycles, the bridge calculates even parity across the S_AD and S_C/$\overline{\text{BE}}$ buses. As an initiator during PCI write cycles, the bridge outputs this parity indicator with a one-S_CLK delay. As a target during PCI read cycles, the calculated parity is compared to the initiator's parity indicator. A miscompare can result in a parity error assertion ($\overline{\text{S\_PERR}}$). |
| $\overline{\text{S\_PERR}}$ | 76 | I/O | Secondary parity error indicator. $\overline{\text{S\_PERR}}$ is driven by a secondary bus PCI device to indicate that calculated parity does not match S_PAR when enabled through the command register. |
| $\overline{\text{S\_REQ5}}$<br>$\overline{\text{S\_REQ4}}$<br>$\overline{\text{S\_REQ3}}$<br>$\overline{\text{S\_REQ2}}$<br>$\overline{\text{S\_REQ1}}$<br>$\overline{\text{S\_REQ0}}$ | 118<br>116<br>115<br>113<br>112<br>111 | I | Secondary PCI bus request signals. The bridge provides internal arbitration, and these signals are used as inputs from secondary PCI bus initiators requesting the bus. Seven potential initiators (including the bridge) can be located on the secondary PCI bus.<br><br>When the internal arbiter is disabled, $\overline{\text{S\_REQ0}}$ is reconfigured as an external secondary bus grant for the bridge. |
| $\overline{\text{S\_SERR}}$ | 75 | I | Secondary system error. $\overline{\text{S\_SERR}}$ is passed through the primary interface by the bridge if enabled through the bridge control register. $\overline{\text{S\_SERR}}$ is never asserted by the bridge. |
| $\overline{\text{S\_STOP}}$ | 80 | I/O | Secondary cycle stop signal. $\overline{\text{S\_STOP}}$ is driven by a PCI target to request the initiator to stop the current secondary bus transaction. $\overline{\text{S\_STOP}}$ is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers. |
| $\overline{\text{S\_TRDY}}$ | 82 | I/O | Secondary target ready. $\overline{\text{S\_TRDY}}$ indicates the secondary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of S_CLK where both $\overline{\text{S\_IRDY}}$ and $\overline{\text{S\_TRDY}}$ are asserted; until $\overline{\text{S\_IRDY}}$ and $\overline{\text{S\_TRDY}}$ are asserted, wait states are inserted. |
| $\overline{\text{S\_FLSHREQ}}$ | 131 | I | Flush request. When $\overline{\text{S\_FLSHREQ}}$ is asserted, it signals a request to the PCI2030 to suspend internal write posting. When the bridge is ready to suspend internal write posting, it responds by asserting $\overline{\text{S\_FLSHACK}}$. $\overline{\text{S\_FLSHACK}}$ remains asserted until the write posting buffers are empty. |
| $\overline{\text{S\_FLSHACK}}$ | 130 | O | Flush acknowledge. $\overline{\text{S\_FLSHACK}}$ is asserted by the PCI2030 to indicate that the internal write posting is suspended. $\overline{\text{S\_FLSHACK}}$ remains asserted until the write posting buffers are empty. |

### power supply

| TERMINAL NAME | TERMINAL NO. | FUNCTION |
|---|---|---|
| GND | 5, 19, 22. 30, 33, 49, 53, 63, 77, 86, 93, 103, 107, 121, 136, 146, 151, 161, 165, 169 | Device ground terminals |
| $V_{CC}$ | 12, 26, 36, 40, 56, 66, 70, 84, 89, 100, 114, 128, 139, 144, 153, 158, 172 | Power-supply terminal for core logic (3.3 V) |
| P_$V_{CCP}$ | 14, 28, 42, 149, 156, 174 | Primary bus-signaling environment supply. P_$V_{CCP}$ is used in protection circuitry on primary bus I/O signals. |
| S_$V_{CCP}$ | 59, 79, 98, 117, 141 | Secondary bus-signaling environment supply. S_$V_{CCP}$ is used in protection circuitry on primary bus I/O signals. |

### absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Supply voltage range: $V_{CC}$ . . . . . –0.5 V to 4.6 V
$V_{CCP}$ . . . . . –0.5 V to 6 V
Input voltage range, $V_I$: Standard . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$: Standard . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) (see Note 2) . . . . . ±20 mA
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Virtual junction temperature, $T_J$ . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers. $V_I$ > $V_{CC}$ does not apply to fail-safe terminals.
2. Applies to external output and bidirectional buffers. $V_O$ > $V_{CC}$ does not apply to fail-safe terminals.

### recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_t$ | Input transition (rise and fall) time | CMOS compatible | 1 | | 4 | ns |
| $T_A$ | Operating ambient temperature range | Commercial | 0 | 25 | 70 | °C |
| $T_J$‡ | Virtual junction temperature | Commercial | 0 | 25 | 115 | °C |

‡ These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.

### recommended operating conditions for PCI interface

| | | | OPERATION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage | Commercial | 3.3 V | 3 | 3.3 | 3.6 | V |
| $V_{CCP}$ | PCI supply voltage | Commercial | 3.3 V | 3 | 3.3 | 3.6 | V |
| | | | 5 V | 4.75 | 5 | 5.25 | |
| $V_I$ | Input voltage | | 3.3 V | 0 | | $V_{CCP}$ | V |
| | | | 5 V | 0 | | $V_{CCP}$ | |
| $V_O$§ | Output voltage | | 3.3 V | 0 | | $V_{CCP}$ | V |
| | | | 5 V | 0 | | $V_{CCP}$ | |
| $V_{IH}$¶ | High-level input voltage | CMOS compatible | 3.3 V | 0.5 $V_{CCP}$ | | | V |
| | | | 5 V | 2 | | | |
| $V_{IL}$¶ | Low-level input voltage | CMOS compatible | 3.3 V | | | 0.3 $V_{CCP}$ | V |
| | | | 5 V | | | 0.8 | |

§ Applies to external output buffers
¶ Applies to external input and bidirectional buffers without hysteresis

## electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | SIDE | TEST CONDITIONS | OPERATION | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –0.5 mA | 3.3 V | 0.9 $V_{CC}$ | | V |
| | | | $I_{OH}$ = –2 mA | 5 V | 2.4 | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 1.5 mA | 3.3 V | | 0.1 $V_{CC}$ | V |
| | | | $I_{OL}$ = 6 mA | 5 V | | 0.55 | |
| $I_{IH}$ | High-level input current | Input pins | $V_I = V_{CC}$† | 3.6 V | | 10 | µA |
| | | | | 5.25 V | | 20 | |
| | | I/O pins‡ | $V_I = V_{CC}$† | 3.6 V | | 20 | |
| | | | | 5.25 V | | 25 | |
| $I_{IL}$ | Low-level input current | Input pins | $V_I$ = GND | 3.6 V to 5.25 V | | –1 | µA |
| | | I/O pins‡ | $V_I$ = GND | 3.6 V to 5.25 V | | –20 | |
| $I_{OZ}$ | High-impedance output current | | $V_O = V_{CCP}$ or GND | | | ±20 | µA |

† For PCI pins, $V_{CC} = V_{CCP}$.
‡ For I/O pins, the input leakage current includes the off-state output current $I_{OZ}$.

## PCI clock/reset timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1, Figure 2, and Figure 3)

| | | ALTERNATE SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_c$ | Cycle time, PCLK | $t_{cyc}$ | 30 | ∞ | ns |
| $t_{wH}$ | Pulse duration, PCLK high | $t_{high}$ | 11 | | ns |
| $t_{wL}$ | Pulse duration, PCLK low | $t_{low}$ | 11 | | ns |
| $\Delta v/\Delta t$ | Slew rate, PCLK | $t_r$, $t_f$ | 1 | 4 | V/ns |
| $t_w$ | Pulse duration, RSTIN | $t_{rst}$ | 1 | | ms |
| $t_{su}$ | Setup time, PCLK active at end of $\overline{\text{RSTIN}}$ (see Note 3) | $t_{rst\text{-}clk}$ | 100 | | µs |

NOTE 3: The setup and hold times for the secondary are identical to those for the primary; however, the times are relative to the secondary PCI close.

## PCI timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4 and Figure 1 and Figure 4)

| | | | ALTERNATE SYMBOL | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time | PCLK to shared signal valid delay time | $t_{val}$ | $C_L$ = 50 pF, See Note 5 | | 11 | ns |
| | | PCLK to shared signal invalid delay time | $t_{inv}$ | | 2 | | |
| $t_{en}$ | Enable time, high-impedance-to-active delay time from PCLK | | $t_{on}$ | | 2 | | ns |
| $t_{dis}$ | Disable time, active-to-high-impedance delay time from PCLK | | $t_{off}$ | | | 28 | ns |
| $t_{su}$ | Setup time before PCLK valid | | $t_{su}$, See Note 6 | | 7 | | ns |
| $t_h$ | Hold time after PCLK high | | $t_h$, See Note 6 | | 0 | | ns |

NOTES: 4. This data sheet uses the following conventions to describe time (t) intervals. The format is: $t_A$, where *subscript A* indicates the type of dynamic parameter being represented. One of the following is used: $t_{pd}$ = propagation delay time, $t_d$ = delay time, $t_{su}$ = setup time, and $t_h$ = hold time.
5. PCI shared signals are AD31–AD0, C/$\overline{\text{BE3}}$–C/$\overline{\text{BE0}}$, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{STOP}}$, IDSEL, $\overline{\text{DEVSEL}}$, and PAR.
6. The setup and hold times for the secondary are identical to those for the primary; however, the times are relative to the secondary PCI close.

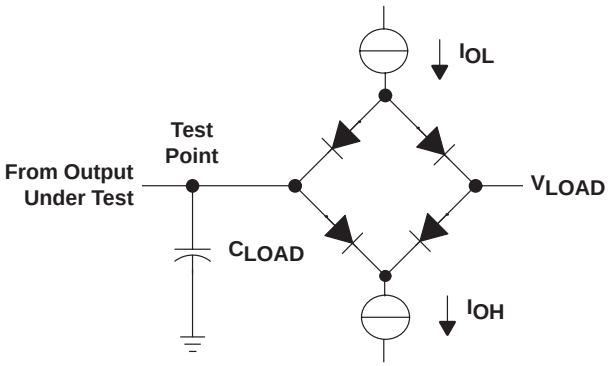
## PARAMETER MEASUREMENT INFORMATION

**LOAD CIRCUIT PARAMETERS**

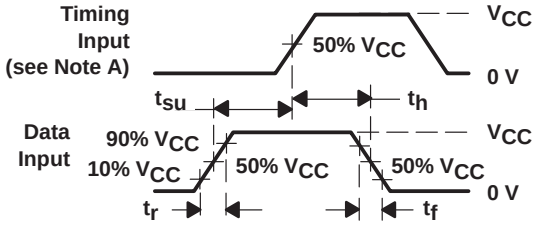
| TIMING PARAMETER | | $C_{LOAD}$† (pF) | $I_{OL}$ (mA) | $I_{OH}$ (mA) | $V_{LOAD}$ (V) |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 50 | 8 | –8 | 0 |
| | $t_{PZL}$ | | | | 3 |
| $t_{dis}$ | $t_{PHZ}$ | 50 | 8 | –8 | 1.5 |
| | $t_{PLZ}$ | | | | |
| $t_{pd}$ | | 50 | 8 | –8 | ‡ |

† $C_{LOAD}$ includes the typical load-circuit distributed capacitance.

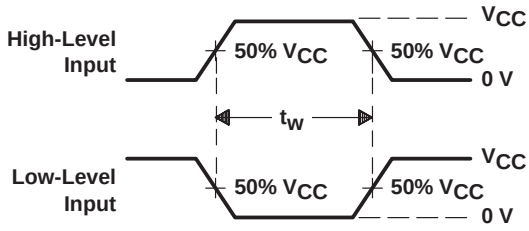
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where $V_{OL}$ = 0.6 V, $I_{OL}$ = 8 mA



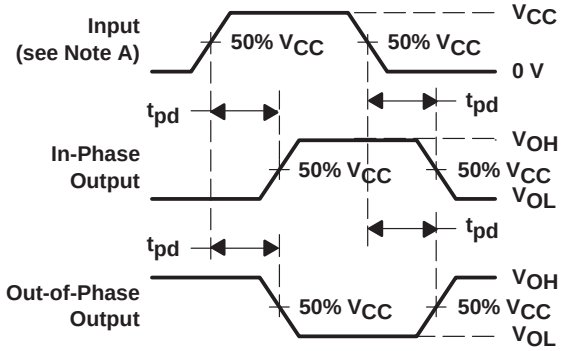

**LOAD CIRCUIT**



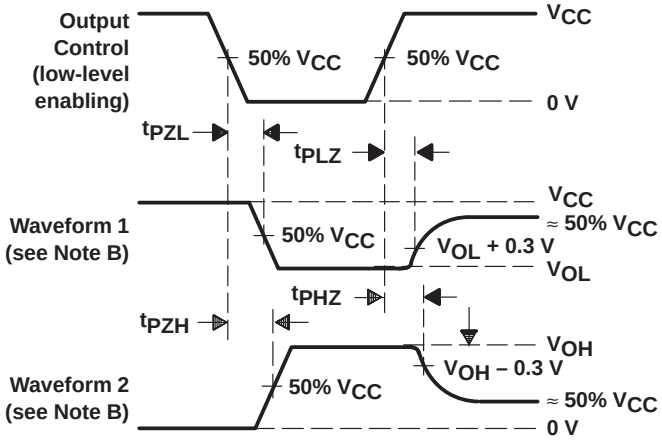

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
**INPUT RISE AND FALL TIMES**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**




**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, $Z_O$ = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. For $t_{PLZ}$ and $t_{PHZ}$, $V_{OL}$ and $V_{OH}$ are measured values.

**Figure 1. Load Circuit and Voltage Waveforms**

## PCI BUS PARAMETER MEASUREMENT INFORMATION

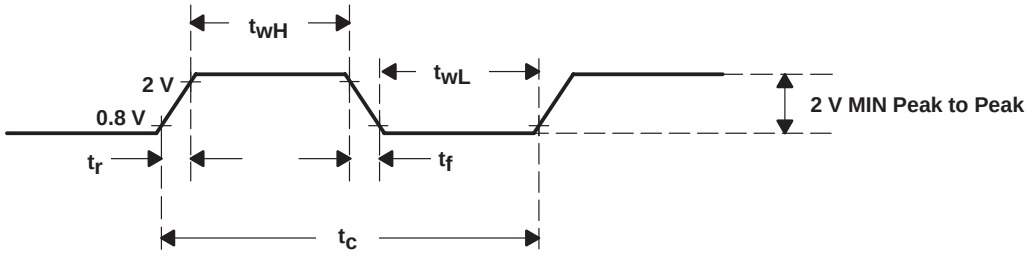



**Figure 2. PCLK Timing Waveform**

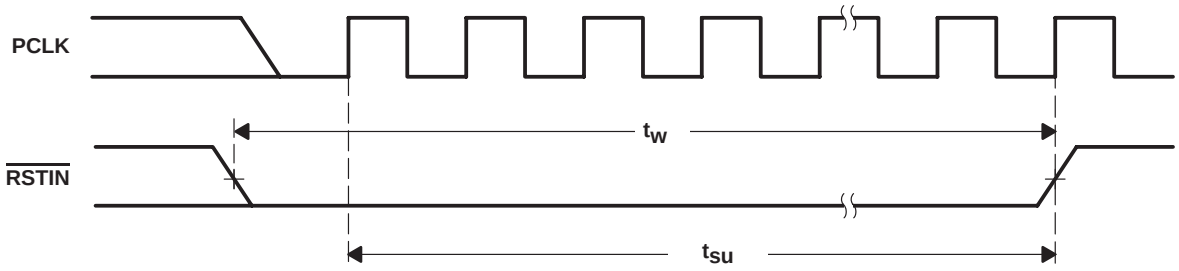



**Figure 3. $\overline{RSTIN}$ Timing Waveforms**

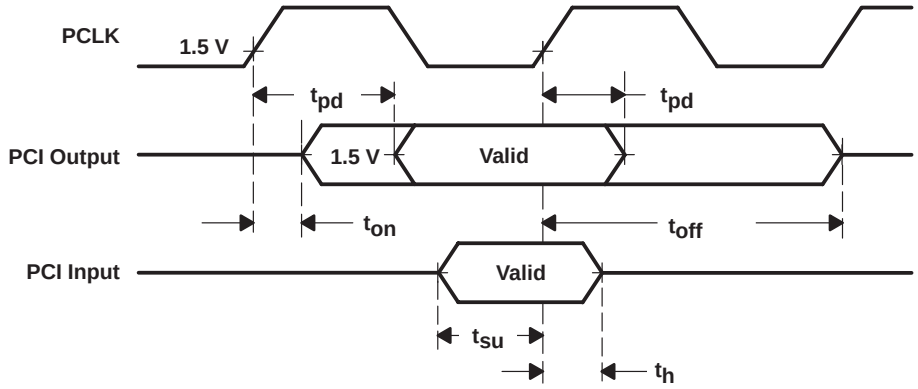
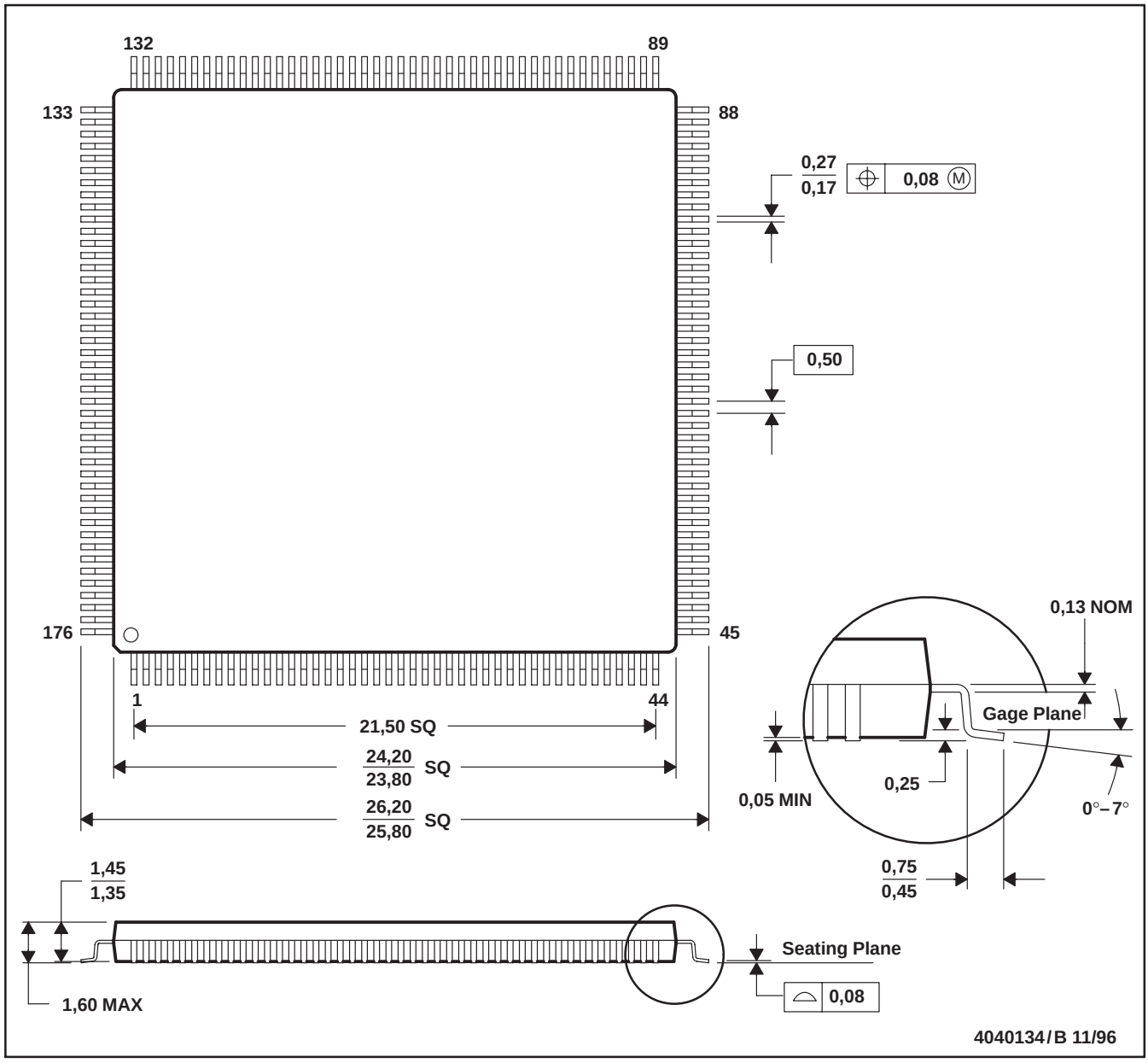



**Figure 4. Shared-Signals Timing Waveforms**

## MECHANICAL DATA

**PGF (S-PQFP-G176)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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