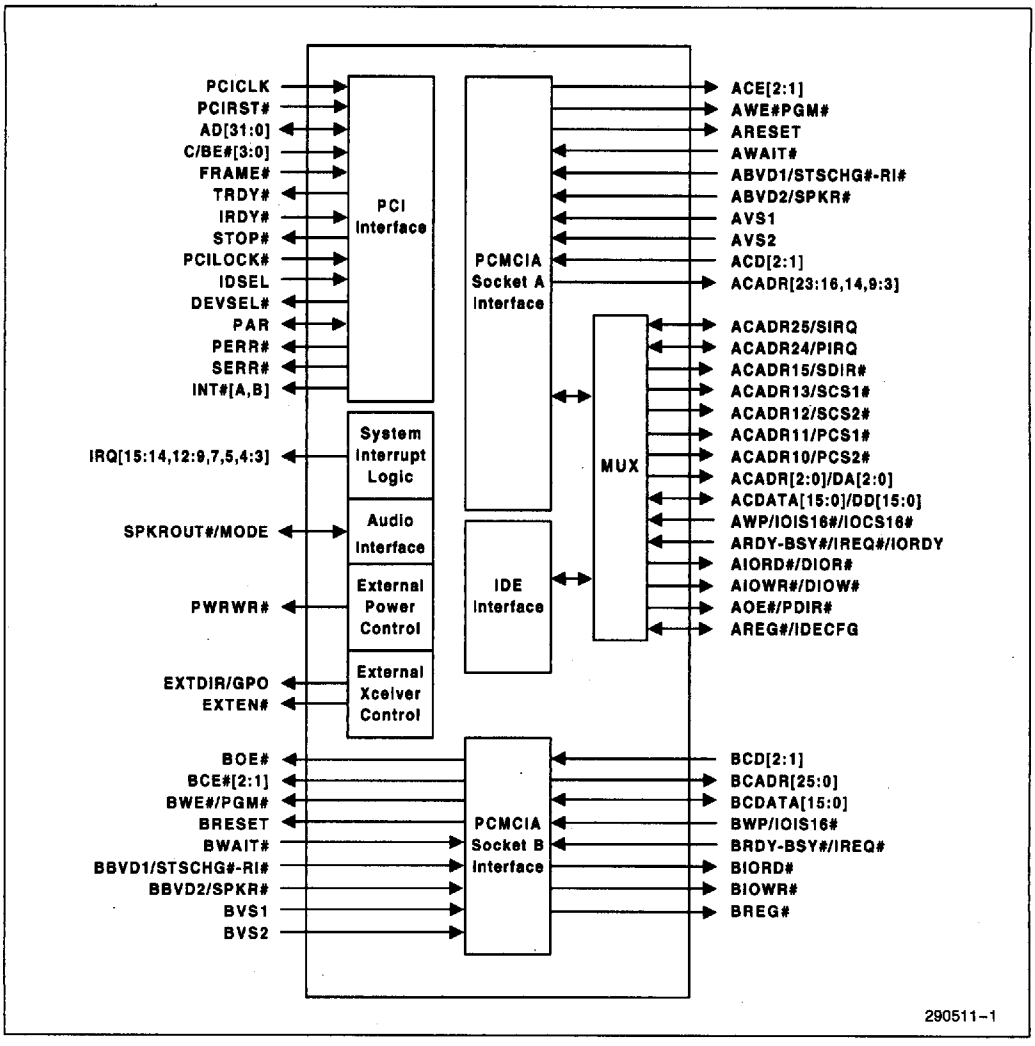
82092AA
PCI TO PCMCIA/ENHANCED-IDE CONTROLLER

- **Provides the Ultimate Plug and Play Solution for High Performance PCI Desktop Systems**
  - **Supports Combinations of PCMCIA and Enhanced Local Bus IDE Interfaces**
  - **Contains a 32-bit PCI Local Bus Slave Interface Running at 25/33 MHz**
  - **Supports Motherboard and Add-In Card Implementations**
- **Compliant with PCMCIA 2.1/JEIDA 4.1 Interface Standard**
  - **Supports up to Four 68-pin Standard PC Card Sockets, Cascadable for Additional Sockets**
  - **Each Socket Interchangeably Supports Either Memory or I/O PC Cards**
  - **Software Compatible with the Industry Standard 82365SL PCIC**
  - **Supports PCMCIA-ATA Disk Drive Devices**
  - **Features Prefetch Read and Post Write Data Buffer for PCMCIA Memory Cycles**
- **System Bus Timings Compatible with Pentium™ Processors and Intel486™ Processors**
  - **Supports All Intel PCIsets**
  - **Programmable PCMCIA and IDE Interface Timing**
  - **Easily Configured to Support Other Standard Architectures**
- **Dual Voltage Operation**
  - **Each PCMCIA Socket Automatically Configures to Support Either 3.3V or 5.0V PC Cards**
- **Power Management**
  - **Individual Socket Power Control**
  - **Hot Insertion and Removal Capability**
- **PCI Local Bus Interfaces for Four Enhanced IDE Devices**
  - **Provides Write Posting and Read Prefetching to Support High Performance IDE Devices**
  - **Primary and Secondary IDE Devices can be Independently Programmed for Various Speed Selections**
- **Flexible System Configuration Options**
  - **Two-Socket Configuration with On-Chip Buffering**
  - **Four-Socket Configuration with Partial External Buffering**
- **Eliminates the Need for System Configuration Jumpers**
  - **Address Mapping for PCMCIA 2.1/JEIDA 4.1 PC Card Memory**
  - **Address Windowing for I/O Space**
  - **Full 4-GByte PCI Address Range**
  - **Selectable Interrupt Steering from PC Cards to System Interrupt Lines**
- **208-Pin QFP Package**

The 82092AA is a high-bandwidth, software-configurable bridge that interfaces as many as four PCMCIA/ExCA (PC Memory Card International Association/Exchangeable Card Architecture) PC cards and four enhanced IDE devices to the Peripheral Component Interconnect (PCI) Bus. It is software compatible with the Intel 82365SL PC Card Interface Controller, but features a 32-bit PCI interface for maximum system performance. The PPEC simplifies system design by reducing component count between the PCI Bus, PC cards, and IDE devices, and maximizes system flexibility by providing such benefits as PC card select decoding, multiple memory address translation maps, power management, and I/O interrupt steering. The PPEC also supports auto-configuration, allowing dynamic system setup when inserting and removing PC Cards.

October 1995
Order Number: 290511-002



Mode 0 (Two Socket) Block Diagram

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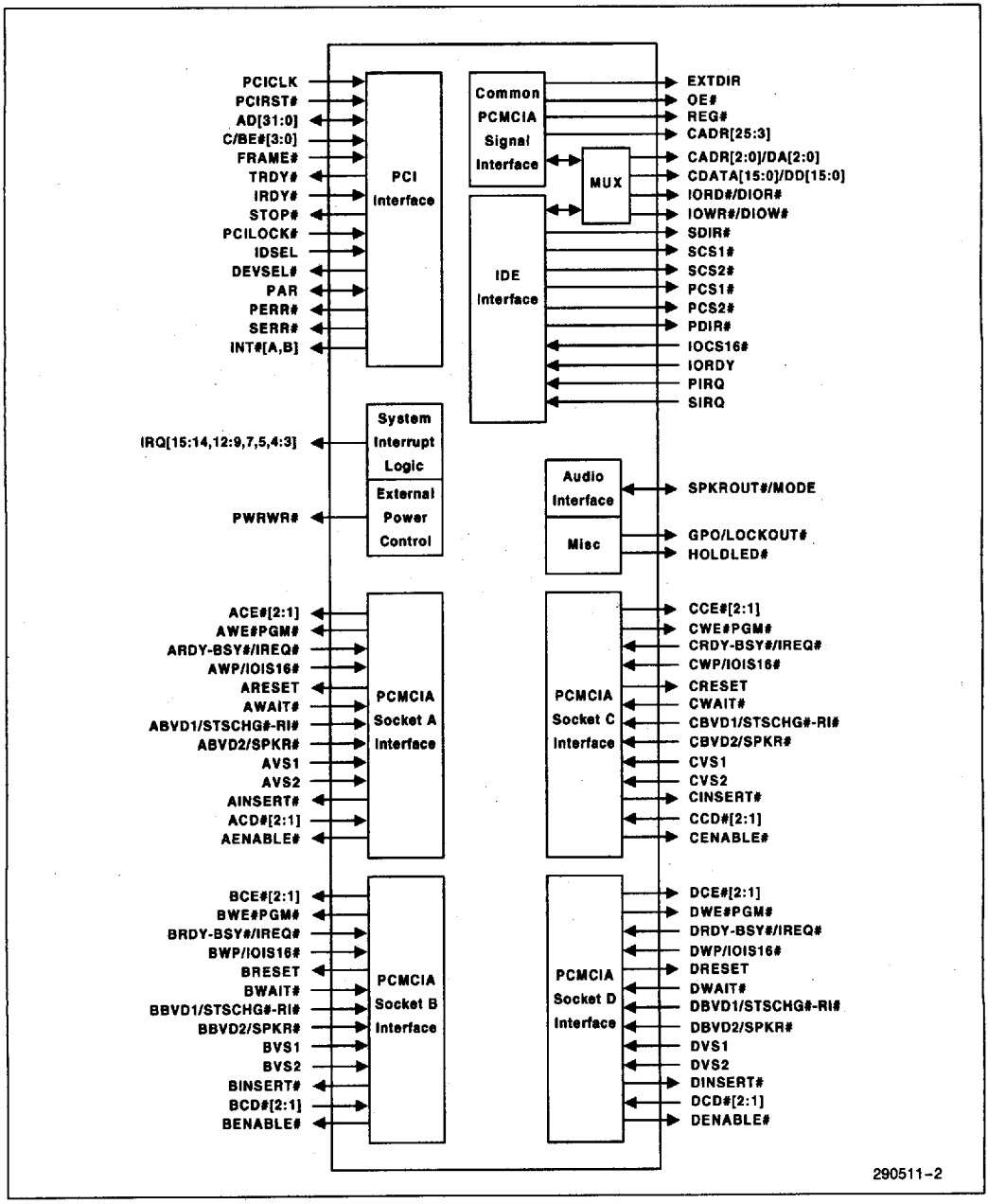

Mode 1 (Four Socket) Block Diagram

82092AA
PCI TO PCMCIA/ENHANCED-IDE CONTROLLER

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1.0 INTRODUCTION

The PPEC is a follow-on product to the Intel industry standard 82365SL PC Card Interface Controller (PCIC) used in mobile systems. It enhances the 82365SL definition by providing a full 32-bit PCI interface for increased system performance, and by supporting up to four PCMCIA sockets and four local bus IDE devices for greater flexibility. The PPEC is 82365SL compatible, and provides a standard system interface for PC Cards at the hardware and data interchange level.

Figure 1 shows a typical PPEC system implementation. The PPEC interfaces directly to the 5.0V PCI Local Bus, and supports four PCMCIA cards and four IDE devices in the configuration that is shown. The PPEC operates as a slave over the full PCI frequency range, but is optimized for 25 MHz and 33 MHz.

PPEC Configuration Modes

The PPEC supports two configuration modes that allow selection of the number of PC Card sockets supported, the number of IDE interfaces supported, and the type of buffering for each socket.

Mode 0 configures the PPEC for two independent PCMCIA sockets, or for one PCMCIA socket and two IDE interfaces. The sockets are internally buffered, and allow hot (power-on) card insertion and extraction. Each of the two IDE interfaces supports two IDE devices.

Mode 1 configures the PPEC for up to four PCMCIA sockets and two IDE interfaces. External buffering is used for the address, data, and shared control signals if fully-buffered interfaces are required. Each of the two IDE interfaces supports two IDE devices, as in Mode 0.

Each PPEC PCMCIA/JEIDA card interface consists of 60 signal and 8 power connections. In Mode 0, each of the two PCMCIA sockets has its own set of signals and buses, but the IDE interface signals are multiplexed with Socket A signals. In Mode 1, one address bus, one data bus, and several control signals are used as common signals for all four sockets, and several IDE interface signals are multiplexed with the common signals.

1.1 Enhanced PCI Local Bus IDE Interface

The local bus IDE interfaces, designated the Primary IDE Interface and the Secondary IDE Interface, and their corresponding drives #0 and #1 are independently programmed to operate in the enhanced (programmable) timing mode, or in standard compatible timing mode. The IDE physical interface is multiplexed with existing PCMCIA signals to reduce cost, and the IDE controller uses internal PCMCIA Post-Write data buffers and separate Read-Prefetch buffers to improve the system performance. The interfaces are externally buffered in both PPEC configuration modes.

The PPEC provides an IDE Hardware Configuration mechanism using the Power-On IDE Configuration Register which is mapped in the PCI configuration space. This allows full use of the PPEC's Enhanced Fast Local Bus IDE without any requirement for BIOS upgrade or modification if the BIOS is not aware of the PPEC IDE.

The higher performance of the PCI local bus IDE architecture with respect to the ISA IDE architecture results from the faster timing modes that are available in the PCI local bus IDE architecture. The PPEC provides improved timing even when the IDE controller is configured to run cycles that correspond to IDE ATA specification timing modes 0, 1 or 2 (which are originally defined for ISA-based systems) because of the proximity to the host CPU, and because of the clock granularity (PCI 33 MHz) at which timing is controlled. A more significant improvement is obtained when the PPEC is configured for the drives that support enhanced timing mode 3 or any arbitrarily-defined faster timing mode.

Enhanced Timing

The PPEC features programmable timing (see Primary and Secondary IDE Timing Control Register descriptions) in the form of clock counts for the following timing parameters:

- T_{su} (address/data set-up time)
- T_{pw} (command pulse width)
- T_{cyc} (overall cycle length)

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The programmable timing allows support of currently defined and future IDE Modes, and for optimizations based on PCI clock frequencies other than 33 MHz. IDE Primary and Secondary interface timing is independently controlled, allowing IDE drives with different timing characteristics to be supported by the same physical interface while still operating at their optimum speeds.

Further timing configuration is provided at the level of the Primary and Secondary interface. Each drive (drive 0 and drive 1) can be independently programmed to run in enhanced timing mode or in standard compatible Mode #0, so that any combination of fast and slow drives is possible.

1.2 Internal Register and PCMCIA Address Window Access

The PCI-PCMCIA Bridge PCI Configuration Registers and the PCI-IDE PCI Configuration Registers conform to the Peripheral Component Interconnect (PCI) specification. The specification describes the essential registers that must be supported by PCI devices and functions, and should be referenced for a detailed explanation of the PCI-PCMCIA Bridge and PCI-IDE PCI Configuration Register access.

1.2.1 PCMCIA SOCKET CONFIGURATION REGISTER ACCESS

The PCMCIA Socket Configuration registers, comprised of general setup registers, interrupt registers, I/O mapping control registers, and memory mapping control registers, are used for control of the PCMCIA socket functions. They are a superset of the 82365SL register set, and are accessed using the same indexing method that is used in the 82365SL.

Two read/write ports, an *index port* and a *data port,* are used to access the registers. The index port is written with the register offset that is used to access the register. Data is then written to the register or read from the register via the data port.

The index port address is loaded into the PCI-PCMCIA Bridge Base Address Register, which is located in PCI Configuration space. The data port address is the next location (index port address + 1). When writing to the configuration registers, the index and data registers may be accessed simultaneously with a 16-bit write operation to increase performance. The index value is placed on data bits[7:0], and the data value to be written is placed on data bits[15:8].

The PPEC does not respond to a data port read or write operation unless a valid index has first been written to the index port.

1.2.2 PCMCIA MEMORY WINDOWS

The PPEC supports five independently enabled and configured memory and I/O address mapping windows for each PCMCIA PC Card socket. The windows allow portions of 64 MByte common memory and/or 64 MByte attribute memory spaces on the PC Cards to be mapped to portions of the PCI Memory address. Each window's data bus width, PCMCIA interface timing, software write protect, and enable can be independently controlled. Mapping of each memory window can start and stop on any 4 KByte boundary of PCI memory space within a 16 MByte page.

A Card Memory Page Address Register associated with each socket allows selection of the 16 MByte window page anywhere in the 4 GByte PCI address space (see Figure 2). The PC Card memory offset address is added to the PCI address bits 23:12 to generate the address for the PC Card. The address mapping is compatible with the 82365SL.

A window is opened by writing the PCI Memory start address, PCI Memory stop address, and PC Card memory offset to the window's *System Memory Address Mapping Start, System Memory Address Mapping Stop, and Card Memory Offset Address* high and low byte registers. The Card Memory Page Address Register must be written with the window's 16 MByte page address in PCI memory space, and the window must be enabled in the Address Window Enable Register.

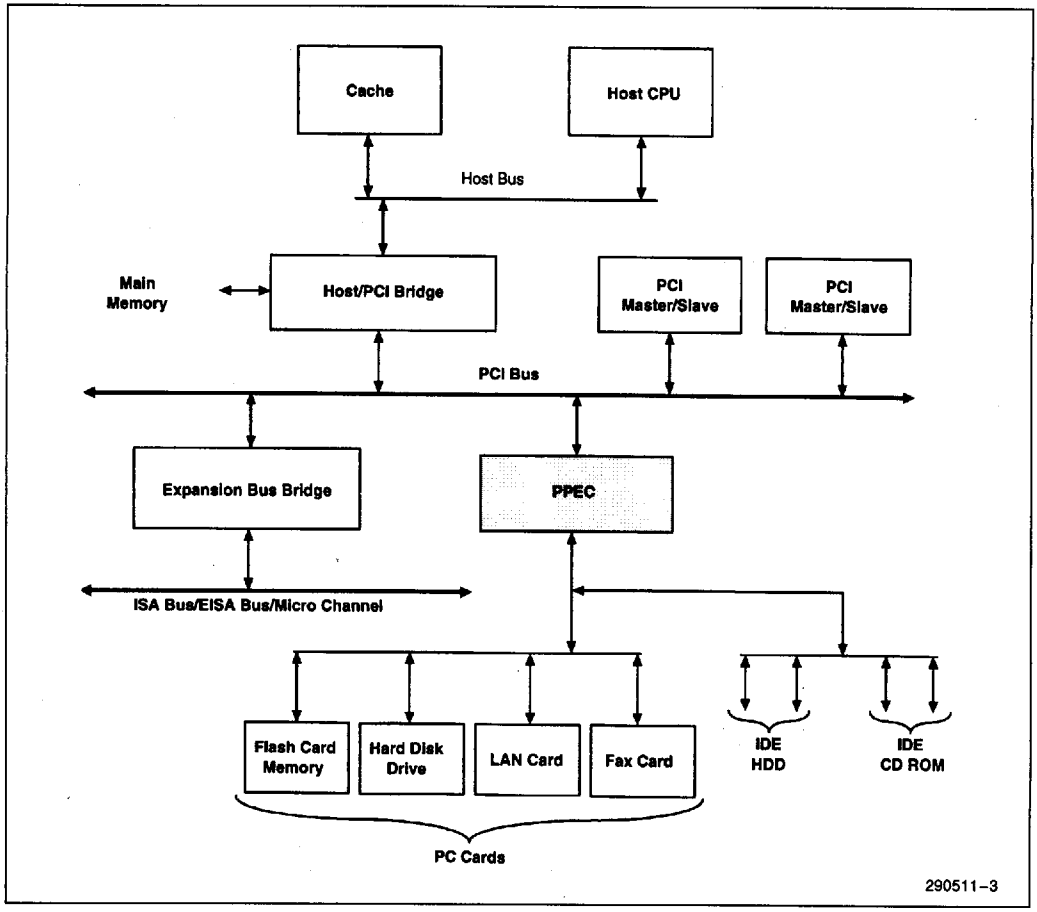

Figure 1. Typical PPEC System Implementation

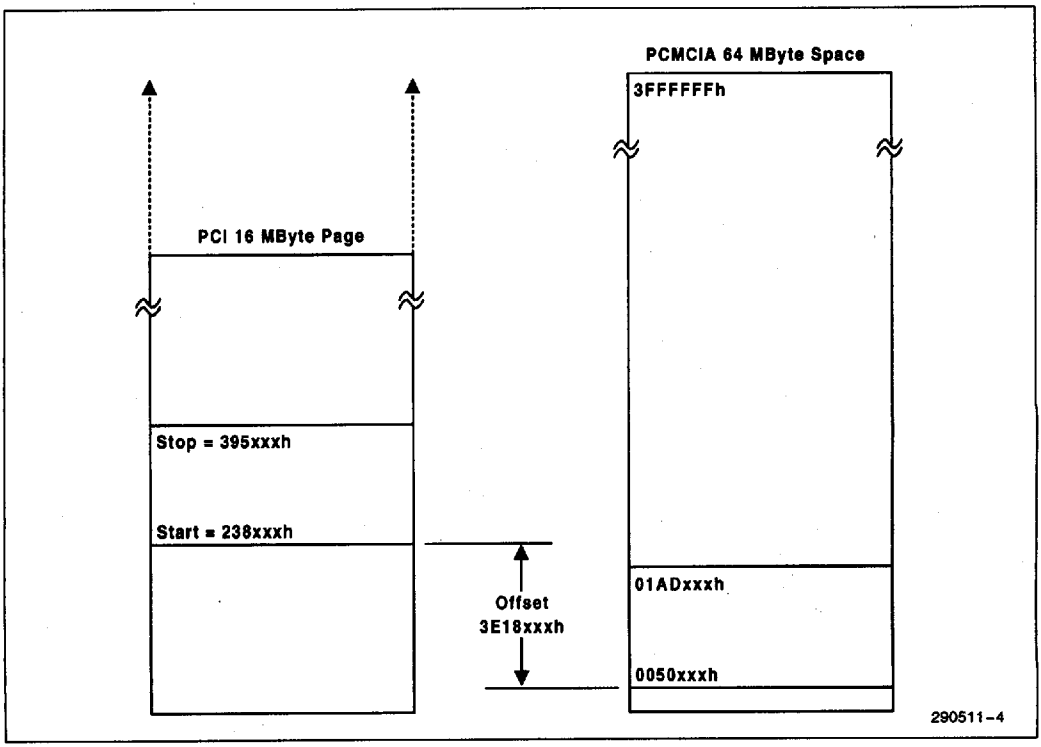

Figure 2. PCMCIA Memory Address Mapping

Common/Attribute Memory Address Mapping

Both Common and Attribute memory can be accessed on the PC Card through any of the PCI Memory address mapping windows according to the state of the *Register Active* bit in the Card Memory Offset Address High Byte Register. When this bit is set to 0, common memory can be accessed; when set to one, attribute memory can be accessed. The PCI memory window to common or attribute memory can be mapped from any PCI address to any PC Card address.

Several PCI Memory address mapping windows to different common memory address spaces can be opened simultaneously. Each of these windows can be configured to use a different timing mode, software write protect, and data width.

1.2.3 PCMCIA I/O WINDOWS

The PPEC features two independently enabled and controlled I/O address windows for each PCMCIA PC Card socket. The windows can be non-contiguous, and each window's I/O data bus width can be independently controlled. The windows have a 1 byte addressing resolution.

I/O addressing of PC Cards is very similar to memory addressing. Each I/O address window has a 16-bit *start address* and a 16-bit *stop address* located in the window's *I/O Address Start* and *I/O Address Stop* high and low byte registers. PCI I/O Address bits[15:0] are compared with the start and stop addresses and must be greater than or equal to the start address, and less than or equal to the stop address for access to the window. PCI address bits[31:16] must be 0 when addressing I/O Cards.

Indirect offset addressing is not supported for I/O windows. PCI I/O Address bits[15:0] are passed directly to the PC Card address pins if they fall within an I/O Window. Bits[25:16] of the PC Card address are driven low.

1.3 Data Buffers

The PPEC features read prefetching and write posting data buffering for up to four Dwords. This allows high speed 32-bit data transfers between the PCI Local Bus and the PPEC, and lower-speed 8-bit and 16-bit data transfers between the PPEC and the PC Cards and the IDE devices. Assembly/disassembly logic translates 32-bit data from the PCI bus into 8- and 16-bit data required by the PCMCIA PC Cards and the IDE devices.

Figure 3 shows a representation of the data buffer and the IDE prefetch buffers. The same physical buffers are used for both PCMCIA/IDE Posted Write operations, and for PCMCIA Prefetch operations. Separate 32-bit latches are used for storing IDE Prefetch data: one for the Primary drive interface, and one for the Secondary drive interface.

The operation of the data buffers is controlled by two bits in the PCI-PCMCIA Configuration Control Register that enable and disable Posted Write Buffer and IDE Prefetch operation. Both modes may be active simultaneously, but the write posting function has priority over the prefetch function.

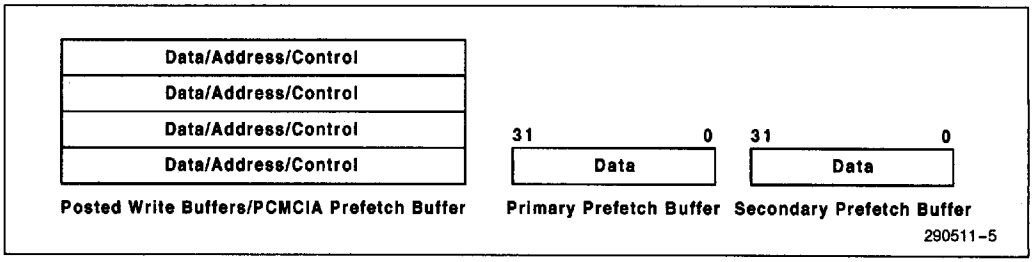

Figure 3. Data and IDE-Prefetch Buffers

Posted Writes and Prefetch Reads for IDE cycles are globally enabled in the PCI-PCMCIA PCI Configuration Control Register, and individually enabled for each IDE device in the PCI-IDE Configuration Control Register. IDE Posted Write cycles operate the same way as PCMCIA Posted Write cycles. However, the PPEC does not support burst data transfers for IDE Posted Write operations.

The data buffers are not used for Attribute Memory cycles because of potential timing dependencies.

1.4 PCMCIA Interface

The PPEC configuration mode is selected by an external 10-20K Ohm resistor on the SPKROUT#/MODE pin. The voltage level applied to the pin is sampled at the end of the reset sequence, and the state is stored internally in the PPEC-PCMCIA PCI Configuration Control Register (PCICON). The pin is then reconfigured as an output to support the SPKROUT function. The AREG#/IDECFG pin is also sampled at the end of the reset sequence to determine whether IDE is supported in Mode 0.

Table 1 shows mode selection with the SPKROUT#/MODE and AREG#/IDECFG pins.

Mode 0

Two PCMCIA sockets are supported in Mode 0. Each socket interface (Socket A and Socket B) has its own data bus, address bus, and control pins.

If the AREG#/IDECFG pin is sampled high at the end of the reset sequence, the Socket A PCMCIA registers are disabled and the Socket A interface pins are reconfigured for IDE support, allowing the implementation of two Fast Local Bus IDE interfaces capable of supporting up to four IDE devices. Signal mapping for the IDE Interface in Mode 0 is described in Section 2.8, IDE Interface Signals.

Mode 1

Four PCMCIA sockets are supported in Mode 1 by allowing sockets A, B, C, and D to share a common data bus (CDATA[15:0]), a common address bus (CADR[25:0]), and four common control signals (REG#, OE#, IORD#, and IOWR#). The other control signals are not shared.

External data buffers for each PCMCIA Socket may be used in Mode 1 to prevent the PC Cards from driving an excessive load, and to allow both 3.3V and 5V cards to be used simultaneously in a system. External buffers for the shared address and control lines are optional. They can be fully buffered for each socket or, by utilizing the INSERT# pins, can be either driven directly by the PPEC, or buffered by a single buffer to increase drive strength. See the *PPEC Design Guide* for specific application information.

Table 1. Configuration Mode Selection

SPKROUT#/MODE	AREG#/IDECFG	Mode	Configuration
0	0	0	2 Fully-Buffered PCMCIA Sockets; No IDE
0	1	0	PCMCIA Socket B Only; Dedicated IDE Interface
1	X	1	4-PCMCIA Sockets; Shared Address, Data, Control

Two Fast Local Bus IDE interfaces can be enabled in Mode 1 by programming the PPEC-IDE Interface PCI Configuration Registers. When an IDE cycle is initiated, the PDIR# and SDIR# pins provide direction control for the external IDE data buffers, and the PCS1#, PCS2#, SCS1# and SCS2# signals enable the IDE devices. The PCMCIA sockets are not affected during IDE cycles because the card enables for each socket remain inactive.

The AREG#/IDECFG pin is ignored in this mode.

1.4.1 CARD INSERTION AND EXTRACTION

The INSERT# function allows the PPEC to prepare for the insertion of a PC Card, preventing the insertion from affecting other sockets in implementations requiring shared signal lines (Mode 1, partially buffered). The INSERT# pin is driven active at least 1.5 μs prior to the PC Card signal-pin contact with a PCMCIA socket by an external circuit described in the PPEC Design Guide.

The PPEC empties the Posted Write Buffers (PWBs) and tri-states the shared PCMCIA address and control lines when a falling edge occurs on INSERT#. The PPEC drives the shared signals after power has been applied to the new PC Card, and normal operation resumes.

When a rising edge occurs on a CDx pin, the PPEC again empties the Posted Write Buffers and tri-states the shared address and control lines, and the dedicated PCMCIA socket signals. A rising edge on INSERT# indicates that the PC Card has been disconnected from the signal pins, allowing the PPEC to drive the shared signals and resume normal PCMCIA operation.

Hot insertion and extraction is possible in Mode 0 because all PCMCIA interface signals are independent of each other in this mode. When a card insertion is detected via the Card Detect inputs (xCD#[2:1]) with the Card Detect interrupt enabled, a Card Status Change interrupt is initiated, and power is applied to the PCMCIA socket under software control. When a card removal is detected via the Card Detect inputs, the voltage to the socket is turned off under software control.

1.4.2 POWER CONTROL

The PPEC implements power management for each PCMCIA socket individually. Socket power management is controlled through the Power Control Register and the VS1/VS2 pins.

1.4.2.1 Power Control Register Operation

The Power Control Register controls the routing of power to the PCMCIA socket and enabling of the PCMCIA socket interface pins. A PCIRST clears all of the bits in this register. A detailed description of all of the bits in this register is found in Section 3.2.1.3. This section describes only the V_{CC} Control and V_{PP} Control bits.

V_{CC} Control

The V_{CC} Control bits in the Power Control Register control power to the PC Cards via an external latch. The control signals $V_{CC}5V$ and $V_{CC}3V$ are routed to the external latch through the ACDATA lines during Power Control Write cycles. The value of these bits is modified by software writes to the Power Control Register or by hardware according to the value of the VS1/VS2 pins. Hardware modifies the V_{CC} Control bits only when the INSERT# signals are asserted, indicating partially buffered, Mode 1 implementations.

The V_{CC} Control bits control V_{CC} routing using the following encoding:

Power Control Register Bits		$V_{CC}5V$	$V_{CC}3V$	Description
Bit 4	Bit 3			
0	0	0	0	No Connect
0	1	0	0	Reserved
1	0	1	0	5.0 V
1	1	0	1	3.3 V

If the INSERT# signals are used in Mode 1 partially-buffered implementations, the VS1/VS2 pins are sampled during a PC Card insertion and are used to determine the values of $V_{CC}5V$ and $V_{CC}3V$. The VS1/VS2 pins affect the V_{CC} Control bits in the following way:

VS1	VS2	Power Control Register Bits		$V_{CC}5V$	$V_{CC}3V$	Description
		Bit 4	Bit 3			
0	0	1	1	0	1	3.3V
0	1	1	1	0	1	3.3V
1	0	0	0	0	0	Not Supported; (SERR# Asserted)
1	1	1	0	1	0	5.0V

In Mode 0 and in fully-buffered Mode 1 implementations, the INSERT# signals are not used, and power control is completely dependent upon software.

V_{PP} Control

The V_{PP} Control bits in the Power Control Register are latched externally, along with the V_{CC} Control bits. They are modified with software writes to the Power Control Register only.

1.4.2.2 External Power Control Latch

The PPEC is designed to directly interface with Maxim's MAX780 Dual-Slot PCMCIA Power Controller. This device provides V_{PP} power and controls V_{CC} power for 2 PCMCIA sockets. Two MAX780's are required for 4-socket implementations. The MAX780 contains an internal register for latching the power control signals provided by the 82365SL and compatible controllers $V_{PP}EN[1:0]$ and $V_{CC}EN[1:0]$. This latch allows the PPEC to write the values of the power control signals via the PCMCIA data lines, thus eliminating the need for dedicated power control signals. If the Maxim device is not used in a system, an external register (74ALS273 or equivalent) is required to latch the power control signals. This external latch, whether implemented using the Maxim device or a 74ALS273, is referred to in this document as the External Power Control Latch.

The following are the signals that transfer power control information to the External Power Control Latch, and the bus signal pins through which they are transferred.

Power Signal	Transfer Pin Name
Power Control Write Signal	PWRWR#
Socket A $V_{PP}EN0$ Control Signal	ACDATA[0]
Socket A $V_{PP}EN1$ Control Signal	ACDATA[1]
Socket B $V_{PP}EN0$ Control Signal	ACDATA[2]
Socket B $V_{PP}EN1$ Control Signal	ACDATA[3]
Socket A $V_{CC}3V$ Control Signal	ACDATA[4]
Socket A $V_{CC}5V$ Control Signal	ACDATA[5]
Socket B $V_{CC}3V$ Control Signal	ACDATA[6]
Socket B $V_{CC}5V$ Control Signal	ACDATA[7]
Socket C $V_{PP}EN0$ Control Signal (Mode 1 Only)	ACDATA[8]
Socket C $V_{PP}EN1$ Control Signal (Mode 1 Only)	ACDATA[9]
Socket D $V_{PP}EN0$ Control Signal (Mode 1 Only)	ACDATA[10]
Socket D $V_{PP}EN1$ Control Signal (Mode 1 Only)	ACDATA[11]
Socket C $V_{CC}3V$ Control Signal (Mode 1 Only)	ACDATA[12]
Socket C $V_{CC}5V$ Control Signal (Mode 1 Only)	ACDATA[13]
Socket D $V_{CC}3V$ Control Signal (Mode 1 Only)	ACDATA[14]
Socket D $V_{CC}5V$ Control Signal (Mode 1 Only)	ACDATA[15]

Note that in Mode 1, the ACDATA bus is renamed to CDATA.

The value of the $V_{CC}3V$ and $V_{CC}5V$ signals and $V_{PP}EN[1:0]$ are determined by the control bits in the Power Control register for each socket.

The External Power Control Latch is updated by placing the values of the power control signals onto the corresponding ACDATA lines, and pulsing the PWRWR# signal low. This operation takes place after each of the following conditions:

- A write cycle to any of the Power Control registers
- A high Card Detect pin on a socket having Auto Power enabled
- Rising edge of PCIRST#
- PC Card Reset
- Detection of a PC Card insertion via one of the xINSERT# pins

The PPEC allows any cycle currently taking place on the PCMCIA bus or PCI bus to complete before performing an external power control write cycle, then initiates a write cycle to the external latch. The power control write operation cycle time is 6 PCICLKs, and consists of placing the Power Control bits for all sockets on the ACDATA bus, pulsing the PWRWR# signal for 5 PCICLKs, and holding the data for one additional clock to guarantee hold time. If a PCMCIA-targeted PCI cycle is initiated during an external power control write cycle, the PCI cycle is held in wait-states until the PCMCIA cycle can be executed.

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1.4.2.3 Hardware-Initiated Power On Sequence

When the INSERT# pins are used to detect card insertions, the PCMCIA bus is tri-stated until power has been applied to all PC Cards. A condition could exist where a PCI Master device other than the CPU tries to access the PCMCIA bus while the PCMCIA bus is tri-stated, causing the PCI Master to be retried. This would effectively lock out the CPU from the PPEC and prevent the CPU from applying power to the PC Card. To avoid this situation, the PPEC must perform a hardware-initiated power-on sequence to the PC Card whenever the PCMCIA bus is tri-stated due to a PC Card insertion.

The following sequence of events describes a hardware-initiated power-on sequence:

1. INSERT# is detected active for one of the PCMCIA sockets.
2. Line buffers are flushed and the PCMCIA bus is tri-stated.
3. CD1# and CD2# are detected active.
4. The Power Control Register is updated according to the values of VS1/VS2.
5. An external power control write cycle is performed.
6. The PPEC is held for 256 PCICLKs (7.68 μs minimum) to allow V_{CC} voltage to stabilize.
7. The PCMCIA bus and The PPEC resume normal operation.

Any subsequent writes to the Power Control Registers by software override the V_{CC} Control bits set by hardware. If VS1/VS2 indicate the presence of an X.X-only PC Card, the PPEC does not apply power to the card and the PCMCIA bus is held in a tri-state condition until the card is removed. This situation is indicated by HOLDLED# remaining active. If SERR# is enabled, the PPEC asserts SERR# for one PCICLK to alert the system that an error condition exists, and operation can not continue.

1.4.2.4 Auto Power Enable

The Auto Power function in the PPEC is intended to allow hardware to automatically power down a PCMCIA socket based on the Card Detect pins (CDx). With Auto Power enabled, the power control signals $V_{CC}5V$ and $V_{CC}3V$ are active only while both Card Detect inputs are low. As soon as one of the CDx lines goes high indicating that a card is being extracted, an external power control write cycle is initiated to negate the active power control pins. The V_{PP} control pins are automatically negated with the negation of the V_{CC} control pins, independent of the Auto Power function. Software is responsible for debouncing the CDx pins and disabling Auto Power whenever a card is extracted. When the Auto Power function is disabled, the power control signals are not qualified with the Card Detects. The sequence of steps for inserting and extracting a PC Card when using Auto Power is as follows:

1. The default is Auto Power Enable = 0.
2. Software receives a Card Status Change (CSC) interrupt as a result of a card being inserted.
3. Software waits for the CDx pins to become stable.
4. Software reads the VSx pins and sets the V_{CC}/V_{PP} control bits in the Power Control Register.
5. The PPEC issues a write cycle to the external power control latch (Maxim Power Switch or discrete latch).
6. Software waits for power to become stable (50 μs minimum).
7. Software enables the socket interface and sets Auto Power Enable = 1.

Normal operation takes place.

8. The PPEC detects a rising edge on either CDx pin.
9. The PPEC sends a CSC interrupt and issues a write cycle to the external power control latch to disable the socket power. A hardware flag is automatically set, disabling power to the socket.
10. Software waits for the CDx pins to become stable.
11. Software disables the socket interface and sets Auto Power Enable = 0.
12. The PPEC clears the flag that disables power to the socket as a result of step 11.

When the Auto Power bit of the Power Control register (bit 5) is 0, Auto Power is disabled and power is controlled directly from the power control bits without being qualified with CDx. The PPEC does ***not*** prevent software from powering a card to a voltage other than that indicated by the VSx pins. Table 2 summarizes the operation of the PPEC power control.

1.5 PC Card ATA Support

The PCMCIA specification defines a protocol for ATA PC Cards. No special requirements are needed for accesses to PC Card ATA. Accesses to all ATA registers are treated as normal I/O accesses.

1.6 PCI Interface

The PPEC is a PCI target-only device. Its PCI Interface conforms to the Peripheral Component Interconnect (PCI) specification, which should be referenced for an understanding of the interface.
Table 3 identifies the PCI commands that the PPEC supports, and their encoding on signal lines C/BE#[3:0]. The PCI bus signal descriptions in the following section further define the PCI operations that are supported by the PPEC.

1.6.1 PCI SUPPORT

The following sections describe PPEC PCI support. Note that the PPEC is a target-only device, and therefore does not support PCI functions that are defined for PCI masters.

1.6.1.1 Address Decoding

The PPEC uses only positive address decode. The PPEC's PCI-PCMCIA Bridge and PCI-IDE Interface functions both have SLOW DEVSEL# timing response.

Table 2. Power Control Operation

Power Control Register			PPEC Pins		Tri-state Outputs (See Note)	Interface Status Register
Output Enable (Bit 7)	V_{CC} Enable (Bit 4)	Auto Power Enable (Bit 5)	CD1#	CD2#		PC Card Power Active
X	0	X	X	X	OFF	0
0	1	0	0	0	OFF	1
1	1	0	0	0	ON	1
X	1	0	X	1	OFF	1
X	1	0	1	X	OFF	1
0	1	1	0	0	OFF	1
1	1	1	0	0	ON	1
X	1	1	X	1	OFF	0
X	1	1	1	X	OFF	0

NOTE:
For this table, the term Tri-state Outputs includes the PPEC outputs that are unique for a given PCMCIA socket. This includes all of the address, data, and control signals in Mode 0 (2-socket), but does not include the shared address, data, and control signals in Mode 1 (4-socket). The shared PCMCIA signals defined in Mode 1 are enabled and disabled as a function of the INSERT# signals as described in Section 1.4.1.

1.6.1.2 Configuration Cycles

The PPEC supports only Type 0 PCI configuration cycles. As a multifunctional device it supports access to functions numbered 0 and 1. It does not respond to a configuration cycle that accesses functions 2-7, even if the functions are selected with the IDSEL mechanism.

NOTE:
None of the PPEC internal registers or PCMCIA I/O or memory locations can be accessed after PCI reset until PCI Configuration Software (part of BIOS) configures the system resources properly.

1.6.1.3 Burst Transfer Support

The PPEC supports burst transfers to PCMCIA memory and to the IDE I/O Data Port with a post-write buffering mechanism when internal data buffering is enabled.

The PPEC supports only Linear Incrementing burst transfers. Attempts to access the PPEC using burst transfers in a mode other than Linear Incrementing results in subsequent target disconnects, and splitting of the burst cycle into multiple single data phase transfers.

1.6.1.4 Exclusive (Locked) Access Support

The PPEC can be locked as a resource by any PCI Initiator. In the context of locked cycles, the PPEC and the PCMCIA subsystem are considered a single resource. A locked access to any address within the PCMCIA subsystem locks the PPEC.

Note that write-posting and read-prefetch are disabled for PCI locked cycles. Any PCI Initiator access to the PPEC subsystem while it is locked results in retry.

Table 3. PCI Commands

C/BE# [3:0]	Command Type	Supported As Target
0000	Interrupt Acknowledge	No
0001	Special Cycle	No
0010	I/O Read	Yes
0011	I/O Write	Yes
0100	Reserved	N/A(3)
0101	Reserved	N/A(3)
0110	Memory Read	Yes
0111	Memory Write	Yes
1000	Reserved	N/A(3)
1001	Reserved	N/A(3)
1010	Configuration Read	Yes
1011	Configuration Write	Yes
1100	Memory Read Multiple	No(2)
1101	Reserved	N/A(3)
1110	Memory Read Line	No(2)
1111	Memory Write and Invalidate	No(1)

NOTES:
1. Treated as Memory Write.
2. Treated as Memory Read.
3. PPEC does not respond on these commands.

1.6.1.5 Transaction Termination

As a target, the PPEC terminates transactions for the following conditions.

Disconnect

The PPEC responds with a disconnect when it is the target of multiple data phase transactions that cannot be serviced by the internal buffers (i.e., posted for writes or supply prefetched data during read operations). During posting, the PPEC terminates the cycle using disconnect semantics as soon as all posted write buffers are occupied. Similarly, the PPEC disconnects during burst reads as soon as a miss is generated (prefetch data is not available). This is because the next data phases would exceed the 8 PCI clock incremental latency limit while the PCI is kept in wait-states for more that 8 PCI clocks until one of the post write buffers is emptied to its destination, or additional data is fetched from the PCMCIA card or IDE interface.

Retry

The PPEC retries memory write cycles when all post write buffers are full. It also retries any cycle when it is locked as a resource and a PCI master tries to access the PPEC without negating the PCILOCK# signal during the address phase.

Target Abort

The PPEC generates this type of termination during non-aligned Dword I/O transfers with illegal combinations of address and BEx.

1.6.1.6 Parity Generation And Checking

The PPEC supports parity generation and checking for both the address and data phases of cycles in which it positively decodes address. The PPEC asserts the PERR# signal when it recognizes a parity error during bus transactions in which it is involved. The PPEC asserts the SERR# o/d signal for one PCI clock when it detects an address phase parity error, or a PCMCIA interface system error (i.e., when a X.XV-only PC Card is inserted).

1.6.1.7 PCI Memory Cache Support

The PCI can provide basic cache coherency control with two optional PCI signals, SDONE and SBO#. The PPEC does not support those signals, so PCMCIA memory cannot be directly cached. However, alternative schemes can be used (including "shadowing" in main memory and caching locally) to speed access to the read-only PCMCIA memory. This can improve performance of the XIP (eXecute In Place) PCMCIA applications.

1.7 System Interface Functionality

The PPEC can connect to system interrupts in two different ways:

a. via 10 direct system interrupt signals.

b. via 2 PCI interrupt signal lines which require additional routing.

The direct system interrupt mode is provided so that PCMCIA software that requires "ISA compatibility" (i.e. non-shareable IRQ handlers which require specific IRQ level) can run without modifications on Intel Microprocessor Architecture based platforms with PPEC as a PCI-PCMCIA Bridge. In this case, PCI interrupts are not used but the PCMCIA Card interrupts (as well as the Card Status Change interrupt) are configured to connect directly to specific system IRQ lines. On the system side, the PPEC interrupt signals can support either edge (ISA like) or level (active low-EISA, Microchannel, PCI like) triggering. Multiple PC Cards in a system can conflict if they try to utilize the same Edge interrupt Level. By steering them to different interrupt lines, the conflicts can be eliminated.

Designs that are not dependent on this type of software "compatibility" can use PCI interrupts (i.e., interrupt is configured using mechanism "b").

The Global Control Register provides individual bits to enable Edge/Level Mode. The Interrupt and General Control Register contains bits for I/O card Interrupt Steering. The Card Status Change Interrupt Configuration register contains bits for Card Status Change Interrupts.

1.7.1 DIGITAL AUDIO SUPPORT—SPKROUT# SIGNAL

The PPEC supports PC Card digital audio SPKR# signals. These signals are passed through to the SPKROUT# line, which is an exclusive-OR of all SPKR# inputs (from all sockets). In motherboard designs, this output line can be connected to the system speaker driver directly. In add-in card implementations, a cable can be used to access the speaker, or a Piezo electric transducer can be provided on the add-in card.

2.0 PPEC SIGNALS

The signals described in this section are arranged in functional groups. The # symbol at the end of a signal name indicates that the signal's active or asserted state occurs when the signal is at a low voltage level. When # is not present after the signal name, the signal is asserted when it is at the high voltage level.

The terms *assertion* and *negation* are used extensively in this document to minimize confusion when a mixture of *active-low* and *active-high* signals are described. The terms *assert* and *assertion* indicate that a signal is active, independent of whether that level is represented by a high voltage or a low voltage. The terms *negate* and *negation* indicate that a signal is inactive.

The following notation is used to describe the PPEC signal types:

in:	A standard input-only signal.
in (ST)	A Schmitt Trigger input signal.
out	A totem pole output signal.
o/d	An open drain input/output signal.
t/s	A bi-directional tri-state signal.
t/s/o	A uni-directional, tri-state output signal.
s/t/s	A sustained tri-state signal. This is an active low tri-state signal that is owned and driven by one and only one agent at a time. The agent that drives a s/t/s signal low must drive it high for at least one clock before letting it float. A new agent can not start driving an s/t/s signal sooner than one clock after the previous owner tri-states it. An external pull-up must be provided by the central resource to sustain the inactive state until another agent drives the signal.

2.1 PCI Bus Interface Signals

Name	Type	Description
PCICLK	in	**PCI CLOCK:** Provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. PPEC design is optimized for 25 MHz and 33 MHz PCI bus frequency. **NOTE:** PCMCIA and IDE state machines use PCICLK as a clock reference. This allows simpler design with good granularity for optimized timing, but selection of a PCI clock frequency other than 25 or 33 MHz may impact PCMCIA and IDE interface performance.
PCIRST#	in	**PCI RESET:** Forces the entire PPEC component into a known state. All t/s and s/t/s signals are forced to a high impedance state, and the o/d signals are allowed to float high. All internal PPEC state machines are reset, and all registers are set to their default values. PCIRST# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, negation must be with a clean, bounce-free edge. PCIRST# must be asserted for a minimum 1 ms, and PCICLK must be active during the last 100 μs of the PCIRST# pulse.
AD[31:0]	t/s	**ADDRESS AND DATA:** Address and data are multiplexed on the same PCI pins. During the first clock of a transaction, AD[31:0] transfer a physical address (32 bits). During following clocks, AD[31:0] transfer data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports write bursts. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB), and AD[31:24] the most significant byte (MSB). The information contained in the two low order address bits varies by address space. In the I/O address space, AD[1:0] are used to provide full byte address. During memory space accesses, these two bits provide information on the type of burst ordering. During configuration space accesses, they identify the type of configuration access. When the PPEC is the target of a PCI cycle, AD[31:0] is input during the address phase of a transaction. During the following data phase(s), the PPEC asserts data on AD[31:0] if a PCI read, or accepts data if a PCI write.

2.1 PCI Bus Interface Signals (Continued)

Name	Type	Description
C/BE#[3:0]	in	**BUS COMMAND AND BYTE ENABLES:** These signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE#[3:0] define the bus command for bus command definitions. During the data phase, C/BE#[3:0] are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE#[0] applies to byte 0, and C/BE#[3] to byte 3. C/BE[3:0]# are not used for address decoding.
FRAME#	in	**CYCLE FRAME:** Driven by the current initiator to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. Data transfers continue while FRAME# is asserted. When FRAME# is negated, the transaction is in the final data phase.
TRDY#	s/t/s	**TARGET READY:** Asserted by the PPEC as a target to indicate completion of the current data phase. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock during which both TRDY# and IRDY# are sampled asserted. When the PPEC is the target during a read cycle, TRDY# indicates that the PPEC has valid data asserted on AD[31:0]. When it is a target during a write cycle, it indicates that the PPEC is prepared to latch data.
IRDY#	in	**INITIATOR READY:** IRDY# as an input indicates that the current cycle initiator is able to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock during which both IRDY# and TRDY# are sampled asserted. When the PPEC is the target of a write cycle, IRDY# indicates that valid data is present on AD[31:0]. During a read, it indicates that the initiator is prepared to latch data.
STOP#	s/t/s	**STOP:** Indicates that the PPEC, as a target of an PCI cycle, is requesting a master to stop the current transaction. Different semantics of the STOP# signal are defined in the context of other handshake signals (TRDY# and DEVSEL#).
PCILOCK#	in	**PCI LOCK:** Indicates an atomic operation that may require multiple transactions to complete. When PCILOCK# is sampled negated during the address phase of a transaction in which the PPEC is involved, the PPEC's interface becomes a locked resource until it samples PCILOCK# and FRAME# negated. When other masters attempt accesses to PPEC while it is locked, the PPEC responds with a RETRY termination.
IDSEL	in	**INITIALIZATION DEVICE SELECT:** Used as a chip select during configuration read and write transactions. It is sampled during the address phase of a transaction. If the PPEC samples IDSEL active during configuration read or write and address AD[1:0] = 00, it will respond by asserting DEVSEL# on the next cycle.
DEVSEL#	s/t/s	**DEVICE SELECT:** The PPEC asserts DEVSEL# to claim a PCI transaction as a result of positive decode, and when it samples IDSEL active and address AD[1:0] = 00 during configuration cycles to the PPEC configuration registers.
PAR	t/s	**PARITY:** Parity is even across AD[31:0] and C/BE#[3:0]. The PPEC drives PAR during read data phases when it is a target of a PCI cycle. This signal is an input in all other cases. During an address phase or write data phase in which the PPEC is a target, the PPEC samples this signal to compare it with internally generated parity. Note that PAR signal driving and tri-stating is always one clock delayed from the corresponding AD[31:0] signal driving and tri-stating.

2.1 PCI Bus Interface Signals (Continued)

Name	Type	Description
INTA#	o/d	**PCI INTERRUPT REQUEST A:** This is a level sensitive, active low signal that is used to signal interrupts from the PPEC's PCI-PCMCIA functional block. It is enabled in the PPIRR register. The connection of INTA# to the system interrupt controller is system specific. Note that this signal typically requires an external pull-up resistor.
INTB#	o/d	**PCI INTERRUPT REQUEST B:** This is a level sensitive, active low signal that is used to signal interrupts from the PPEC's PCI-IDE Interface functional block. It is enabled in the PPIRR register. The connection of INTB# to the system interrupt controller is system specific. Note that this signal typically requires an external pull-up resistor.
PERR#	s/t/s	**PARITY ERROR:** This is a sustained tri-state signal that is used to report data parity errors during all transactions for which the PPEC positively decodes address. It is typically used by the system logic to generate an NMI. SERR# is pure open drain, and is actively driven for a single PCI clock. The assertion of SERR# is synchronous with the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the negated state is accomplished by a weak pull-up resistor (same value as for s/t/s) which is provided by the system design, and not by the signaling agent or central resource. This pull-up resistor may take two to three clock periods to fully restore SERR#.
SERR#	o/d	**SYSTEM ERROR:** An open-drain signal that is used to report address parity errors during all transactions in which PPEC is involved. It is typically used by the system logic to generate an NMI. SERR# is pure open drain and is actively driven for a single PCI clock. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the negated state is accomplished by a weak pull-up resistor (same value as used for s/t/s) that is provided by the system, and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#.

2.2 System Interrupt Signals

Name	Type	Description
IRQ3	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ3:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ4	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ4:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.

2.2 System Interrupt Signals (Continued)

Name	Type	Description
IRQ5	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ5:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ7	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ7:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ9	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ9:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ10	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ10:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ11	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ11:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ12	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ12:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ14	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ14:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt environments. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.
IRQ15	t/s/o or o/d	**SYSTEM INTERRUPT REQUEST IRQ15:** Depending on the PPEC's configuration, this signal can be selected as an active high t/s/o or active low o/d driven signal according to the specific signaling requirement for shared/non-shared ISA/EISA/ Microchannel or other system bus interrupt requirements. Note that this signal may require an external pull-up resistor depending on the system configuration and usage.

2.3 Audio Interface And Configuration Mode Selection Signal

Name	Type	Description
SPKROUT# /MODE	t/s or o/d	**SPEAKER OUTPUT OR PCMCIA INTERFACE CONFIGURATION MODE:** SPKROUT#/MODE is configured as an input during reset. The user selects 2-Socket Mode with a weak pull-down resistor (10K) on the signal pin, and selects 4-Socket with a weak pull-up resistor. The PPEC automatically reconfigures the pin as an output for use as SPKROUT# after reading and storing the state of the SPKROUT#/MODE pin at the end of the reset sequence. This signal MUST be connected to an external pull-up or pull-down resistor according to the desired operating mode.

2.4 External Power Control Signal

Name	Type	Description
PWRWR#	out	**POWER CONTROL WRITE:** This signal is a write strobe for the PCMCIA Socket Power Control Logic. It is used to latch V_{CC} and V_{PP} power-control information that is transferred via the PCMCIA Socket A data lines. This signal is active during I/O write access to the PPEC's internal PCMCIA Power Control Registers, and during automatic Power-Control write sequences when reset is active or when the PCMCIA auto-power function is activated.

2.5 PCMCIA Interface Signals

The PPEC supports two PCMCIA socket configuration modes: Mode 0 and Mode 1. The number of sockets supported differs with each mode. The PPEC signals therefore change according to the operating mode.

All t/s and t/s/o PCMCIA signals are implemented using 5V/3.3V configurable buffers.

2.5.1 MODE 0 (TWO-SOCKET) CONFIGURATION MODE SIGNALS

Mode 0 configures the PPEC for two PCMCIA sockets: Socket A and Socket B. PCMCIA function signals are identical for both sockets. However, Socket A signals may be multiplexed with IDE interface signals (see Section 2.6) while Socket B signals are not multiplexed, and the Socket A AREG#/IDECFG signal has two functions while the Socket B REG# signal has one function. Figure 4 shows the PPEC signal pinout for Mode 0.

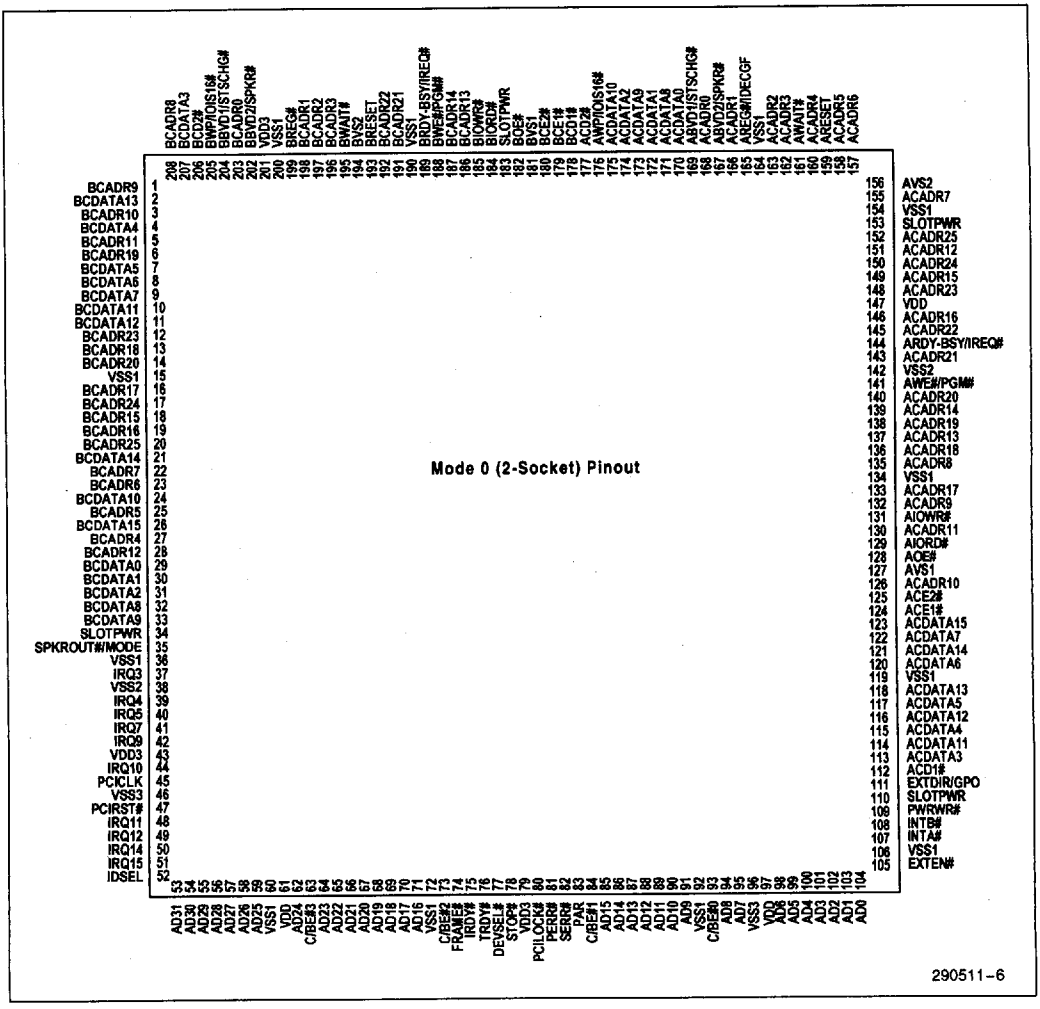

Figure 4. Mode 0 Pinout

2.6 Socket A and B PCMCIA Signals

Name	Type	Description
ACDATA[15:0] BCDATA[15:0]	t/s	**SOCKET A AND SOCKET B DATA BUS SIGNALS [15:0]:** This is a 16-bit data bus that is used for data transfer between the PPEC and the PCMCIA card.
ACADR[25:0] BCADR[25:0]	t/s	**SOCKET A AND SOCKET B ADDRESS BUS SIGNALS [25:0]:** This is a 26-bit address bus that is used for addressing memory locations and attribute memory within a 64 MByte PCMCIA address range, and for addressing I/O within a 64 KByte PCMCIA address range.
AIORD# BIORD#	t/s/o	**SOCKET A AND SOCKET B I/O READ:** The PPEC uses this active low signal and the REG# signal to gate I/O Read data from the PC Card. When low, IORD# gates I/O Read data from a memory PC Card only when the REG# signal is also asserted.
AIOWR# BIOWR#	t/s/o	**SOCKET A AND SOCKET B I/O WRITE:** The PPEC uses this active low signal and the REG# signal to gate I/O Write data to the PC Card. When low, IOWR# gates the I/O Write data to the PC Card only when the REG# signal is also asserted.
AREG#/ IDECFG	t/s/o in	**SOCKET A ATTRIBUTE MEMORY SELECT AND IDE CONFIGURATION:** This signal has two functions. During reset it is configured as an input with the IDE Configuration function. The signal level is sampled at the end of the reset sequence. If it is sampled low, all of the Socket A pins are used for PCMCIA Socket-A interface signals; if it is sampled high, some of Socket A pins are used for IDE interface signals. The status of IDECFG pin when sampled is stored in the PPEC IDE Configuration Register so that it can be used to support BIOS software with enhanced auto-configuration capabilities. If it is sampled low at the end of the reset sequence, the signal is configured after reset as an output with the Attribute Memory Select function. The signal is inactive (high) during all normal accesses to main memory of PC Cards. I/O PC Cards do not respond to IORD# or IOWR# assertion when the AREG# signal is inactive. When it is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space. This signal pin MUST be either externally pulled-up (IDE interface) with a weak pull-up resistor (10K Ohm) or pulled down (no IDE interface), depending on the system configuration.
BREG#	t/s/o	**SOCKET B ATTRIBUTE MEMORY SELECT:** This signal is inactive (high) during all normal accesses to what is known as Main Memory of the PC Card. I/O PC Cards do not respond to IORD# or IOWR# when the BREG# signal is inactive. When this signal is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space.
AOE# BOE#	t/s/o	**SOCKET A AND SOCKET B OUTPUT ENABLE:** This is an active low signal that gates Memory Read data from memory PC Cards.

2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
ACE[2:1]# BCE[2:1]#	t/s/o	**SOCKET A AND SOCKET B CHIP ENABLE [2:1]:** These are active low signals that are driven by the PPEC when the socket is enabled. CE1# enables even bytes; CE2# enables odd bytes.
AWE#/PGM# BWE#/PGM#	t/s/o	**SOCKET A AND SOCKET B WRITE ENABLE/PROGRAM:** This signal has a single function with two semantics. In WE# semantics it is used by the host to gate Memory Write data. In PGM# semantics it is used for memory PC Cards that employ programmable memory technologies.
ARDY-BSY#/ IREQ# BRDY-BSY#/ IREQ#	in (ST)	**SOCKET A AND SOCKET B READY/BUSY OR INTERRUPT REQUEST:** This signal has two functions. When a memory card is in use, it has the *Ready/Busy* function. The signal is driven low by the memory PC Card to indicate that the card circuits are busy processing a previous write command. READY/BUSY# is set high when the memory PC Card is ready to accept a new data transfer command. When an I/O card is in use, it has the *IREQ#* interrupt request function. The card asserts IREQ# to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. The status of this signal is stored in the Interface Status Register.
AWP/IOIS16# BWP/IOIS16#	in	**SOCKET A AND SOCKET B WRITE PROTECT OR CARD IS 16-BIT PORT:** This signal has two functions. For memory PC Cards, it has the *Write Protect* function that reflects the status of the Write Protect switch on the cards. If a memory PC Card switch is present, this signal is asserted by the card when the switch is enabled (write protection desired), and negated when the switch is disabled. If the memory PC Card has no Write Protect switch, the card connects this line to ground or V_{CC}, depending on the condition of the card memory. If the memory PC Card can always be written, the signal pin is connected to ground. If the memory PC Card is permanently Write Protected, the pin is connected to V_{CC}. The status of WP is stored in the Interface Status Register. However, Memory Write Cycle is not blocked by the xWP signal unless the Write Protect bit is set to 1 in the card memory offset Address High Byte Register. For I/O PC Cards, it has the *"Card is 16-Bit Port"* (IOIS16#) function. The signal is asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port that is addressed is capable of 16-bit accesses. This signal is used by the PPEC's data assembly/disassembly logic to determine the number of PCMCIA cycles required to complete data transfer (which from the PCI perspective can be 32-bits wide). If this signal is not asserted during a 16-bit I/O access, the PPEC generates two 8-bit data cycles to the even and odd bytes of the 16-bit word which is requested by the initial cycle. The status of this signal is stored in the Interface Status Register.
ARESET BRESET	t/s/o	**SOCKET A AND SOCKET B RESET:** This signal forces a hard reset to the PC card when asserted.

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2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
AWAIT# BWAIT#	in	**SOCKET A AND SOCKET B BUS CYCLE WAIT:** This signal is driven by the PC card to delay completion of a memory or I/O cycle that is in progress.
ABVD1/ STSCHG# BBVD1/ STSCHG#-	in	**SOCKET A AND SOCKET B BATTERY VOLTAGE DETECT 1/STATUS CHANGE-RING INDICATE:** This signal has three functions. As Battery Voltage Detect 1, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high) the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As CHANGED STATUS (STSCHG#), it is held high the when the *Signal on Change* bit or the *Changed* bit in the Card Status Register on the PC Card is set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. The signal status is stored in the Interface Status Register.
ABVD2/ SPKR# BBVD2/ SPKR#	in	**SOCKET A AND SOCKET B BATTERY VOLTAGE DETECT OR DIGITAL AUDIO:** This signal has two functions. As Battery Voltage Detect, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As Digital Audio, it is the input for a single amplitude (digital) audio waveform that is intended to drive the system's speaker via the SPKROUT# output pin on the system (host) interface. The status of the Battery Voltage Detect signal is stored in the Interface Status Register.

2.6 Socket A and B PCMCIA Signals (Continued)

Name	Type	Description
AVS1 BVS1	in	**SOCKET A AND SOCKET B CARD VOLTAGE CAPABILITY SENSE # 1:** The PPEC samples this signal and the corresponding xVS2 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register
AVS2 BVS2	in	**SOCKET A AND SOCKET B CARD VOLTAGE CAPABILITY SENSE # 1:** The PPEC samples this signal before configuring V_{CC} power to the socket to determine the PC card input voltage capability. If it is sampled high, 5V or 3.3V can be applied to the PC Card depending on the state of VS1. If it is sampled low, the PC Card required voltage is less than 3.3V, which the PPEC does not support. The status of this signal is available in the Socket Power Configuration Register.
ACD[2:1]# BCD[2:1]#	in (ST)	**SOCKET A AND SOCKET B CARD DETECT [2:1]:** These are two Card Detect signals that allow verification of proper card insertion. The signals are positioned at opposite ends of the connector to facilitate the detection process, and are connected to ground in the PC Card. The signals are therefore forced low whenever a card is placed in the socket. The status of the signals are available in the Interface Status Register. These signals have internal pull-up resistors.
EXTEN#	out	**EXTEN#:** This is used only in Mode 0, and only when the IDE Interface is not enabled. When the IDE is enabled in Mode 0, the EXTEN# signal pin is reserved. When low, EXTEN# enables external transceivers that de-couple the PCMCIA power latch from the Socket A CDATA[7:0] data bus signals to allow "hot" insertion and removal.
EXTDIR or GPO	out	**EXTERNAL TRANSCEIVER DIRECTION CONTROL OR GENERAL PURPOSE OUTPUT:** This signal has two functions, depending on whether the IDE Interface is enabled, as determined by the state of IDECFG at the end of the reset sequence. If the IDE Interface is disabled, the EXTDIR signal provides direction control for external transceivers. It is high during read cycles, and low during write cycles. If the IDE Interface is enabled, the GPO provides a general-purpose output. The GPO signal is directly controlled by bit 1 of the Global Security Control Register, and can be used to provide global PC Card LOCK function by controlling an external socket locking mechanism.

NOTE:
The PCMCIA Input Acknowledge (INPACK) signal is not supported by the PPEC.

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2.6.1 MODE 1 (FOUR-SOCKET) CONFIGURATION SIGNALS

In Configuration Mode 0, two PC Card sockets are available. In Configuration Mode 1, four PC Card sockets are available, requiring more signals than Mode 0. Figure 5 shows the PPEC signal pinout for Mode 1.

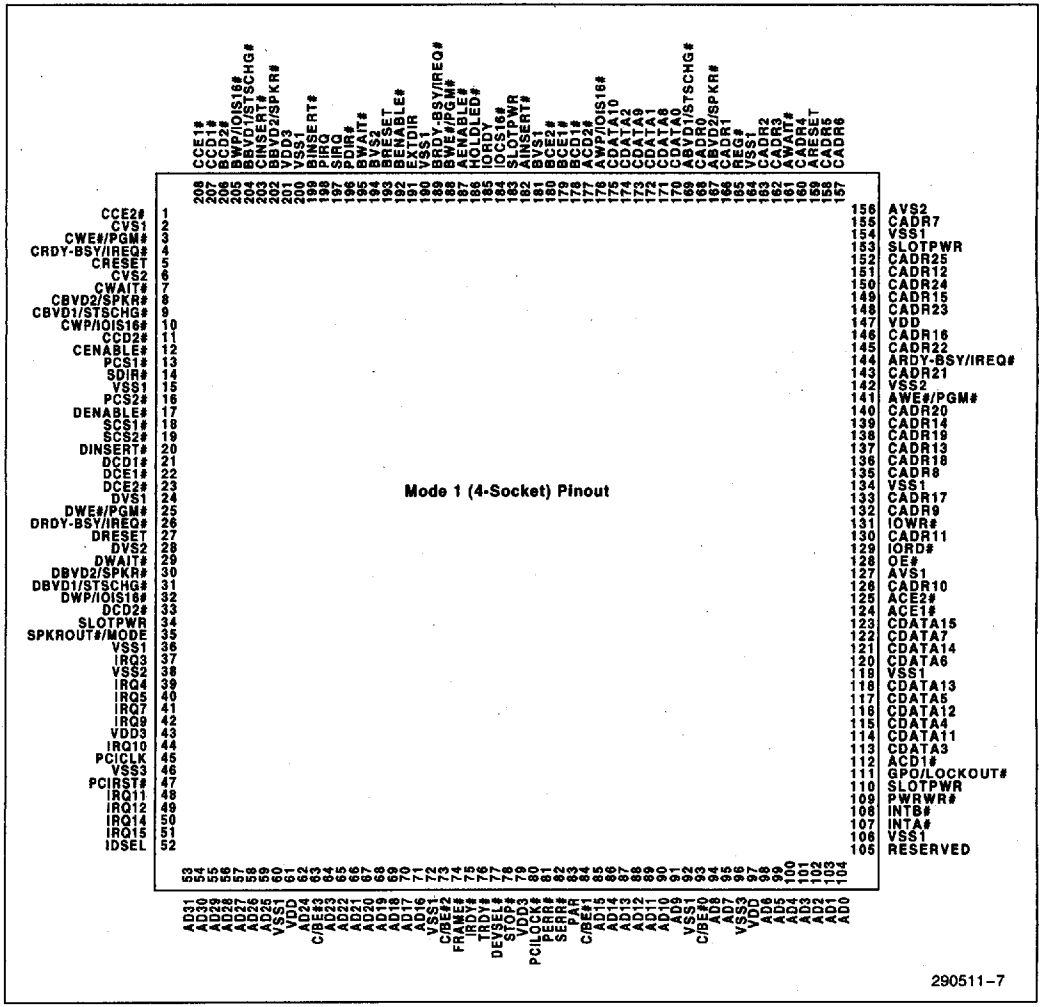

Figure 5. Mode 1 Pinout

Several signals and buses that are dedicated to Socket A in Mode 0 are common to all four sockets in Mode 1, as shown in Table 4.

Table 4. Mode 1 Common Signals

Mode 0 Socket A Signals	Mode 1 Common Socket Signals
ACDATA[15:0]	CDATA [15:0]
ACADR[25:0]	CADR[25:0]
AREG#	REG#
AOE#	OE#
AIORD#	IORD#
AIOWR#	IOWR#

This use of common signals significantly reduces the number of signals (and package pins) that would be required if each socket had it's own dedicated set of signals. It also releases the corresponding Socket B signal pins (BCDATA[15:0], BCADR[25:0], etc.) for use by the following socket-specific signals:

xCE1#	xVS1	xENABLE	xRDY-BUSY#/IREQ#
xCE2#	xVS2	xBVD1	xINSERT
xCD1#	xWP/IOIS16#	xBVD2	xWAIT#
xCD2#	xWE#/PGM#	xRESET	xINSERT#

XINSERT# and HOLDLED# (not listed) are Mode 1 signals that are not used in Mode 0.

All of the signals used in Mode 1 are described in the following table. The sockets have separate, but functionally identical sets of signals. Table 5 lists the PPEC pinout for the various configuration modes.

2.7 Socket A, B, C, and D PCMCIA Signals

Pin Name	Type	Description
CDATA[15:0]	t/s	**COMMON DATA BUS SIGNALS [15:0]:** This is a 16-bit data bus that is used for data transfer between the PPEC and the PCMCIA cards, and the PPEC and IDE drives when the IDE Interface is used. This bus is common to all of the sockets.
CADR[25:0]	t/s	**COMMON ADDRESS BUS SIGNALS [25:0]:** This is a 26-bit address bus that is used for addressing memory locations and attribute memory within a 64 MByte PCMCIA address range, and for addressing I/O within a 64 KByte PCMCIA address range. This bus is common to all of the sockets. If the IDE interface is used, CADR[2:0] transfer IDE register addresses during IDE accesses.
IORD#	t/s/o	**COMMON I/O READ:** The PPEC uses this active low signal and the REG# signal to gate I/O Read data from the PC Card. When low, IORD# gates I/O Read data from a memory PC Card only when the REG# signal is also asserted. This signal is common to all of the sockets.
IOWR#	t/s/o	**COMMON I/O WRITE:** The PPEC uses this active low signal and the REG# signal to gate I/O Write data to the PC Card. When low, IOWR# gates the I/O Write data to the PC Card only when the REG# signal is also asserted. This signal is common to all of the sockets.

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2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
REG	t/s/o	**COMMON ATTRIBUTE MEMORY SELECT:** This signal is inactive (high) during all normal accesses to main memory of PC Cards. I/O PC Cards do not respond to IORD# or IOWR# assertion when the AREG# signal is inactive. When it is active (low), access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. Configurable memory PC Cards and I/O PC Cards contain configuration and status registers in the Attribute Memory Space. This signal is common to all of the sockets, and requires an external pull-up resistor to prevent the signal from floating during reset.
OE#	t/s/o	**COMMON OUTPUT ENABLE:** This is an active low signal that gates Memory Read data from memory PC Cards. It is common to all of the sockets.
EXTDIR	out	**EXTERNAL TRANSCEIVER DIRECTION CONTROL:** This signal is high during reads, and low during writes, and is used for both high bytes and low bytes. It defaults to write (low) at power-up. EXTDIR is used to control the drive direction of only the PCMCIA transceivers. Separate transceiver controls are provided for the IDE Interface.
ACE#[2:1] BCE#[2:1] CCE#[2:1] DCE#[2:1]	t/s/o	**SOCKET A-D CHIP ENABLE [2:1]:** These are active low signals that are driven by the PPEC when the socket is enabled. CE1# enables even bytes; CE2# enables odd bytes.
AWE#/PGM# BWE#/PGM# CWE#/PGM# DWE#/PGM#	t/s/o	**SOCKET A-D WRITE ENABLE/PROGRAM:** This signal has single function, but with two semantics. In WE# semantics, this signal is used by the host to gate Memory Write data. In PGM# semantics this signal is used for memory PC Cards that employ programmable memory technologies.
ARDY-BSY#/ IREQ BRDY-BSY#/ IREQ# CRDY-BSY#/ IREQ# DRDY-BSY#/ IREQ#	in(ST)	**SOCKET A-D READY/BUSY OR INTERRUPT REQUEST:** This signal has two functions, depending on the card in the socket. When a memory card is in use, it has the *Ready/Busy* function. The signal is driven low by the memory PC Card to indicate that the card circuits are busy processing a previous write command. READY/BUSY# is set high when memory PC Cards are ready to accept a new data transfer command. When an I/O card is in use, it has the */REQ#* interrupt request function. The card asserts IREQ# to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. The status of this signal is available in the Interface Status Register.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
AWP/IOIS16# BWP/IOIS16# CWP/IOIS16# DWP/IOIS16#	in	**SOCKET A-D WRITE PROTECT OR CARD IS 16-BIT PORT:** This signal has two functions, depending on the type of card in the socket. For memory PC Cards, it has the *Write Protect* function that reflects the status of the Write Protect switch on the cards. If a memory PC Card switch is present, this signal is asserted by the card when the switch is enabled (write protection desired), and negated when the switch is disabled. If the memory PC Card has no Write Protect switch, the card connects this line to ground or to V_{CC}, depending on the condition of the card memory. If the memory PC Card can always be written, the signal pin is connected to ground. If the memory PC Card is permanently Write Protected, the pin is connected to V_{CC}. The status of WP is available in the Interface Status Register. However, Memory Write Cycle is not blocked by the WP signal unless the Write Protect bit is set to 1 in the card memory offset Address High Byte Register. For I/O PC Cards, it has the *"Card is 16-Bit Port"* (IOIS16#) function. The signal is asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port that is addressed is capable of 16-bit accesses. This signal is used by the PPEC's data assembly/disassembly logic to determine the number of PCMCIA cycles required to complete data transfers (which from the PCI perspective can be 32-bits wide). If this signal is not asserted during a 16-bit I/O access, the PPEC generates two 8-bit data cycles to the even and odd bytes of the 16-bit word which is requested by the initial cycle. The status of this signal is available in the Interface Status Register.
ARESET BRESET CRESET DRESET	t/s/o	**SOCKET A-D RESET:** This signal forces a hard reset to the PC card when asserted.
AWAIT# BWAIT# CWAIT# DWAIT#	in	**SOCKET A-D BUS CYCLE WAIT:** This signal is driven by the PC card to delay completion of a memory or I/O cycle that is in progress.

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2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Name	Type	Description
ABVD1/ STSCHG# BBVD1/ STSCHG# CBVD1/ STSCHG# DBVD1/ STSCHG#	in	**SOCKET A-D BATTERY VOLTAGE DETECT 1/STATUS CHANGE:** This signal has three functions. As Battery Voltage Detect 1, it is driven by memory a PC Card that has a battery to indicate the condition of the battery, and is used with BVD2 as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As CHANGED STATUS (STSCHG#), it is held high the when the *Signal on Change* bit or the *Changed* bit in the Card Status Register on the PC Card is set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. The signal status is stored in the Interface Status Register.
ABVD2/ SPKR# BBVD2/ SPKR# CBVD2/ SPKR# DBVD2/ SPKR#	in	**SOCKET A-D BATTERY VOLTAGE DETECT OR DIGITAL AUDIO:** This signal has two functions. As Battery Voltage Detect, it is driven by a memory PC Card that has a battery to indicate the condition of the battery as follows: • When both BVD1 and BVD2 are asserted (high), the battery is in good condition. • When BVD2 is negated while BVD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the memory PC Card is still assured. When BVD1 is negated (low) with BVD2 either asserted or negated, the battery is no longer serviceable and data is lost. As Digital Audio, it is the input for a single amplitude (digital) audio waveform that is intended to drive the system's speaker via the SPKROUT# output pin on the system (host) interface. The status of the Battery Voltage Detect signal is stored in the Interface Status Register.
AVS1 BVS1 CVS1 DVS1	in	**SOCKET A-D CARD VOLTAGE CAPABILITY SENSE #1:** In Mode 1 partially buffered and non-buffered implementations, the PPEC samples this signal and the corresponding xVS2 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register.

2.7 Socket A, B, C, and D PCMCIA Signals (Continued)

Pin Name	Type	Description
AVS2 BVS2 CVS2 DVS2	in	**SOCKET A-D CARD VOLTAGE CAPABILITY SENSE #2:** In Mode 1 partially buffered and non-buffered implementations, the PPEC samples this signal and the corresponding xVS1 signal before applying V_{CC} power to the socket to determine the PC card input voltage capability. The signal must be connected to an external pull-up resistor. The status of this signal is stored in the Socket Power Configuration Register.
ACD[2:1]# BCD[2:1]# CCD[2:1]# DCD[2:1]#	in (ST)	**SOCKET A-D CARD DETECT [2:1]:** These are two Card Detect signals that allow verification of proper card insertion. The signals are positioned at opposite ends of the connector to facilitate the detection process, and are connected to ground in the PC Card. The signals are therefore forced low whenever a card is placed in the host socket. The status of the signals are stored in the Interface Status Register. ADC[2:1]# and BCD[2:1]# have internal pull-up resistors; CCD[2:1]# and DCD[2:1]# require external pull-up resistors.
AENABLE# BENABLE# CENABLE# DENABLE#	out	**SOCKET A-D BUFFER ENABLE:** This signal enables the PC Card socket buffers/ transceivers, and is controlled by the corresponding socket Power Control Register.
AINSERT# BINSERT# CINSERT# DINSERT#	in	**SOCKET A-D CARD INSERTION DETECT:** These signals are used in non-buffered or partially-buffered Mode 1 implementations to provide the PPEC with an early indication that a PC Card is being inserted into a PCMCIA socket. xINSERT# requires an external pull-up resistor, and is connected directly to one of the socket pins which is used normally (in fully buffered configuration) for V_{SS} connection. See the "PPEC Design Guide" for a detailed discussion of the use of these pins.
GPO/ LOCKOUT#	out	**GENERAL PURPOSE OUTPUT/LOCKOUT:** When bit 2 of the Global Security Control Register (GSCTRL) is set to 1, the GPO signal is enabled. When bit 2 of the GSTCTRL register is set to 0, the LOCKOUT# signal is enabled. The default value of bit 2 of the GSCTRL register is 0, enabling the LOCKOUT# signal. The GPO signal is directly controlled by bit 1 of the Global Security Control Register, and can be used to provide global PC Card LOCK function by controlling an external socket locking mechanism. LOCKOUT# is intended for systems that require a locking mechanism for the PCMCIA sockets. When the Lockout feature is selected and LOCKOUT# is active, the CD2# for each socket is treated as an Eject Request pin, and CD1# is internally routed to the circuitry that uses CD2#. This feature does not affect the routing of the CDx# signals to the interrupt generator or to the status registers, so a rising edge on either card detect still generates a Card Status Change interrupt. All other internal circuitry that uses CD1# and CD2#, such as the circuitry that tri-states the PCMCIA bus during a card removal, uses CD1# exclusively while the socket is locked.
HOLDLED#	out	**HOLD LED:** This signal is used to indicate a HOLD condition on the PCMCIA Bus during PC Card insertions and removals in non-buffered or partially-buffered Mode 1 implementations.

2.8 IDE Interface Signal

The PPEC supports two Fast Local Bus IDE interfaces (2 connectors with a total of 4 IDE drives) in both PCMCIA interface configuration modes. For clarity, the IDE interface pins are named and defined in this section independently of the basic signals with which they are multiplexed.

Most of the IDE interface signals are multiplexed with Socket A signals in Mode 0. Table 5 lists the signal pinout for Mode 0 with and without IDE selection.

In Mode 1, the IDE interface is independent of the PCMCIA interface with the exception of the data, address, write, and read strobes which are used for both interfaces as follows:

IDE Signal	PCMCIA Signal
DD[15:0]	CDATA[15:0]
DA[2:0]	CADR[2:0]
DIOW#	IOWR#
DIOR#	IORD#

Figure 2 shows the Mode 1 IDE signals.

2.9 IDE Interface Signals

Name	Type	Description
DD[15:0]	t/s	**DRIVE DATA BUS [15:0]:** This is an 8-bit or 16-bit bi-directional data bus that is located between the IDE interface controller, and the drive. The lower 8 bits are used for 8-bit transfers (registers, ECC bytes and, if the drive supports the Features Register, for 8-bit-only data transfers that may be selected). Data signals DD[7:0] can be used to support the IDE Hardware Configuration feature.
DA[2:0]	out	**DRIVE ADDRESS [2:0]:** This is a 3-bit binary coded address asserted by the host to access a drive register or the drive data port.
DIOR#	out	**DRIVE I/O READ STROBE:** The falling edge of DIOR# enables data from a register or from the drive's data port onto the IDE interface data bus. The rising edge of DIOR# latches data into the PPEC.
DIOW#	out	**DRIVE I/O WRITE STROBE:** The rising edge of DIOW# clocks data from the IDE interface data bus into a register or into the drive's data port.
IOCS16#	in	**I/O CHIP-SELECT 16-BIT:** The assertion of IOCS16# indicates to the PPEC that 16-bit data port has been addressed, and that the drive is prepared to send or receive a 16-bit data word.
IORDY	in	**I/O CHANNEL READY:** This signal is driven low by the currently accessed drive to extend the IDE transfer cycle when the drive is not ready to respond to a data transfer request. When IORDY is not negated, it is in a high impedance state from the perspective of the IDE drive(s). An external pull-up resistor must be provided on the cable side of the IDE Interface.
PCS1#	out	**PRIMARY IDE CHIP SELECT FOR DATA/COMMAND I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Command Block Registers of the drive(s) on the Primary IDE Interface.

2.9 IDE Interface Signals (Continued)

Name	Type	Description
PCS2#	out	**PRIMARY IDE CHIP SELECT FOR CONTROL/STATUS I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Control Block Registers of the drive(s) on the Primary IDE Interface.
SCS1#	out	**SECONDARY IDE CHIP SELECT FOR DATA/COMMAND I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Command Block Registers of the drive(s) on the Secondary IDE Interface.
SCS2#	out	**SECONDARY IDE CHIP SELECT FOR CONTROL/STATUS I/O ADDRESS RANGE:** This signal can be asserted only when IDEEN# is asserted (low) during IDE cycles to the appropriate address range as defined by the IDE Address Configuration Registers. It selects Control Block Registers of the drive(s) on the Secondary IDE Interface.
PIRQ	in	**PRIMARY IDE INTERFACE INTERRUPT REQUEST:** This signal is used by the IDE drives on the Primary connector to interrupt the host processor. It can be routed to any system interrupt, and can therefore be internally OR-ed (within the PPEC) with Secondary IDE interrupt.
SIRQ	in	**SECONDARY IDE INTERFACE INTERRUPT REQUEST:** This signal is used by the IDE drives on the Secondary connector to interrupt the host processor. It can be routed to any system interrupt, and can therefore be internally OR-ed (within the PPEC) with Primary IDE interrupt.
PDIR#	out	**PRIMARY IDE TRANSCEIVER DIRECTION CONTROL:** This signal controls the drive direction of the Primary IDE transceivers. The signal is asserted low only during read access to the Primary IDE registers. It is driven high all other times (during writes to Primary IDE registers, and when the Primary IDE is not accessed.
SDIR#	out	**SECONDARY IDE TRANSCEIVER DIRECTION CONTROL:** This signal controls the drive direction of the Secondary IDE transceivers. The signal is asserted low only during read access to the Secondary IDE registers. It is driven high all other times (during writes to Secondary IDE registers, and when the Secondary IDE is not accessed).

2.10 Pin Cross-Reference List

Table 5 lists the PPEC signals in package pin order according to mode. Note that the signal pinout changes in Mode 0 depending on whether the IDE interface is enabled. In Mode 1, the IDE interface is separate from the socket interfaces with the exception of the IDE DD[15:0] data bus, DA[2:0] address bus, DIOR# read strobe, and DIOW# write strobe which are multiplexed with the CDATA[15:0], CADR[2:0], IORD#, and IOWR# common socket signals.

Table 5. Pin Cross-Reference

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
1	CCE2#	BCADR9	BCADR9
2	CVS1	BCDATA13	BCDATA13
3	CWE#/PGM#	BCADR10	BCADR10
4	CRDY-BSY#/IREQ#	BCDATA4	BCDATA4
5	CRESET	BCADR11	BCADR11
6	CVS2	BCADR19	BCADR19
7	CWAIT#	BCDATA5	BCDATA5
8	CBVD2/SPKR#	BCDATA6	BCDATA6
9	CBVD1/STSCHG#	BCDATA7	BCDATA7
10	CWP/IOIS16#	BCDATA11	BCDATA11
11	CCD2#	BCDATA12	BCDATA12
12	CENABLE#	BCADR23	BCADR23
13	PCS1#	BCADR18	BCADR18
14	SDIR#	BCADR20	BCADR20
15	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
16	PCS2#	BCADR17	BCADR17
17	DENABLE#	BCADR24	BCADR24
18	SCS1#	BCADR15	BCADR15
19	SCS2#	BCADR16	BCADR16
20	DINSERT#	BCADR25	BCADR25
21	DCD1#	BCDATA14	BCDATA14
22	DCE1#	BCADR7	BCADR7
23	DCE2#	BCADR6	BCADR6
24	DVS1	BCDATA10	BCDATA10
25	DWE#/PGM#	BCADR5	BCADR5
26	DRDY-BSY#/IREQ#	BCDATA15	BCDATA15
27	DRESET	BCADR4	BCADR4
28	DVS2	BCADR12	BCADR12

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
29	DWAIT#	BCDATA0	BCDATA0
30	DBVD2/SPKR#	BCDATA1	BCDATA1
31	DBVD1/STSCHG#	BCDATA2	BCDATA2
32	DWP/IOIS16#	BCDATA8	BCDATA8
33	DCD2#	BCDATA9	BCDATA9
34	SLOTPWR (5V)	SLOTPWR (5V)	SLOTPWR (5V)
35	SPKROUT#/MODE	SPKROUT#/MODE	SPKROUT#/MODE
36	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
37	IRQ3	IRQ3	IRQ3
38	V_{SS} (CORE)	V_{SS} (CORE)	V_{SS} (CORE)
39	IRQ4	IRQ4	IRQ4
40	IRQ5	IRQ5	IRQ5
41	IRQ7	IRQ7	IRQ7
42	IRQ9	IRQ9	IRQ9
43	VDD (5V)	VDD (5V)	VDD (5V)
44	IRQ10	IRQ10	IRQ10
45	PCICLK	PCICLK	PCICLK
46	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
47	PCIRST#	PCIRST#	PCIRST#
48	IRQ11	IRQ11	IRQ11
49	IRQ12	IRQ12	IRQ12
50	IRQ14	IRQ14	IRQ14
51	IRQ15	IRQ15	IRQ15
52	IDSEL	IDSEL	IDSEL
53	AD31	AD31	AD31
54	AD30	AD30	AD30
55	AD29	AD29	AD29
56	AD28	AD28	AD28
57	AD27	AD27	AD27
58	AD26	AD26	AD26
59	AD25	AD25	AD25
60	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)

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Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
61	VDD (5V)	VDD (5V)	VDD (5V)
62	AD24	AD24	AD24
63	C/BE3	C/BE3	C/BE3
64	AD23	AD23	AD23
65	AD22	AD22	AD22
66	AD21	AD21	AD21
67	AD20	AD20	AD20
68	AD19	AD19	AD19
69	AD18	AD18	AD18
70	AD17	AD17	AD17
71	AD16	AD16	AD16
72	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
73	C/BE2	C/BE2	C/BE2
74	FRAME#	FRAME#	FRAME#
75	IRDY#	IRDY#	IRDY#
76	TRDY#	TRDY#	TRDY#
77	DEVSEL#	DEVSEL#	DEVSEL#
78	STOP#	STOP#	STOP#
79	VDD (5V)	VDD (5V)	VDD (5V)
80	PCILOCK#	PCILOCK#	PCILOCK#
81	PERR#	PERR#	PERR#
82	SERR#	SERR#	SERR#
83	PAR	PAR	PAR
84	C/BE1	C/BE1	C/BE1
85	AD15	AD15	AD15
86	AD14	AD14	AD14
87	AD13	AD13	AD13
88	AD12	AD12	AD12
89	AD11	AD11	AD11
90	AD10	AD10	AD10
91	AD9	AD9	AD9
92	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
93	C/BE0	C/BE0	C/BE0

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
94	AD8	AD8	AD8
95	AD7	AD7	AD7
96	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
97	VDD (5V)	VDD (5V)	VDD (5V)
98	AD6	AD6	AD6
99	AD5	AD5	AD5
100	AD4	AD4	AD4
101	AD3	AD3	AD3
102	AD2	AD2	AD2
103	AD1	AD1	AD1
104	AD0	AD0	AD0
105	RESERVED	EXTEN#	RESERVED
106	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
107	INTA#	INTA#	INTA#
108	INTB#	INTB#	INTB#
109	PWRWR#	PWRWR#	PWRWR#
110	SLOTPWR (5V)	SLOTPWR (5V)	SLOTPWR (5V)
111	GPO/LOCKOUT#	EXTDIR	GPO
112	ACD1#	ACD1#	RESERVED
113	CDATA3	ACDATA3	DD3
114	CDATA11	ACDATA11	DD11
115	CDATA4	ACDATA4	DD4
116	CDATA12	ACDATA12	DD12
117	CDATA5	ACDATA5	DD5
118	CDATA13	ACDATA13	DD13
119	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
120	CDATA6	ACDATA6	DD6
121	CDATA14	ACDATA14	DD14
122	CDATA7	ACDATA7	DD7
123	CDATA15	ACDATA15	DD15
124	ACE1#	ACE1#	RESERVED
125	ACE2#	ACE2#	RESERVED
126	CADR10	ACADR10	PCS2#
127	AVS1	AVS1	RESERVED

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
128	OE#	AOE#	PDIR#
129	IORD#	AIORD#	DIOR#
130	CADR11	ACADR11	PCS1#
131	IOWR#	AIOWR#	DIOW#
132	CADR9	ACADR9	RESERVED
133	CADR17	ACADR17	RESERVED
134	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
135	CADR8	ACADR8	RESERVED
136	CADR18	ACADR18	RESERVED
137	CADR13	ACADR13	SCS1#
138	CADR19	ACADR19	RESERVED
139	CADR14	ACADR14	RESERVED
140	CADR20	ACADR20	RESERVED
141	AWE#/PGM#	AWE#/PGM#	RESERVED
142	V_{SS} (CORE)	V_{SS} (CORE)	V_{SS} (CORE)
143	CADR21	ACADR21	RESERVED
144	ARDY-BSY#/IREQ#	ARDY-BSY#/IREQ#	IORDY
145	CADR22	ACADR22	RESERVED
146	CADR16	ACADR16	RESERVED
147	VDD (5V)	VDD (5V)	VDD (5V)
148	CADR23	ACADR23	RESERVED
149	CADR15	ACADR15	SDIR#
150	CADR24	ACADR24	PIRQ
151	CADR12	ACADR12	SCS2#
152	CADR25	ACADR25	SIRQ
153	SLOTPWR (5V)	SLOTPWR (5V)	SLOTPWR (5V)
154	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
155	CADR7	ACADR7	RESERVED
156	AVS2	AVS2	RESERVED
157	CADR6	ACADR6	RESERVED
158	CADR5	ACADR5	RESERVED
159	ARESET	ARESET	RESERVED
160	CADR4	ACADR4	RESERVED

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
161	AWAIT#	AWAIT#	RESERVED
162	CADR3	ACADR3	RESERVED
163	CADR2	ACADR2	DA2
164	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
165	REG#	AREG#/IDECFG	AREG#/IDECFG
166	CADR1	ACADR1	DA1
167	ABVD2/SPKR#	ABVD2/SPKR#	RESERVED
168	CADR0	ACADR0	DA0
169	ABVD1/STSCHG#	ABVD1/STSCHG#	RESERVED
170	CDATA0	ACDATA0	DD0
171	CDATA8	ACDATA8	DD8
172	CDATA1	ACDATA1	DD1
173	CDATA9	ACDATA9	DD9
174	CDATA2	ACDATA2	DD2
175	CDATA10	ACDATA10	DD10
176	AWP/IOIS16#	AWP/IOIS16#	IOCS16#
177	ACD2#	ACD2#	RESERVED
178	BCD1#	BCD1#	BCD1#
179	BCE1#	BCE1#	BCE1#
180	BCE2#	BCE2#	BCE2#
181	BVS1	BVS1	BVS1
182	AINSERT#	BOE#	BOE#
183	SLOTPWR (5V)	SLOTPWR (5V)	SLOTPWR (5V)
184	IOCS16#	BIORD#	BIORD#
185	IORDY	BIOWR#	BIOWR#
186	HOLDLED#	BCADR13	BCADR13
187	AENABLE#	BCADR14	BCADR14
188	BWE#/PGM#	BWE#/PGM#	BWE#/PGM#
189	BRDY-BSY#/IREQ#	BRDY-BSY#/IREQ#	BRDY-BSY#/IREQ#
190	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)	V_{SS} (OUTPUTS)
191	EXTDIR	BCADR21	BCADR21
192	BENABLE#	BCADR22	BCADR22
193	BRESET	BRESET	BRESET

Table 5. Pin Cross-Reference (Continued)

Pin	Mode 1 Pin Name (Four Sockets)	Mode 0 Pin Name (Two Sockets)	Mode 0 Pin Name (One Socket + IDE)
194	BVS2	BVS2	BVS2
195	BWAIT#	BWAIT#	BWAIT#
196	PDIR#	BCADR3	BCADR3
197	SIRQ	BCADR2	BCADR2
198	PIRQ	BCADR1	BCADR1
199	BINSERT#	BREG#	BREG#
200	V_{SS} (INPUTS)	V_{SS} (INPUTS)	V_{SS} (INPUTS)
201	VDD (5V)	VDD (5V)	VDD (5V)
202	BBVD2/SPKR#	BBVD2/SPKR#	BBVD2/SPKR#
203	CINSERT#	BCADR0	BCADR0
204	BBVD1/STSCHG#	BBVD1/STSCHG#	BBVD1/STSCHG#
205	BWP/IOIS16#	BWP/IOIS16#	BWP/IOIS16#
206	BCD2#	BCD2#	BCD2#
207	CCD1#	BCDATA3	BCDATA3
208	CCE[1]#	BCADR[8]	BCADR[8]

3.0 PPEC REGISTER DESCRIPTIONS

The PPEC registers consist of PCI configuration registers, and PCMCIA Socket Configuration registers. The PCI configuration registers are classified as PCI-PCMCIA Bridge PCI Configuration Registers, or PCI-IDE Interface PCI Configuration Registers. The PCMCIA Socket Configuration registers are classified as General Setup Registers, Interrupt Registers, I/O Mapping Control Registers, or Memory Mapping Control Registers.

Several PPEC registers contain reserved bits or fields labeled "Reserved" that must be handled correctly by software. During reads, software must mask the reserved bits as undefined. During writes, software must ensure that the values of the reserved bits are preserved by first reading the reserved bits, merging the reserved bit values with the new values of the non-reserved bits, then writing the data.

Several bits are described as "not implemented" in the register descriptions. These bits correspond to PCI-defined functions that are not implemented in the PPEC, but are described to facilitate tracking of PCI-supported features.

3.1 PCI Configuration Registers

The PPEC supports PCI-PCMCIA Bridge and PCI-IDE Interface functions. These functions can be configured independently with two sets of PCI configuration registers in compliance with the PCI Local Bus Specification Revision 2.0. The two sets of configuration registers are accessed through a mechanism defined for multi-functional PCI devices. The PCI-PCMCIA Bridge configuration registers are addressed as a function #0 with AD[10:8] as shown in the following table, and the PCI-IDE Interface configuration registers are addressed as a function #1. Attempted access of a register in the 2–7 function range results in no response by the PPEC and a PCI-master abort.

Functions are accessed by AD[10:8] during the address phase of the configuration cycle as follows:

AD[10:8]	PPEC PCI Function Addressed
000	#0: PCI-PCMCIA Bridge
001	#1: PCI-IDE Interface
010 through 111	none (Reserved)

Note that the control bits for certain PCI functions that are defined in the PCI Specification but not used in the PPEC are shown in the configuration registers, but are described as "not implemented".

Table 6. PCI-PCMCIA Bridge PCI Configuration Registers

Address Offset	Mnemonic	Register Name	Access
00–01h	VENID	Vendor ID	RO
02–03h	DEVID	Device ID	RO
04–05h	PCICMD	PCI Command	R/W
06–07h	PCISTS	PCI Status	RO
08h	REVID	Revision ID	RO
09–0Bh	CCODE	Class Code (CCPIB and CCCB)	RO
0C–0Dh		Reserved	
0Eh	HTYPE	Header Type	RO
0Fh		Reserved	
10–13h	PBBA	PCI-PCMCIA Bridge Base Address	R/W
14–3Bh		Reserved	
3Ch	INTLIN	Interrupt Line	R/W
3Dh	INTPIN	Interrupt Pin	R/W
3E–3Fh		Reserved	
40h	PCICON	PCI Configuration Control	R/W
41–4Fh		Reserved	
50h	PPIRR	PCMCIA-PCI Interrupt Routing Register	
51–FFh		Reserved	

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3.1.1 PPEC FUNCTION #0—PCI-PCMCIA BRIDGE PCI CONFIGURATION REGISTERS

The PCI-PCMCIA Bridge PCI Configuration Registers, listed in Table 6, are 8-bit, 16-bit, and 32-bit registers. Particular bytes within 16-bit and 32-bit register are selected with byte enables. Reserved registers and bits are reserved for future use, and writing to them has no effect. When writing to a register with reserved bits, the reserved bits should be read first, then properly masked and written back to prevent future software incompatibility.

3.1.1.1 VENID—Vendor ID

Register Offset: 00h
Default Value: 8086h
Access: Read Only
Size: 16 bits

This is a unique 16 bit value assigned to a vendor that, together with the Device ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Vendor Identification
This is a 16-bit value assigned to Intel.

3.1.1.2 DEVID—Device ID

Register Offset: 02h
Default Value: 1221h
Access: Read Only
Size: 16 bits

This is a unique 16 bit value that is assigned to the PCI-PCMCIA Bridge function. The Device ID, together with the Vendor ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Device Identification
This value identifies the PCI-PCMCIA Bridge function.

3.1.1.3 PCICMD—PCI Command

Register Offset: 04h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This 16 bit register contains PCI control information.

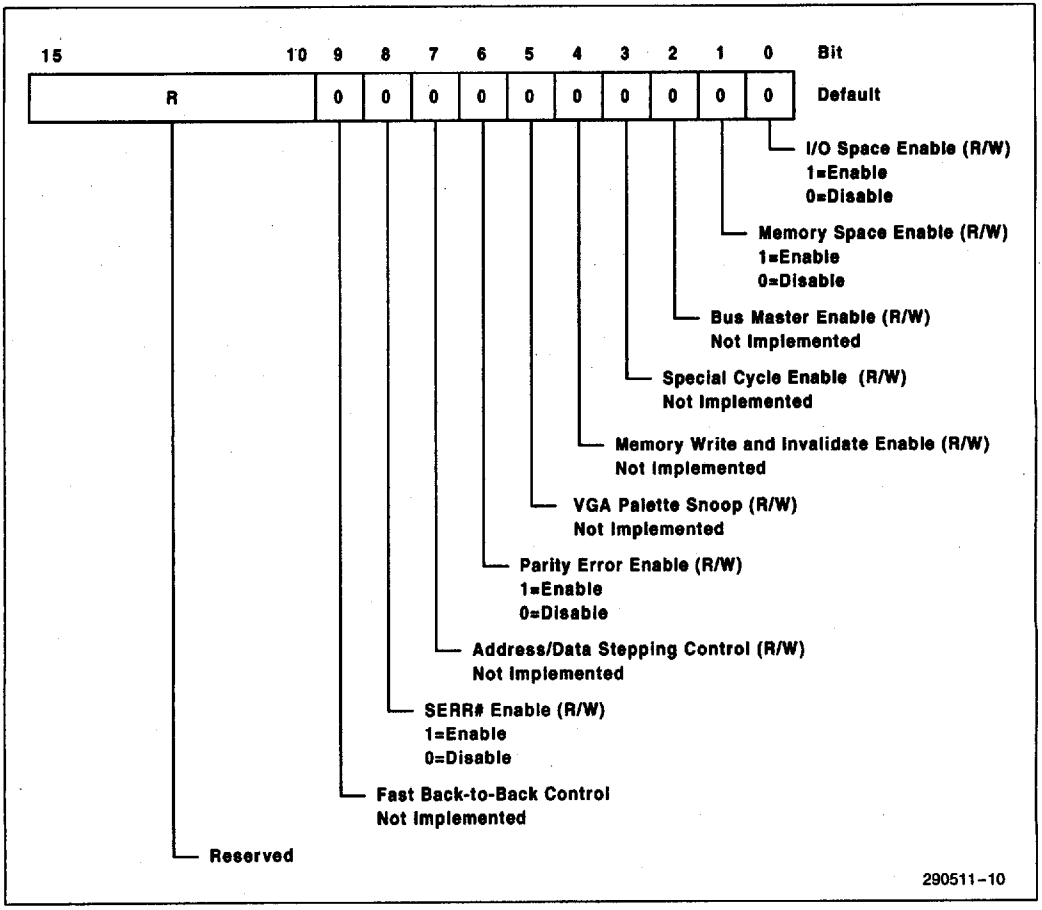

Figure 6. PCI Command Register

Bits[15:10]: Reserved

Bit 9: Fast Back-to-Back Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 8: SERR# Enable
When this bit is set to 1, the PPEC asserts SERR# when it detects a parity error during an address phase, and when it detects an X.X PC Card in Mode 1, partially-buffered implementations. When this bit is set to 0, SERR# is not asserted for any reason. Reset sets the bit to 0.

Bit 7: Address/Data Stepping Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 6: Parity Error Enable
This bit controls PPEC response to PCI data parity errors. When this bit is set to 1, the PPEC activates PERR# when it detects a parity error during a data phase. When this bit is set to 0, the PPEC ignores parity errors. Reset sets the bit to 0 and disables data parity checking.

Bit 5: VGA Palette Snoop
This bit is intended only for specific control of PCI-based VGA devices, and is not applicable to the PPEC. The bit is not implemented, and always reads "0".

Bit 4: Memory Write and Invalidate Enable
This control function can be used only by the PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 3: Special Cycle Enable
This bit is intended to enable response to supported special cycles. Since the PPEC does not respond to any special cycle, the bit is not implemented and always reads "0".

Bit 2: Bus Master Enable
This bit is intended to enable mastership of the PCI. Since the PPEC cannot be a PCI master, the bit is not implemented and always reads "0".

Bit 1: Memory Space Enable
This bit enables the PPEC to accept PCI-originated memory cycles. When the bit is set to 0, the PPEC does not respond to PCI memory cycles to PCMCIA cards, and the PPEC DEVSEL# logic is inhibited during the memory cycles.

Bit 0: I/O Space Enable
This bit enables the PCI-PCMCIA Bridge to accept PCI-originated I/O cycles. When the bit is set to 0, the PPEC does not respond to PCI master I/O cycles, and the PPEC DEVSEL# logic is inhibited during the I/O cycles.

3.1.1.4 PCISTS—PCI Status

Register Offset:	06h
Default Value:	0480h
Access:	Read Only (*see description)
Size:	16-bits

This 16-bit register is used to record status information for PCI bus-related events. Reads to this register behave normally. Writing bits 11, 14, and 15 to 1 set the bits to 0. The other register bits cannot be written.

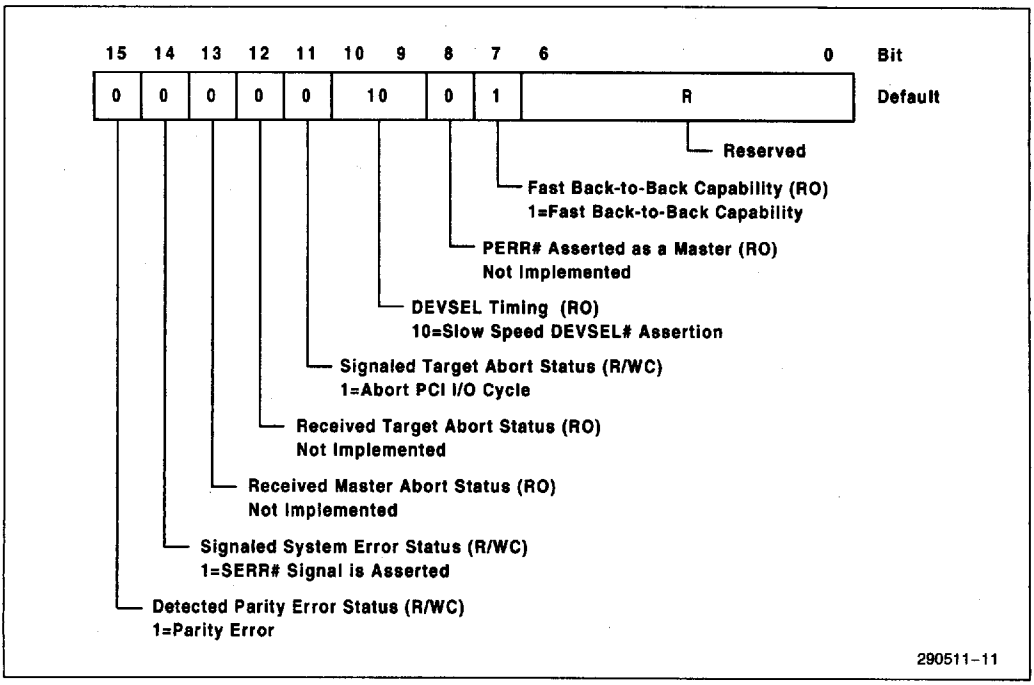

Figure 7. PCI Status Register

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Bits 15: Detected Parity Error Status
This bit is to be set whenever the 82092AA as a target detects a parity error during the data phase, even if parity error handling is disabled (as controlled by bit 6 in the *PCI Command* register). DEFAULT=0.

Bit 14: Signaled System Error Status
This bit is used to indicate that PCI device asserted SERR# signal. The 82092AA will assert this bit whenever it generates address phase parity error via SERR# pin. DEFAULT=0.

Bit 13: Received Master Abort Status (not applicable)
Since this control function can be used only by the PCI master it is not implemented and the bit is always read as a "0" (disabled).

Bit 12: Received Target Abort Status (not applicable)
Received Target Abort Sataus by the PCI master. Since this control function can be used only by the PCI master it is not implemented and the bit is always read as a "0" (disabled).

Bit 11: Signaled Target Abort Status
This bit is to be set by PCI target devices when they generate a Target Abort.

The 82092AA generates Target Abort in the case when it is the target of the PCI I/O cycle and address/byte-enable combination is invalid. More details are provided in Section 1.6.1.5, Transaction Termination.

Bit[10:9]: DEVSEL Timing
These read-only bits encode the timing of DEVSEL# when 82092AA responds as a Target. PCI Specification defines three allowable timings for assertion of DEVSEL#: 00b=fast, 01b=medium, and 10b=slow (11b is reserved). These bits are Read-Only and they indicate the slowest time that a device asserts DEVSEL# for any bus command except *Configuration Read* and *Configuration Write*. The 82092AA PCI-IDE function implements medium speed DEVSEL# timing and therefore these bits contain value 01b.

Bit 8: PERR# Asserted as a Master
This control function can be used only by a PCI master. Therefore this control function is not implemented and the bit will be always read as a "0" (disabled).

Bit 7: Fast Back-to-Back Capability
This read-only bit indicates PCI target capability to support fast back-to-back cycles. The 82092AA can support this type of cycle originated by any PCI master and therefore this bit is set to "1". DEFAULT=1.

Bit[6:0]: Reserved

3.1.1.5 REVID—Revision ID

Register Offset:	08h
Default Value:	01h
Access:	Read Only
Size:	8 bits

This 8 bit register contains device revision information. Writes to this register have no effect.

Bits[7:0]: Revision Identification
This is the revision level of the PPEC. The initial PPEC revision level is 01h.

3.1.1.6 CCPIB—Class Code-Programming Interface Byte

Register Offset:	09h
Default Value:	00h
Access:	Read Only
Size:	8 bits

This 8 bit register contains device Programming Interface information related to the Class Code bytes located at 0Ah offset. Writes to this register have no effect.

Bits[7:0]: Programming Interface
There are no specific register-level programming interfaces defined for this Class Code (indicated by register CCCB). Therefore, the value of this field is 0.

3.1.1.7 CCCB—Class Code-Class Code Bytes

Register Offset:	0Ah
Default Value:	0605h
Access:	Read Only
Size:	16 bits

This 16-bit register contains device Class Code bytes in the following format: [BASE CLASS][SUB-CLASS]. Writes to this register have no effect.

Bits[15:8]: Base Class
The value 06h in this field identifies the function class as a *bus bridge.*

Bits[7:0]: Sub-Class
The value 05h in this field identifies the function sub-class as a *PCMCIA bridge.*

3.1.1.8 HTYPE—Header Type

Register Offset: 0Eh
Default Value: 80h
Access: Read Only
Size: 8 bits

This register indicates whether or not the device contains multiple functions, and identifies the layout of bytes 10h through 3Fh in configuration space. Bit 7 indicates a multi-functional device when set to 1. Bits[6:0] specify layout of bytes 10h-3Fh. The PPEC uses layout type #0 as defined in the PCI specification. Writes to this register have no effect.

Bit 7: Multifunction Indicator
This bit is set to 1 to indicate that the PPEC is a multifunctional device.

Bits[6:0]: Byte Layout
This field specifies layout type "0" for bytes 10-3Fh, as defined in the PCI specification.

3.1.1.9 PBBA—PCI-PCMCIA Bridge Base Address

Register Offset: 10h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the PCMCIA Index/Data Socket Configuration registers mapped in the system I/O space. PCMCIA Index/Data Socket Configuration registers allow indirect access to the block of PCMCIA socket control registers which consists of 256 8-bit locations divided into four sub-blocks, each containing 64 8-bit configuration registers that control the operations of particular PCMCIA socket.

PCMCIA Index/Data Registers can be mapped anywhere in 4 GByte I/O space on a Dword boundary. They provide 82365SL-compatible windowing access to the PCMCIA socket control/configuration registers. The 82365SL-compatible PCMCIA configuration registers access via Index/Data registers implies that Index is an 8-bit I/O port located at [BASEADDRESS], and Data is an 8-bit I/O port located at [BASEADDRESS] + 1.

Bits[31:2]: Base Address
This value determines the starting address of the PCMCIA Index/Data Socket Configuration registers mapped in the system I/O space.

Bit 1: Reserved

Bit 0: I/O Space Indicator
This bit is set to 1 to indicate I/O space.

NOTE:
Accesses to locations BASEADDRESS + 2 and BASEADDRESS + 3 are not permitted. These accesses may cause errors that are not reported to the system.

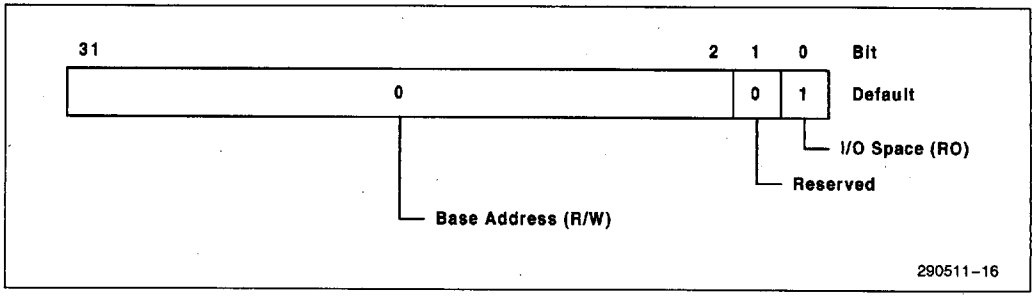

Figure 8. PCI-PCMCIA Bridge Base Address Register

3.1.1.10 INTLIN—Interrupt Line

Register Offset: 3Ch
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register is used to communicate interrupt line routing information. BIOS software must initialize this register during system configuration. The value in this register identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected. Device drivers and the operating system can use this information to determine priority and vector information. The value in this register is system architecture specific.

Bits[7:0]: Interrupt Line Identification
The value in this field identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected.

NOTE:
The PCI-PCMCIA Bridge can connect to system interrupt controllers in two different ways:

a. via a single PCI interrupt signal line INTA#, that requires additional routing (system specific).
b. via 10 direct system interrupt signals.

Mode (b) is provided to allow PCMCIA software that requires "ISA compatibility" (i.e., non-shareable IRQ handlers that require specific IRQ level) to run without modifications on Intel-architecture platforms with the PPEC as a PCI-PCMCIA Bridge. In this case, the PCI interrupt scheme is not used, but the PCMCIA Card interrupts (as well as the Card Status Change interrupt) are configured to connect directly to specific system IRQ lines. The PCI Interrupt Line and the PCMCIA-PCI Interrupt Routing Register (PPIRR) remain in default state 0. Designs that are not dependent on this type of software "compatibility" can use PCI interrupt scheme using mechanism (a).

3.1.1.11 INTPIN—Interrupt Pin

Register Offset: 3Dh
Default Value: 01h
Access: Read Only
Size: 8 bits

This register is used to indicate that the PCI-PCMCIA Bridge uses the INTA# PCI Interrupt Pin for signaling PC Card interrupts (Card Status Change and/or I/O Interrupts). The PCMCIA-PCI Interrupt Routing Register (PPIRR, located at offset 50h) is used to enable (per PC Card) signaling of interrupts using the PCI interrupt scheme.

Bits[7:0]: Interrupt Pin Selection
The value in this field, 01h, identifies the interrupt pin used by the PPEC's PCI-PCMCIA Bridge function as INTA#.

3.1.1.12 PCICON—PCI Configuration Control

Register Offset: 40h
Default Value: XXh
Access: Read/Write
Size: 8 bits

The default is determined by the PCMCIA and IDE configurations as defined in the PCMCIA Interface description in this document.

Bit 0: PCICLK Configuration
This read/write bit defines the system PCICLK frequency. It must be initialized by the system software to provide optimized timing for 25 MHz or 33 MHz. as follows:

1 = 25 MHz PCICLK
0 = 33 MHz PCICLK

Bits[7:6]: Reserved

Bit 5: Enhanced PCMCIA Timing Mode Enable
When set to 1, this bit enables enhanced PCMCIA timing mode. When set to 0, the PPEC timing is 82365SL compatible manner as far as timing control based on the SMSTH0 PCMCIA memory window control register is concerned. The slowest 365 timing is selected and all writes to the enhanced timing mode bits are ignored. When set to 1, the enhanced timing control is enabled.

Bit 4: Global PCMCIA Read-Prefetch Buffering Enable
This bit globally enables PCI to PCMCIA data buffering for Prefetch Read operations when set to 1. When set to 0, buffered operations are disabled.

Bit 3: Global PCMCIA Post-Write Buffering Enable
This bit globally enables PCI to PCMCIA data buffering for Post Write operations when set to 1. When set to 0, buffered operations are disabled.

This register provides read-only configuration information and data buffering enable/disable function.

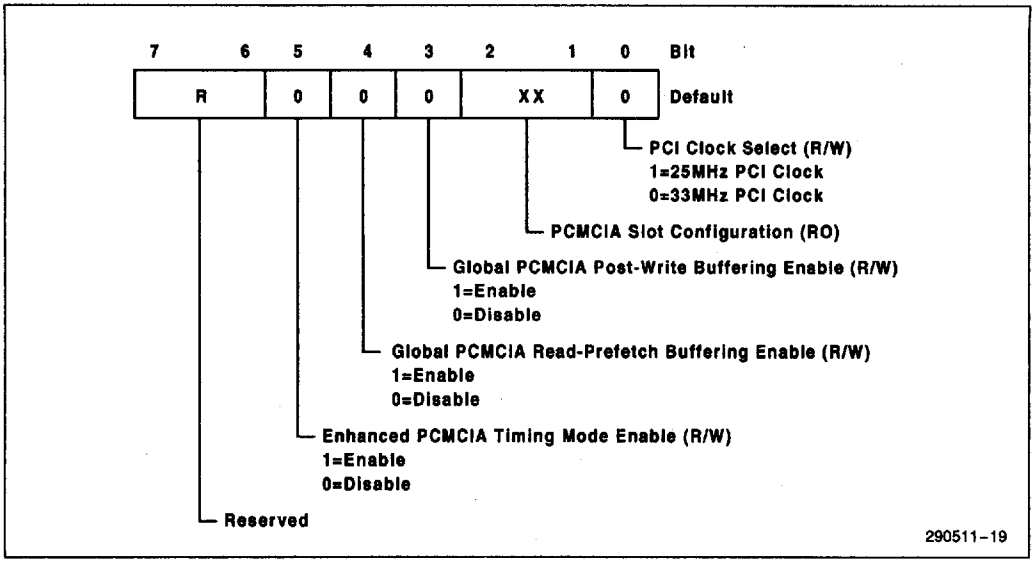

Figure 9. PCI Configuration Control Register

Bits[2:1]: PCMCIA Socket Configuration
These two read-only bits define the PCMCIA socket configuration (i.e., the number of supported sockets based on PCMCIA interface and IDE interface pin configuration) as follows:

Bit2	Bit1	Configuration
0	0	2 PCMCIA Sockets (2-Socket Mode)
0	1	1 PCMCIA Socket And IDE (2-Socket Mode)
1	X	4 PCMCIA Sockets (4-Socket Mode)

3.1.1.13 PPIRR—PCMCIA-PCI Interrupt Routing Register

Register Offset: 50h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows mapping of PCMCIA interrupts to either ISA interrupts, or PCI interrupts. Two interrupts, Card Status Interrupt and Card I/O Interrupt, can be generated and independently routed for each socket. When a register bit is set to 0, the corresponding interrupt is routed via one of the 10 system interrupt lines (ISA mechanism) as specified in the Interrupt and General Control Register and the Card Status Change Interrupt Configuration Register. When a bit is set to 1, the corresponding interrupt is routed via INTA# (PCI mechanism).

Bit 7: Socket D Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 6: Socket D Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 5: Socket C Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 4: Socket C Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 3: Socket B Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

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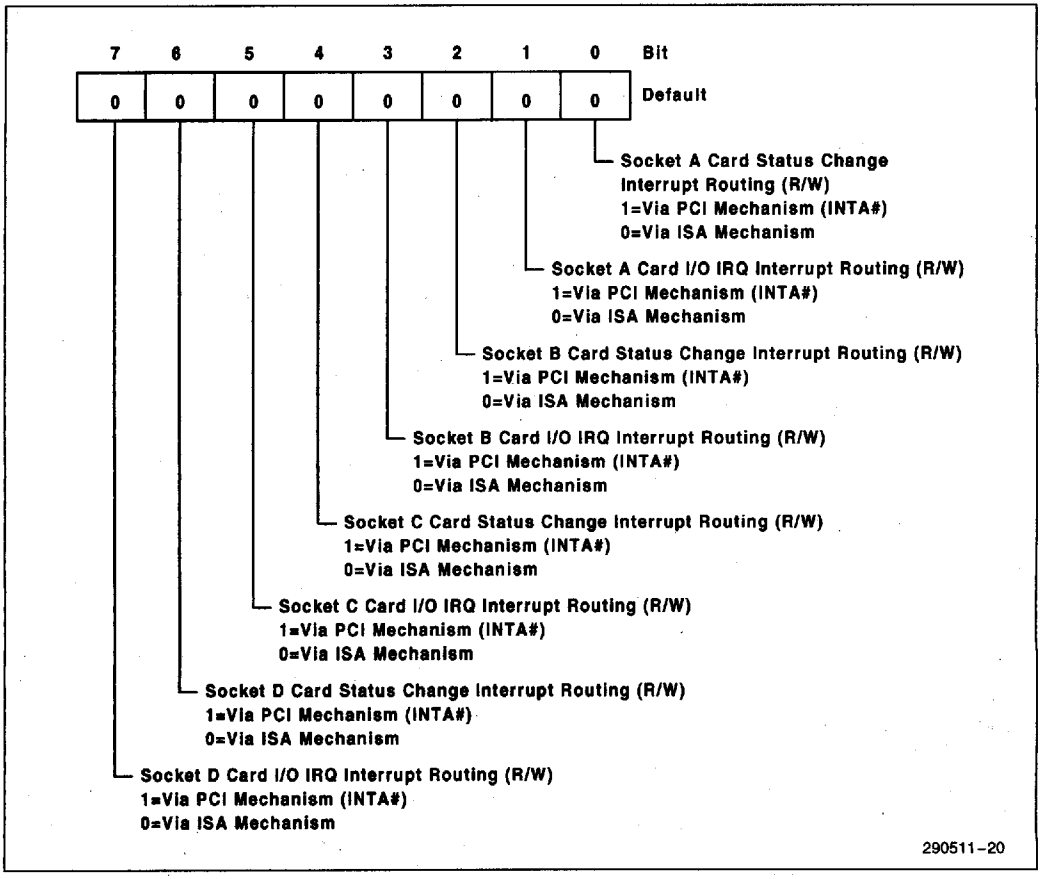

Figure 10. PCMCIA Interrupt Routing Register

Bit 2: Socket B Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 1: Socket A Card I/O IRQ Interrupt Routing
This bit selects Card I/O Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 0: Socket A Card Status Change Interrupt Routing
This bit selects Card Status Change Interrupt routing via the PCI mechanism, or the ISA mechanism.

3.1.2 PPEC Function #1—PCI-IDE Interface PCI Configuration Registers

The PCI-PCMCIA Bridge PCI Configuration Registers, listed in Table 7, are 8-bit, 16-bit, and 32-bit registers. Particular bytes within 16-bit and 32-bit registers are selected with byte enables. Reserved registers and bits are reserved for future use, and writing to them has no effect. When writing to a register with reserved bits, the reserved bits should be read first, then properly masked and written back to prevent future software incompatibility.

Table 7. PCI-IDE Interface PCI Configuration Registers

Address Offset	Mnemonic	Register Name	Access
00-01h	VENID	Vendor ID	RO
02-03h	DEVID	Device ID	RO
04-05h	PCICMD	PCI Command	R/W
06-07h	PCISTS	PCI Status	RO
08h	REVID	Revision ID	RO
09-0Bh	CCODE	Class Code (CCPIB and CCCB)	RO
0C-0Dh		Reserved	
0Eh	HTYPE	Header Type	RO
0Fh		Reserved	
10-13h	PDCBA	IDE Base Address #0—Primary IDE Data/Command	R/W
14-17h	PCSBA	IDE Base Address #1—Primary IDE Control/Status	R/W
18-1Bh	SDCBA	IDE Base Address #2—Secondary IDE Data/Command	R/W
1C-1Fh	SCSBA	IDE Base Address #3—Secondary IDE Control/Status	R/W
20-3Bh		Reserved	
3Ch	INTLIN	Interrupt Line	R/W
3Dh	INTPIN	Interrupt Pin	R/W
3E-3Fh		Reserved	
40h	PCICON	PCI Configuration Control	R/W
41-43h		Reserved	
44h	PIDECFG	Power-On IDE Configuration	R/W
45-47h		Reserved	
48-49h	PIDETC	Primary IDE Timing Control	R/W
4A-4Bh	SIDETC	Secondary IDE Timing Control	R/W
4Ch	IIIRR	IDE-ISA Interrupt Routing Register	R/W
4Dh	IDEICS	IDE Interrupt Configuration and Status Register	R/W
50h	PCIRR	IDE-PCI Interrupt Routing Register	R/W
51-FFh		Reserved	

3.1.2.1 VENID—Vendor ID

Register Offset: 00h
Default Value: 8086h
Access: Read Only
Size: 16 bits

This is a unique 16-bit value assigned to a vendor that, together with the Device ID, uniquely identifies each PCI device. Writes to this register have no effect.

Bits[15:0]: Vendor Identification
This is a 16-bit value assigned to Intel.

3.1.2.2 DEVID—Device ID

Register Offset: 02h
Default Value: 1222h
Access: Read Only
Size: 16 bits

This is a unique 16-bit value that is assigned to the PCI-IDE Interface function. Writes to this register have no effect.

Bits[15:0]: Device Identification
This value identifies the PCI-IDE Interface function.

3.1.2.3 PCICMD—PCI Command

Register Offset: 04h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This 16 bit register contains PCI control information.

Bits[15:10]: Reserved

Bit 9: Fast Back-to-Back Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 8: SERR# Enable
When this bit is set to 1, the PPEC asserts SERR# when it detects a parity error during an address phase, and when it detects an X.X PC Card in Mode 1, partially-buffered implementations. When this bit is set to 0, SERR# is not asserted for any reason. Reset sets the bit to 0.

Bit 7: Address/Data Stepping Control
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 6: Parity Error Enable
This bit controls PPEC response to PCI data parity errors. When this bit is set to 1, the PPEC activates PERR# when it detects a parity error during a data phase. When this bit is set to 0, the PPEC ignores parity errors. Reset sets the bit to 0 and disables data parity checking.

Bit 5: VGA Palette Snoop
This bit is intended only for specific control of PCI-based VGA devices, and is not applicable to the PPEC. The bit is not implemented, and always reads "0".

Bit 4: Memory Write and Invalidate Enable
This control function can be used only by the PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 3: Special Cycle Enable
This bit is intended to enable response to supported special cycles. Since the PPEC does not respond to any special cycle, the bit is not implemented and always reads "0".

Bit 2: Bus Master Enable
This bit is intended to enable mastership of the PCI. Since the PPEC cannot be a PCI master, the bit is not implemented and always reads "0".

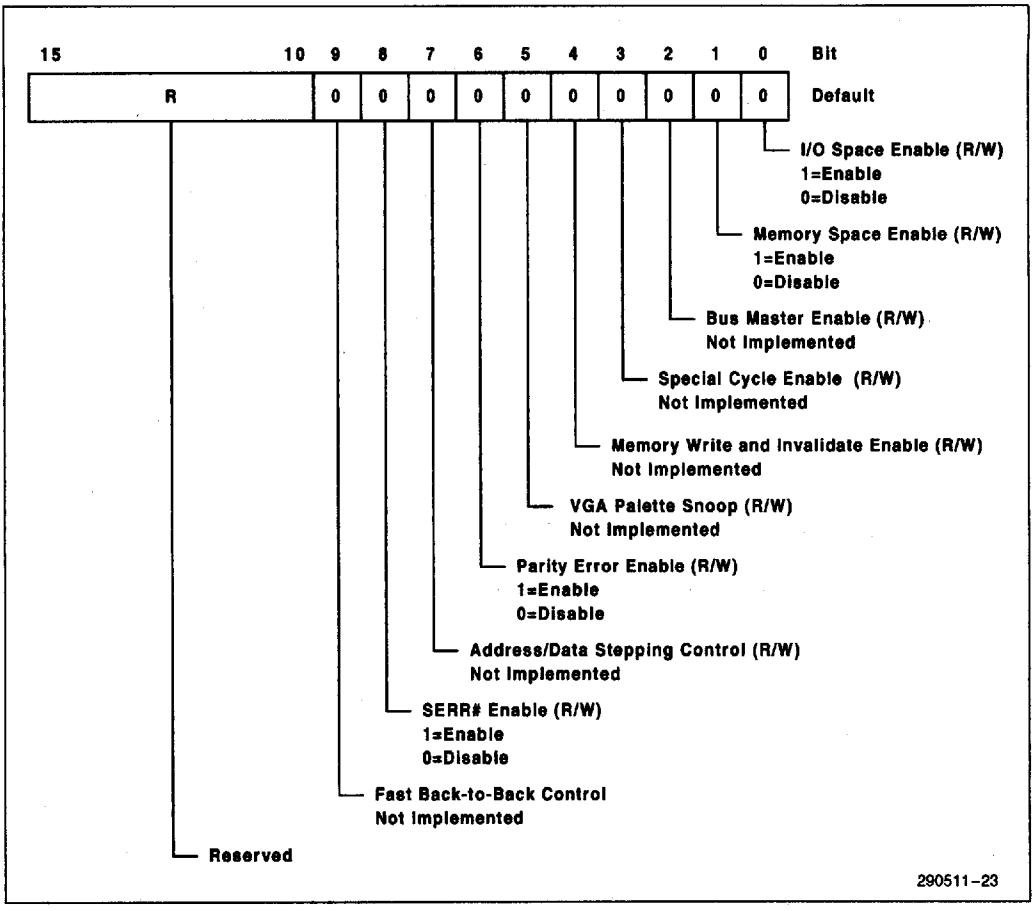

Figure 11. PCI Command Register

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Bit 1: Memory Space Enable
This bit is intended to enable acceptance of PCI-originated memory cycles. Since the PCI-IDE Interface does not use memory cycles, the bit is not implemented and always reads "0".

Bit 0: I/O Space Enable
This bit enables the PCI-IDE Interface to accept PCI-originated I/O cycles. When the bit is set to 0, the interface does not respond to PCI master I/O cycles, and the PPEC's PCI-IDE DEVSEL# logic is inhibited during the I/O cycles.

This 16 bit register is used to record status information for PCI bus-related events. Reads to this register behave normally. Writing bits 11, 14, and 15 to 1 set the bits to 0. The other register bits cannot be written.

Bit 15: Detected Parity Error Status
The PPEC sets this bit to 1 when, as a target, it detects a parity error during a data phase, even if parity error handling is disabled by bit 6 and bit 8 in the PCI Command Register.

3.1.2.4 PCISTS—PCI Status

Register Offset: 06h
Default Value: 0280h
Access: Read Only (see register description)
Size: 16 bits

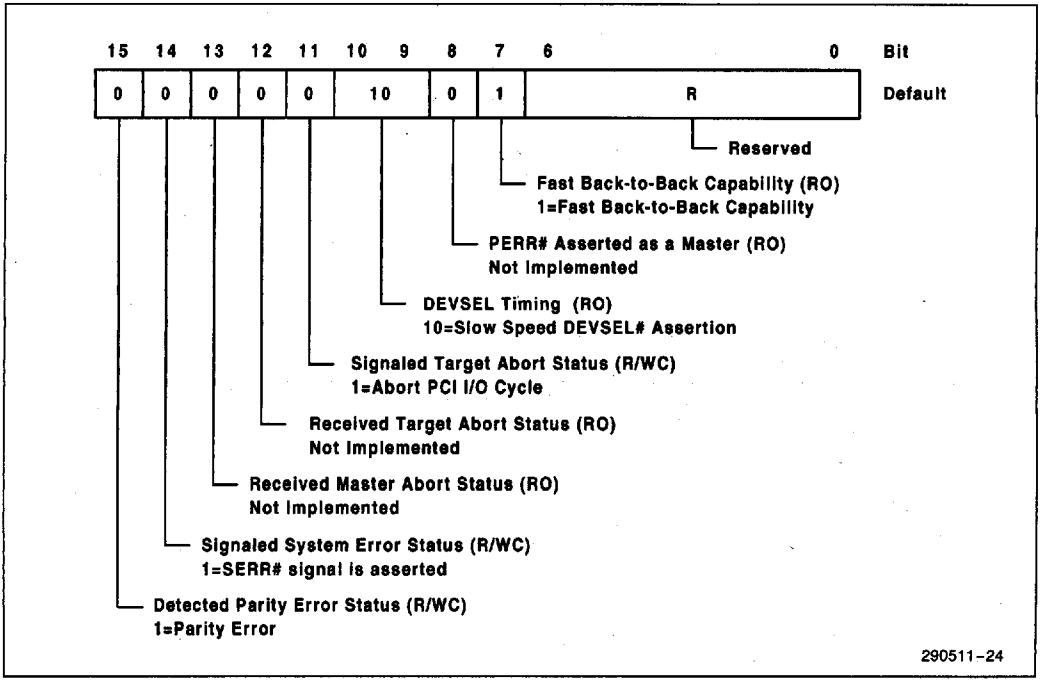

Figure 12. PCI Status Register

Bit 14: Signaled System Error Status
The PPEC sets this bit to 1 whenever it signals an address phase parity error by asserting SERR#.

Bit 13: Received Master Abort Status
This control function can be used only by a PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 12: Received Target Abort Status
This control function can be used only by a PCI master, and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 11: Signaled Target Abort Status
The PPEC sets this bit to 1 when it is the target of a PCI I/O cycle, and the address/byte-enable combination is invalid.

Bits[10:9]: DEVSEL Timing
These read-only bits identify the slowest DEVSEL# response time for all bus commands except *configuration read* and *configuration write*, as defined in the PCI Specification. The PPEC implements medium speed DEVSEL# timing for PCI-IDE functions, and the bits are therefore 10b.

Bit 8: PERR# Asserted as a Master
This control function can be used only by a PCI master and is therefore not implemented in the PPEC. The bit always reads "0" (disabled).

Bit 7: Fast Back-to-Back Capability
This read-only bit is set to 1 to indicate that the PPEC can support fast back-to-back cycles originated by a PCI master.

Bits[6:0]: Reserved

3.1.2.5 REVID—Revision ID

Register Offset:	08h
Default Value:	01h
Access:	Read Only
Size:	8 bits

This 8-bit register contains device revision information. Writes to this register have no effect.

Bits[7:0]: Revision Identification
This is the revision level of the PPEC. The initial PPEC revision level is 01h.

3.1.2.6 CCPIB—Class Code-Programming Interface Byte

Register Offset:	09h
Default Value:	00h
Access:	Read Only
Size:	8 bits

This 8-bit register contains device Programming Interface information related to the Class Code register located at 0Ah offset. Writes to this register have no effect.

Bits[7:0]: Programming Interface
There are no specific register-level programming interfaces defined for this Class Code (indicated by register CCCB). Therefore, the value of this field is 0.

3.1.2.7 CCCB—Class Code-Class Code Bytes

Register Offset:	0Ah
Default Value:	0101h
Access:	Read Only
Size:	16 bits

This 16-bit register contains device Class Code information in the following format: [BASE CLASS][SUB-CLASS]. Writes to this register have no effect.

Bits[15:8]: Base Class
The value 01h in this field identifies the function class as a *mass storage controller*.

Bits[7:0]: Sub-Class
The value 01h in this field identifies the function subclass as an *IDE Controller*.

3.1.2.8 HTYPE—Header Type

Register Offset:	0Eh
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register indicates whether or not the device contains multiple functions, and identifies the layout of bytes 10h through 3Fh in configuration space. Bit 7 indicates s multifunctional device when set to 1. Bits[6:0] specify layout of bytes 10h-3Fh. The PPEC uses layout type #0 as defined in the PCI specification. Writes to this register have no effect.

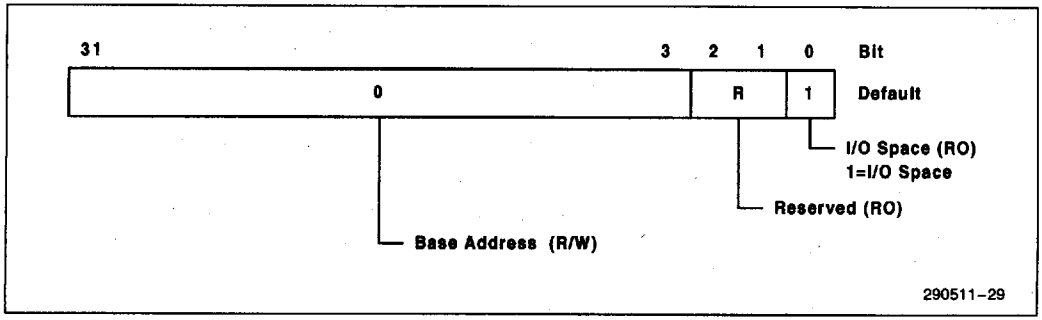

Figure 13. IDE Base Address Register 0

Bit 7: Multifunction Indicator
This bit is set to 1 to indicate that the PPEC is a multifunctional device.

Bits[6:0]: Byte Layout
This field specifies layout type "0" for bytes 10-3Fh, as defined in the PCI Specification.

3.1.2.9 PDCBA—IDE Base Address #0-Primary IDE Data/Command Address Range

Register Offset: 10h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the primary IDE I/O address range for the Data/Command register block. It can be mapped anywhere in 4 GByte space on an 8-byte boundary.

The address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress +7.

Bits[31:3]: Base Address
This field holds the programmable base address of the primary IDE I/O address range for the Data/Command register block.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
The PCI-compliant Base Address mechanism can be used for motherboard PPEC/IDE applications with PCI-customized BIOS. For applications that must use IDE functions in an ISA-compatible manner (e.g. PPEC add-in card with system BIOS that does not support PPEC-IDE), the address ranges defined with the four IDE BASE registers can be disabled by selecting the IDE hardware configuration feature in the IDE Power-On Configuration register. This feature allows configuration of IDE addresses for the compatible ranges, and selection of enhanced IDE timing mode. The compatible ranges are:

- Primary Data/Command Ports: 1F0-1F7h
- Primary Control/Status Ports: 3F6h
- Secondary Data/Command Ports: 170-177h
- Secondary Control/Status Ports: 376h

This PPEC feature eliminates the need for custom software for the IDE function, and applies to all four IDE Base Address Registers.

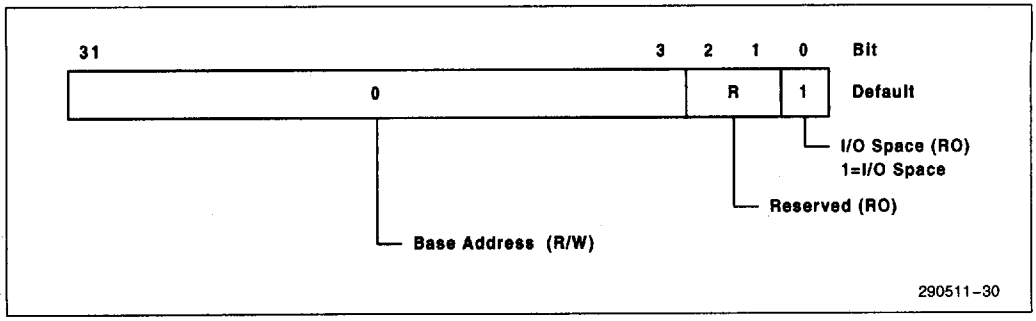

Figure 14. IDE Base Address Register 1

3.1.2.10 PCSBA—IDE Base Address #1-Primary IDE Control/Status Address Range

Register Offset: 14h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the primary IDE I/O address range for the Control/Status register block. It can be mapped anywhere in 4 GByte I/O space on an 8-byte boundary.

The Primary address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the primary IDE I/O address range for the Control/Status register block. These bits are read/write which indicates that the size of the required I/O address range is 8 bytes. In practical applications, only a subset of this range (1 byte) is used to access IDE registers.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
When accessing Control/Status Registers, proper offset must be used – 6h to access address xxx6h (Alternate Status Register).

3.1.2.11 SDCBA—IDE Base Address #2-Secondary IDE Data/Command Address Range

Register Offset: 18h
Default value: 0000 0001h
Access: Read/Write
Size: 32 bits

This register determines the starting address of the secondary IDE I/O address range for the Data/Command register block. It can be mapped anywhere in 4 GByte space on an 8-byte boundary.

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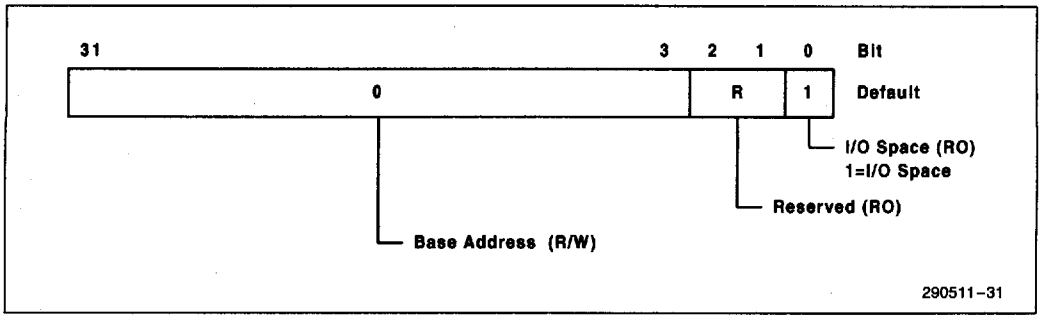

Figure 15. IDE Base Address Register 2

The address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the secondary IDE I/O address range for the Data/Command register block.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

3.1.2.12 SCSBA—IDE Base Address #3-Secondary IDE Control/Status Address Range

Register Offset:	1Ch
Default value:	0000 0001h
Access:	Read/Write
Size:	32 bits

This register determines the starting address of the secondary IDE I/O address range for the Control/Status register block. It can be mapped anywhere in 4 GByte I/O space on an 8-byte boundary.

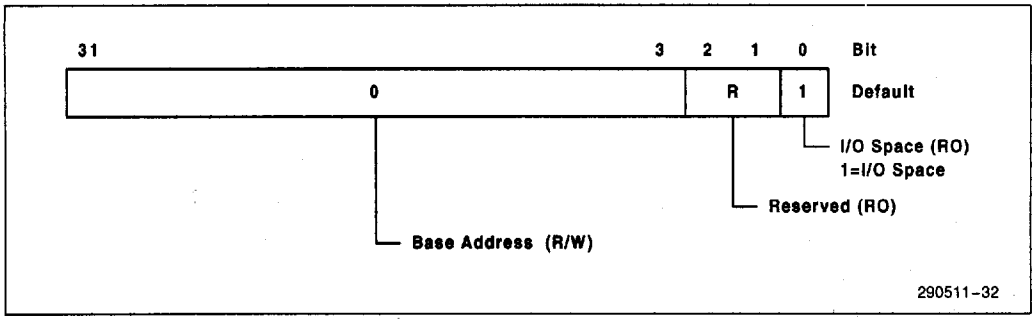

Figure 16. IDE Base Address Register 3

Secondary IDE Control/Status address range is defined as follows:

BaseAddress ≤ address ≤ BaseAddress + 7.

Bits[31:3]: Base Address
This field holds the programmable base address of the secondary IDE I/O address range for the Control/Status register block. These bits are read/write, which indicates that the size of the required I/O address range is 8 bytes. In practical applications, only a subset of this range (2 bytes) is used to access IDE registers.

Bits[2:1]: Reserved

Bit 0: I/O Space
This read only bit is set to 1 to indicate I/O space.

NOTE:
When accessing Control/Status Registers, proper offset must be used–6h to access address xxx6h (Alternate Status Register).

3.1.2.13 INTLIN—Interrupt Line

Register Offset:	3Ch
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This register is used to communicate interrupt line routing information. BIOS software must initialize this register during system configuration. The value in this register identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected. Device drivers and the operating system can use this information to determine priority and vector information. The value in this register is system architecture specific.

Bits[7:0]: Interrupt Line Identification
The value in this field identifies the interrupt request level of the system interrupt controller(s) to which the PPEC interrupt pin is connected.

NOTE:
The IDE Interface can connect to system interrupts in two different ways:

a. via a single PCI interrupt signal line (INTB#) that requires additional routing (system specific).

b. via 10 direct system interrupt signals (ISA mechanism).

Mode (b) is provided so that 'ISA compatible' IDE BIOS software can be used without modifications on X86/Pentium™-based platforms with the PPEC as a PCI-IDE Interface Controller. In this case, PCI interrupts are not used. IDE interrupts are configured to connect directly to a specific system IRQ line as specified in the IDE-ISA Interrupt Routing Register (IIIRR). The PCI Interrupt Line Register (INTLN) and the IDE-PCI Interrupt Routing Register (PCIRR) must remain in default state 0. Designs that do not require this software compatibility can use the PCI interrupt mechanism (a).

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3.1.2.14 INTPIN—Interrupt Pin

Register Offset: 3Dh
Default Value: 02h
Access: Read Only
Size: 8 bits

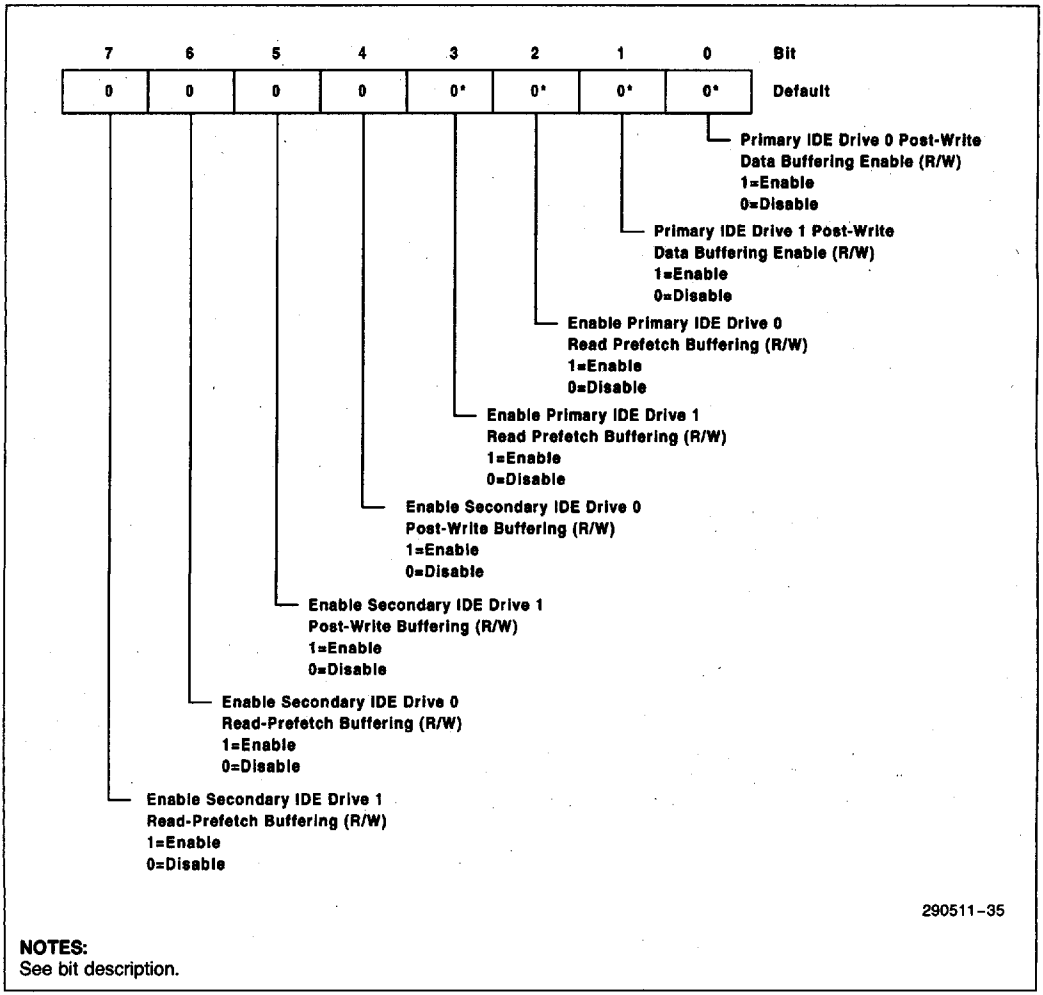
The value in this register, 02h, identifies the interrupt pin used by the PCI-IDE Interface for signaling IDE interrupts (Primary and/or Secondary IRQs) as INTB#. The IDE-PCI Interrupt Routing Register (PCIRR, located at offset 50h) is used to enable (for each IDE interface) interrupt signaling using the PCI interrupt scheme.

Bits[7:0]: Interrupt Pin Selection
The value in this field, 02h, identifies the PCI interrupt pin that is used by the PCI-IDE Interface device function as INTB#.

3.1.2.15 PCICON—PCI Configuration Control

Register Offset: 40h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register provides control of PCI-IDE data buffering.



NOTES:
See bit description.

Figure 17. PCI Configuration Control Register

Bit 7: Enable Secondary IDE Drive 1 Read-Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled.

Bit 6: Enable Secondary IDE Drive 0 Read-Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 0 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled.

Bit 5: Enable Secondary IDE Drive 1 Post-Write Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Post-Write operations. When the bit is set to 0, the buffering is disabled.

Bit 4: Enable Secondary IDE Drive 0 Post-Write Buffering
When this bit is set to 1, PCI to secondary IDE Drive 0 data buffering is enabled for Post-Write operations. When the bit is set to 0, the buffering is disabled.

Bit 3: Enable Primary IDE Drive 1 Read Prefetch Buffering
When this bit is set to 1, PCI to secondary IDE Drive 1 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 2: Enable Primary IDE Drive 0 Read Prefetch Buffering
When this bit is set to 1, PCI to primary IDE Drive 0 data buffering is enabled for Read Prefetch operations. When the bit is set to 0, the buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 1: Enable Primary IDE Drive 1 Post-Write Buffering
When this bit is 1, PCI to secondary IDE Drive 1 Post-Write data buffering is enabled. When this bit is 0, buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

Bit 0: Primary IDE Drive 0 Post-Write Buffering
When this bit is 1, PCI to primary IDE Drive 0 Post-Write data buffering is enabled. When this bit is 0, buffering is disabled. The default value of this bit is dependent on the IDE Hardware Configuration feature. If IDE Hardware Configuration is enabled (bit 0 of the PIDECFG register is set to 1), the bit defaults to the value of bit 7 of the PIDECFG register. If IDE Hardware Configuration is not enabled, the bit defaults to 0.

3.1.2.16 PIDECFG—Power-On IDE Configuration

Register Offset:	44h
Default Value:	xxh
Access:	Read/Write
Size:	8 bits

This register reports the status of the IDE Hardware Configuration signals that are multiplexed on PCMCIA Socket A data lines ACDATA[7:0] when the PPEC operates in Mode 0 (2-socket mode), and on common data lines CDATA[7:0] when the PPEC operates in Mode 1 (4-socket mode). The status of these signals is latched in this register during reset if this feature is enabled by the global IDE Hardware Configuration enable pin. These bits control the preload default value in the IDE timing control registers.

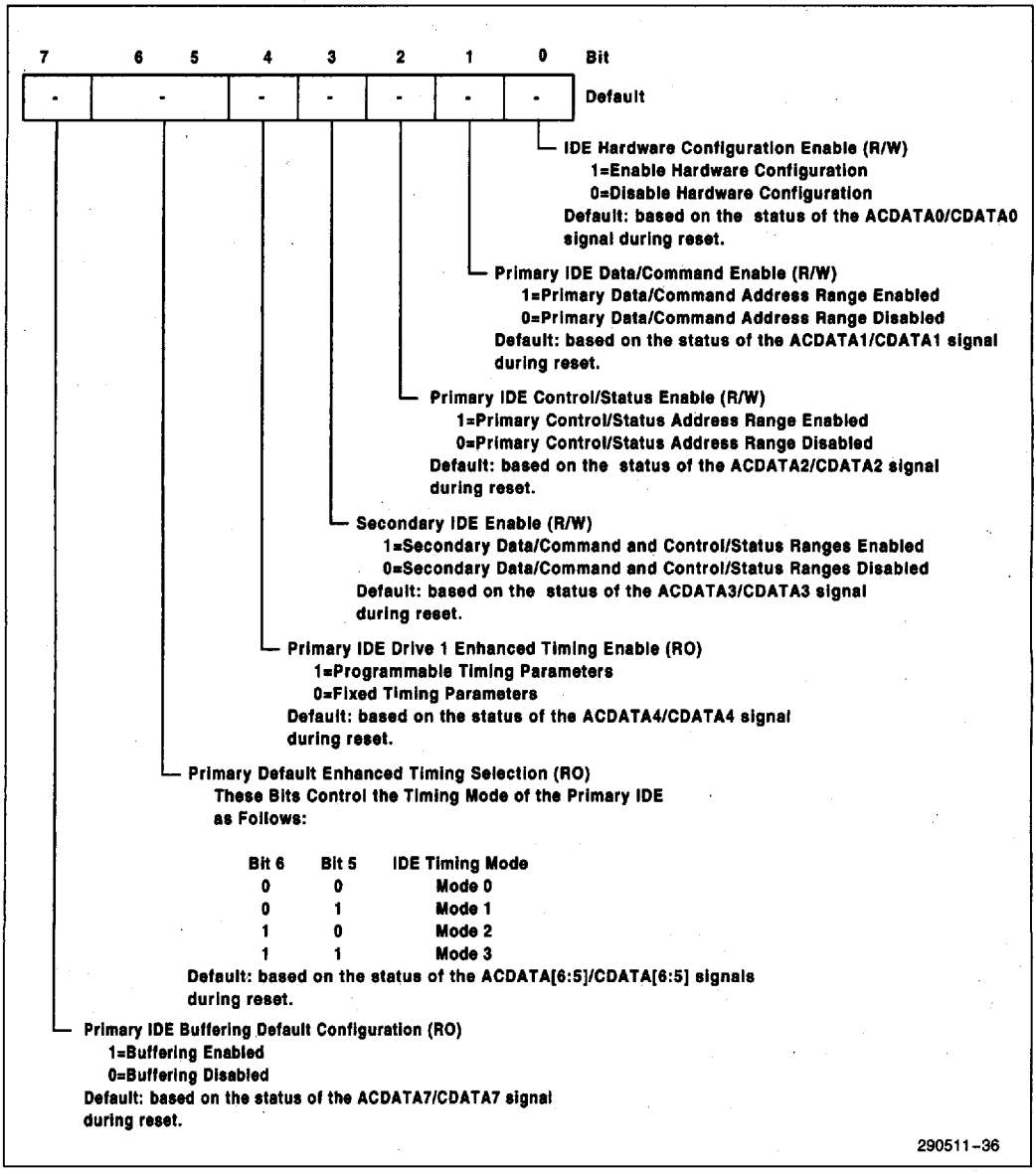


Figure 18. Power-On IDE Configuration Control Register

Bit 7: Primary IDE Buffering Default Configuration
This bit enables IDE data port buffering when set to 1 at the end of the reset sequence if ACDATA0 is externally pulled high, and disables IDE data port buffering when set to 0. If ACDATA0 is externally pulled low at the end of the reset sequence, this bit is not used to configure the IDE interface. After reset, this bit indicates the state of the ACDATA7/ CDATA7 signal at the end of the reset sequence.

Bits[6:5]: Primary Default Enhanced Timing Selection
These bits control the timing mode of the primary IDE interface at the end of the reset sequence if ACDATA0 is externally pulled high, as follows:

Bit 6	Bit 5	IDE Mode Timing
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

If ACDATA0 is externally pulled low at the end of the reset sequence, these bits are not used to configure the IDE interface. After reset, these bits indicate the states of the ACDATA[6:5]/CDATA[6:5] signals at the end of the reset sequence.

Note that these bits directly define the timing mode for Primary IDE drive 0, and that the same timing is applied to the Primary IDE drive 1 if bit 4 of this register is set to 1.

Bit 4: Primary Drive #1 Enhanced Timing Enable
When this bit is set to 1 at the end of the reset sequence with ACDATA0 externally pulled high, primary drive #1 data port timing is based on programmable timing parameters. When the bit is set to 0 at the end of the reset sequence, the timing is fixed, Mode 0 compatible timing. If ACDATA0 is externally pulled low at the end of the reset sequence, this bit is not used to configure the IDE interface. After reset, this bit indicates the state of the ACDATA4/ CDATA4 signal at the end of the reset sequence.

Bit 3: Secondary IDE Enable
When this bit is 0, all Secondary IDE registers are disabled regardless of whether they are selected from the preset compatible range (170-177h, 376h), or IDE Base Address #2 and #3. When this bit is 1, the Secondary IDE registers are enabled. The default value of this bit is 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA3 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

Bit 2: Primary IDE Control/Status Enable
When this bit is 0, the Primary IDE Control/Status register is disabled regardless of whether it is selected from the preset compatible range (3F6h), or IDE Base Address #1. When this bit is 1, the Primary IDE Data/ Command register is enabled. The default value of this bit is 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA2 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

Bit 1: Primary IDE Data/Command Enable
When this bit 0, the Primary IDE Data/Command registers are disabled regardless of whether they are selected from the preset compatible range (1F0-1F7h), or IDE Base Address #0. When this bit is 1, the Primary IDE Data/Command registers are enabled. This bit defaults to 0 if IDE Hardware Configuration is disabled (bit 0 is sampled low). The default value is the value of ACDATA1 sampled at the end of the reset sequence if IDE Hardware Configuration is enabled (bit 0 is sampled high).

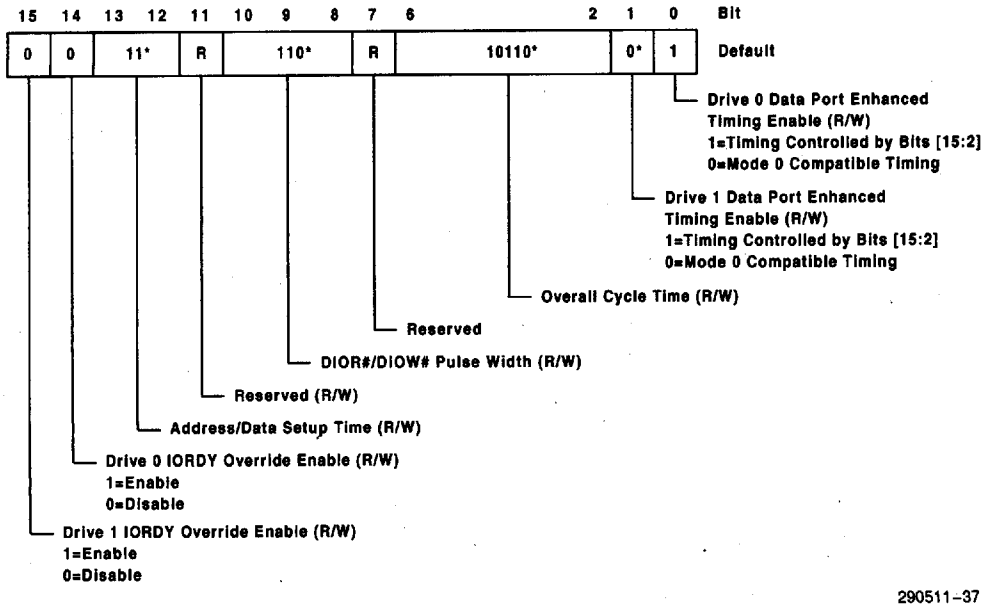
Bit 0: IDE Hardware Configuration Enable
The default value of this bit is determined by the value of the ACDATA0 signal at reset. If ACDATA0 is sampled high at the end of the reset sequence, the default values of hardware configuration bits[7:1] are determined by the values of ACDATA[7:1], the fixed IDE compatible ranges are selected (subject to enable bits[3:1]), and PCI-IDE space defaults to enabled. If ACDATA0 is sampled low, hardware configuration bits[7:1] default to 0, the IDE Base Address registers are selected (subject to enable bits[3:1]), and PCI-IDE I/O space defaults to disabled. A software write to this bit selects between IDE compatible ranges (1) and IDE Base Address registers (0), but does not affect the PCI-IDE I/O space enable.

NOTE:
The Secondary IDE timing and Data Buffering control are not IDE Hardware configurable. They default to the slowest timing mode (Mode 0), and data buffering disabled.

3.1.2.17 PIDETC—Primary IDE Timing Control

Register Offset:	48h
Default value:	xxxxh
Access:	Read/Write
Size:	16 bits

This register determines the timing characteristics and IORDY control of the Primary IDE interface.



NOTE:
See bit description.

Figure 19. Primary IDE Timing Control Register

Bit 15: Drive #1 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for Primary Drive 1 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of primary IDE drive #1 accesses.

Bit 14: Drive #0 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for Primary Drive 0 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of primary IDE drive #0 accesses.

Bits[13:12]: Address/Data Setup Time
These bits define, in system clock (PCICLK) periods, the address/data setup time with respect to the write/read strobes. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 11 = Mode 0.

Bit 11: Reserved

Bits[10:8]: DIOR#/DIOW# Pulse Width
These bits define the width of the Write and Read strobes in system clock (PCICLK) periods. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 110 = Mode 0.

Bit 7: Reserved

Bits[6:2]: Overall Cycle Time
Defines the length of the IDE cycle in system clock (PCICLK) periods. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bits correspond to the IDE timing mode selected by bits[6:5] of the PIDECFG Register. If IDE hardware is not enabled, the default is 10110 = Mode 0.

Bit 1: Drive #1 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Primary Drive 0 access timing is controlled by bits[15:2] of this register. Accesses to other ports is based on compatible timing as defined by Mode 0 in the ATA specification. If IDE hardware configuration is enabled by bit 0 of the Power-On IDE Configuration Register (PIDECFG), the default value of the bit is the value of bit 4 of the PIDECFG Register. If IDE hardware configuration is not enabled, the default is 0. When this bit is set to 0, accesses is based on compatible Mode #0 timing.

Bit 0: Drive #0 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Primary Drive 0 access timing is controlled by bits[15:2] of this register. Accesses to other ports is based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses are based on compatible Mode #0 timing. The default value for this bit is 1.

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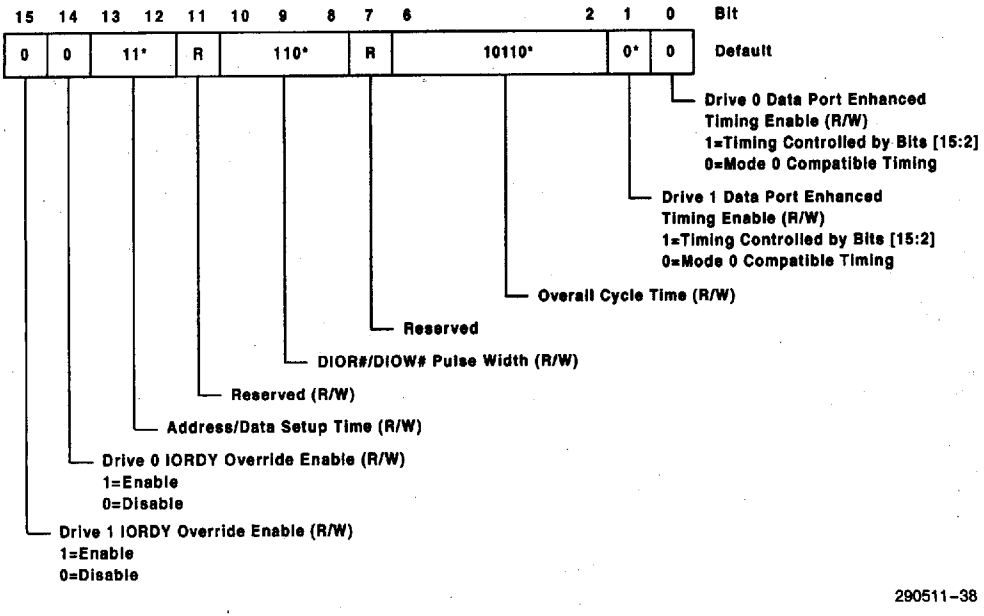
3.1.2.18 SIDETC—Secondary IDE Timing Control

Register Offset:	4Ah
Default value:	3658h
Access:	Read/Write
Size:	16 bits

This register determines the timing characteristics and IORDY control of the Secondary IDE interface.



NOTES:
See bit description.

Figure 20. Secondary IDE Timing Control Register

Bits 15: Drive #1 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for IDE Secondary Drive 1 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of Secondary IDE drive #1 accesses.

Bit 14: Drive #0 IORDY Override Enable
When this bit is set to 1, the external IORDY signal is overridden for IDE Secondary Drive 0 (i.e., the IORDY signal is asserted internally regardless of the state of the external IORDY signal). When this bit is 0, the external IORDY signal is used to control completion of Secondary IDE drive #0 accesses.

Bits[13:12]: Address/Data Setup Time
These bits define, in system clock (PCICLK) periods, the address/data setup time with respect to the write/read strobes.

Bit 11: Reserved

Bits[10:8]: DIOR#/DIOW# Pulse Width.
These bits define the width of the Write and Read strobes in system clock (PCICLK) periods.

Bit 7: Reserved

Bits[6:2]: Overall Cycle Time
These bits define the length of the IDE cycle in system clock (PCICLK) periods.

Bit 1: Drive #1 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Secondary Drive 1 data port access timing is controlled by bits[15:2] of this register. Accesses to other ports are based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses to IDE ports when Drive 0 is active is based on compatible Mode #0 timing.

Bit 0: Drive #0 Data Port Enhanced Timing Enable
When this bit is set to 1, IDE Secondary Drive 0 data port access timing is controlled by bits[15:2] of this register. Accesses to other ports are based on compatible timing as defined by Mode 0 in the ATA specification. When this bit is set to 0, accesses to IDE ports when Drive 0 is active is based on compatible Mode #0 timing.

NOTE:
The Secondary IDE timing mode is not IDE Hardware configurable. It defaults to Mode 0, the slowest timing mode.

3.1.2.19 IIIRR—IDE-ISA Interrupt Routing Register

Register Offset:	4Ch
Default Value:	XXh
Access:	Read/Write
Size:	8 bits

This register selects mapping of the Primary and Secondary IDE Interface interrupt requests to any of 10 ISA-compatible system interrupts.

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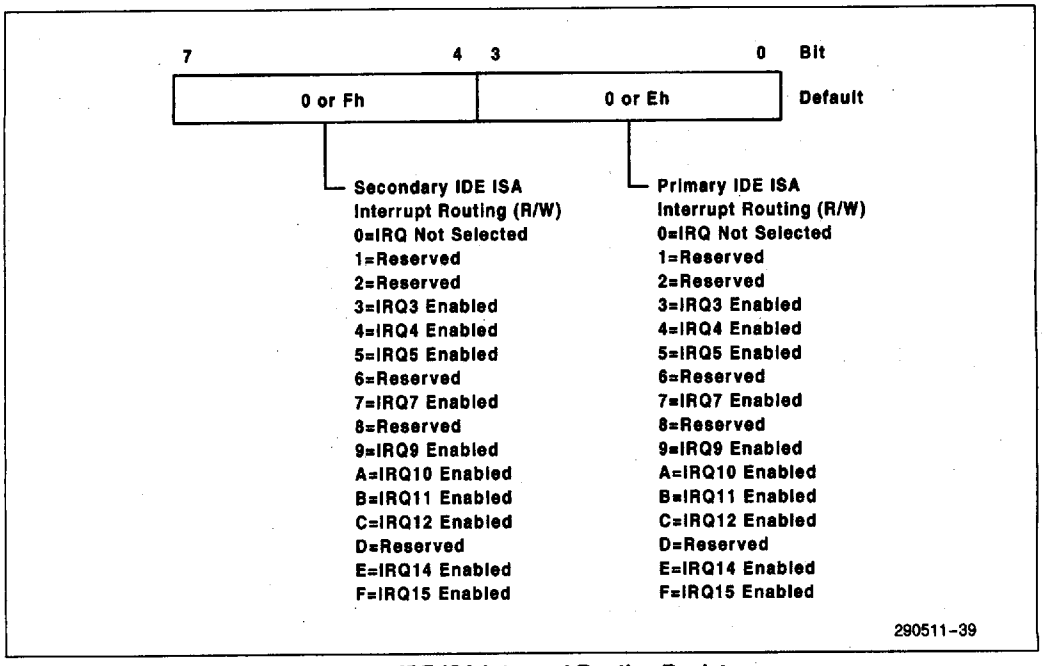

Figure 21. IDE-ISA Interrupt Routing Register

Bits[7:4]: Secondary IDE ISA Interrupt Mapping
This field selects the IRQ level for the Secondary IDE Interface. The default for this field is 0 if IDE Hardware Configuration is disabled (bit 0=0) in the Power-On IDE Configuration Control Register (PIDECFG). The default is Fh if IDE Hardware Configuration is enabled (bit 0=1) and the Secondary address range is enabled.

Bits[3:0]: Primary IDE ISA Interrupt Mapping
This field selects the IRQ level for the Primary IDE Interface. The default for this field is 0 if IDE Hardware Configuration is disabled (bit 0=0) in the Power-On IDE Configuration Control Register (PIDECFG). The default is Eh if IDE Hardware Configuration is enabled (bit 0=1) and the Primary Data/Command address range is enabled.

3.1.2.20 IDEICS—IDE Interrupt Configuration/ Status Register

Register Offset: 4Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows selection of edge or level mode for Primary and Secondary interrupts selected via the IIIRR Register, and provides non-latched read-only status of the physical PIRQ and SIRQ signal pins.

Bits[7:4]: Reserved

Bit 3: Secondary IDE System Interrupt Operation Mode
This bit provides the IRQ operation mode for the system interrupt signal selected to be used as a Secondary IDE Interrupt via the IIIRR Register as follows:

1=Level Mode Selected
0=Edge Mode Selected

Bit 2: Primary IDE System Interrupt Operation Mode
This bit provides the IRQ operation mode for the system interrupt signal selected to be used as a Primary IDE Interrupt via the IIIRR Register as follows:

1=Level Mode Selected
0=Edge Mode Selected

Bit 1: Secondary IDE Interrupt Status
This bit provides the status of the SIRQ Secondary IRQ signal as follows:

1=Secondary IDE IRQ active
0=Secondary IDE IRQ inactive

Bit 0: Primary IDE Interrupt Status
This bit provides the status of the SIRQ Primary IRQ signal as follows:

1=Primary IDE IRQ active
0=Primary IDE IRQ inactive

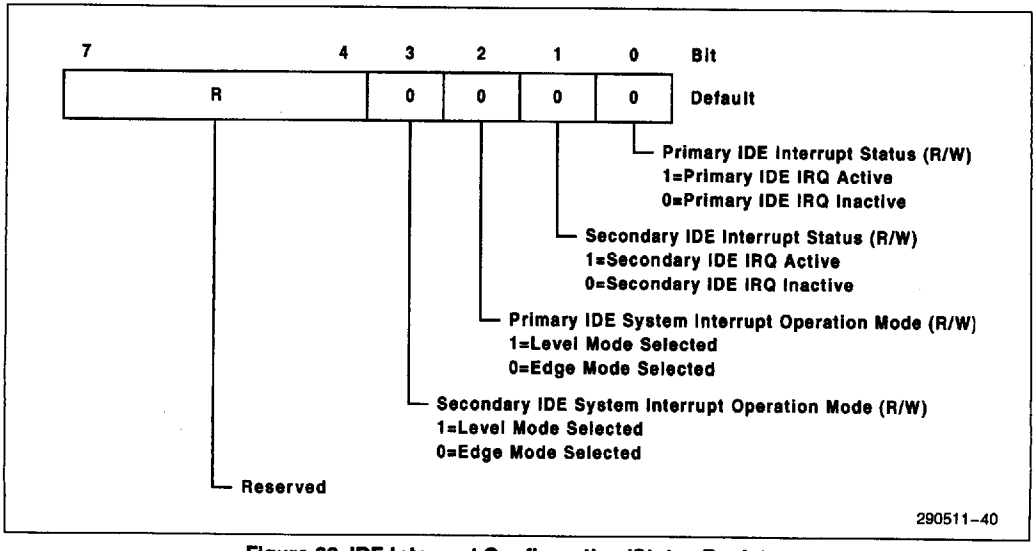

Figure 22. IDE Interrupt Configuration/Status Register

3.1.2.21 PCIRR—IDE-PCI Interrupt Routing Register

Register Offset: 50h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register allows mapping of IDE interrupts to either ISA interrupts, or PCI interrupts. One interrupt can be generated for the primary IDE interface, and another for the secondary IDE interface. Each of the interrupts can be routed independently. When bit 0 or 1 is set to 0, the corresponding interrupt is routed via one of 10 system interrupt lines (ISA mechanism) selected by the IDE ISA Interrupt Mapping Register. When set to 1, the corresponding interrupt is routed via INTB# (PCI mechanism).

Bits[7:2]: Reserved

Bit 1: Secondary IDE Interrupt Routing
This bit selects Secondary IDE Interface Interrupt routing via the PCI mechanism, or the ISA mechanism.

Bit 0: Primary IDE Interrupt Routing
This bit selects Primary IDE Interface Interrupt routing via the PCI mechanism, or the ISA mechanism.

3.2 PCMCIA Socket Configuration Registers

The PPEC has four identical sets of registers for controlling the four PCMCIA sockets, with each set controlling one socket. Each register set is comprised of four types of registers: General Setup Registers, Interrupt Registers, I/O Mapping Control Registers, and Memory Mapping Control Registers. One set of registers is described in the following sections, with the address offset for each socket shown in each description.

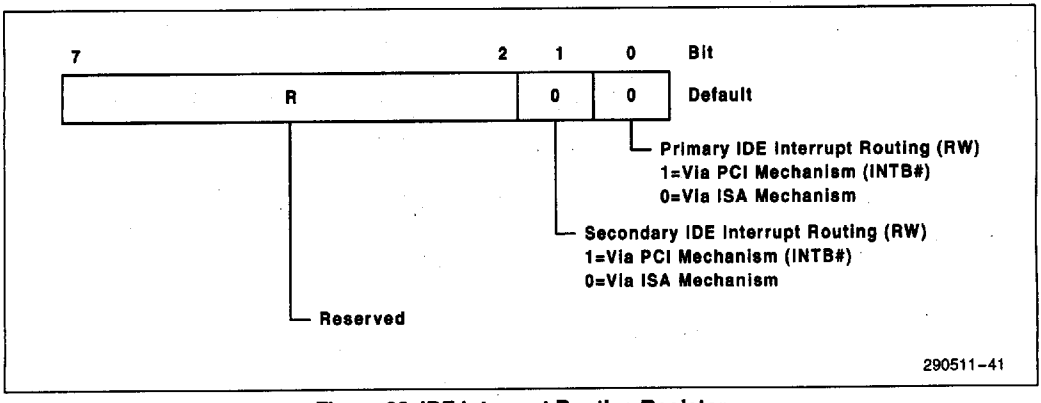

Figure 23. IDE Interrupt Routing Register

3.2.1 GENERAL SETUP REGISTERS

The General Setup Registers, listed in Table 8, are 8-bit registers. Writes to Read Only General Setup registers and register bits have no effect.

Table 8. General Setup Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
00	40	80	C0	IDREG	Identification	RO
01	41	81	C1	ISTAT	Interface Status	RO
02	42	82	C2	PCTRL	Power Control	R/W
04	44	84	C4	CSTCH	Card Status Change	R/W
06	46	86	C6	ADWEN	Address Window Enable	R/W
1E	5E	9E	DE	GCTRL	Global Control	R/W
2E	6E	AE	EE	CSCTRL	Global Security Control	R/W
16	56	96	D6	CDGEN	Card Detect and General Control	R/W
26	66	A6	E6	CPAGE	Card Memory Page	R/W

3.2.1.1 IDREG—Identification Register

Register Offset: Socket A—00h
Socket B—40h
Socket C—80h
Socket D—C0h
Default value: 84h
Access: Read/Write
Size: 8 bits

The Identification Register is used by the system software to determine the type of PC Cards supported by the socket.

Bits[7:6]: Interface Type
These bits indicate the type of PC Cards supported by the PPEC at the particular socket as follows:

00 = I/O Only
01 = Memory Only
10 = Memory and I/O
11 = Reserved

These bits do not identify the type of card that is present at the socket.

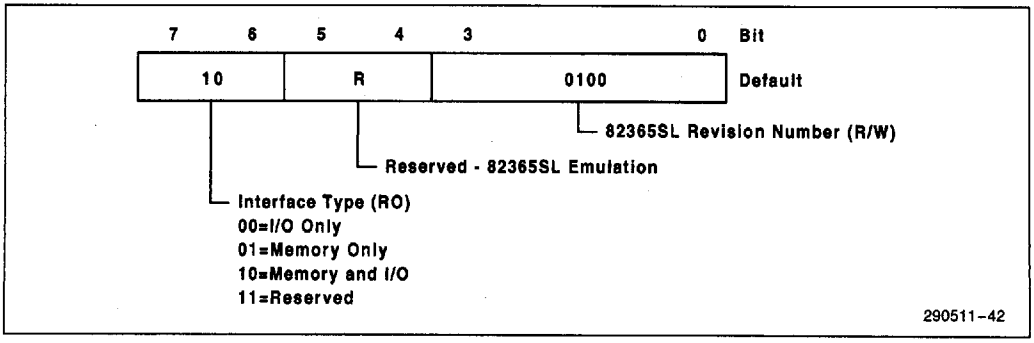

Figure 24. Identification Register

Bits[5:4]: Reserved
These are read/write bits that can be used to store 82365SL-specific information to allow 82365SL emulation.

Bits[3:0]: Reserved—82365SL Revision Information
This read/write field holds 82365SL revision information that allows the PPEC to emulate the 82365SL. Software checks this field before executing code written for the 82365SL.

3.2.1.2 ISTAT—Interface Status Register

Register Offset:	Socket A—01h Socket B—41h Socket C—81h Socket D—C1h
Default value:	XX
Access:	Read-only
Size:	8 bits

The Interface Status Register provides the current status of the PC Card socket interface signals.

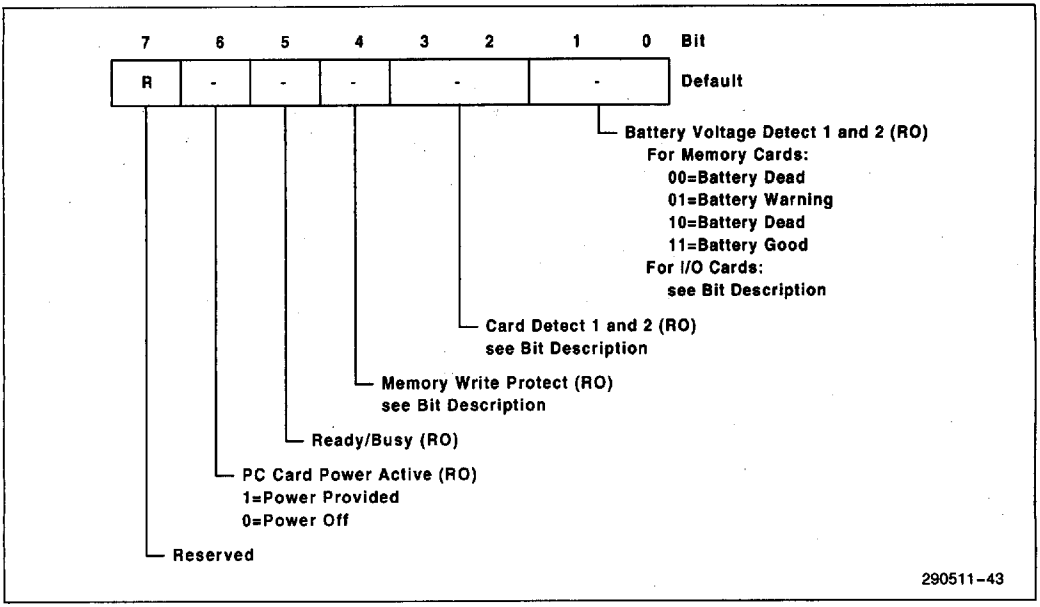

Figure 25. Interface Status Register

Bit 7: Reserved

Bit 6: PC Card Power Active
Indicates the current power status of the socket. If this bit is set to zero, power to the socket is turned off (V_{CC} and V_{PP} are not applied). If the bit is set to one, power is applied to the socket (V_{CC} is applied according to bits[4:3] of the Power Control Register, and V_{PP} is applied according to bits[1:0] of the Power Control Register).

Bit 5: Ready/Busy#
This bit is set to 1 to indicate that the PC Card is ready to accept a data transfer, and set to 0 to indicate that the card is busy completing an operation and cannot accept new data or commands.

Bit 4: Memory Write Protect
This bit indicates the logic level of the WP signal on the memory PC Card interface. However, memory write access to the socket is blocked only if the write protect bit in the associated Card Memory Offset Address Register High byte register is set to one.

Bits[3:2]: Card Detect 1 and 2
These bits indicate, when both are set to 1, that a card is present at the socket and is fully seated. Bit 2 is set to 1 if the CD1 signal on the PC Card interface is active, and bit 3 is set to 1 if the CD2 signal is active. Bits 2 and 3 are set to 0 if the corresponding CD1 and CD2 signals on the PC Card interface are inactive.

Bits[1:0]: Battery Voltage Detect 1 and 2
For memory cards, these bits indicate the status of the battery as follows:

BVD1	BVD2	Status
0	0	Battery Dead
0	1	Battery Dead
1	0	Warning
1	1	Battery Good

For I/O PC Cards, bit 0 indicates the current status of the STSCHG signal from the PC Card. For I/O PC Cards, bit 1 indicates the current state of SPKR signal from the PC Card. Refer to the Interrupt General Control Register bit 7 description for more details.

3.2.1.3 PCTRL—Power Control Register

Register Offset: Socket A—02h
Socket B—42h
Socket C—82h
Socket D—C2h
Default value: xx
Access: Read/Write
Size: 8 bits

This register controls power to the PC card. PCIRST# (PCI reset) clears all bits in this register. Output Enable should not be set until the register has been previously written setting the socket V_{PP} and V_{CC} Power Control bits.

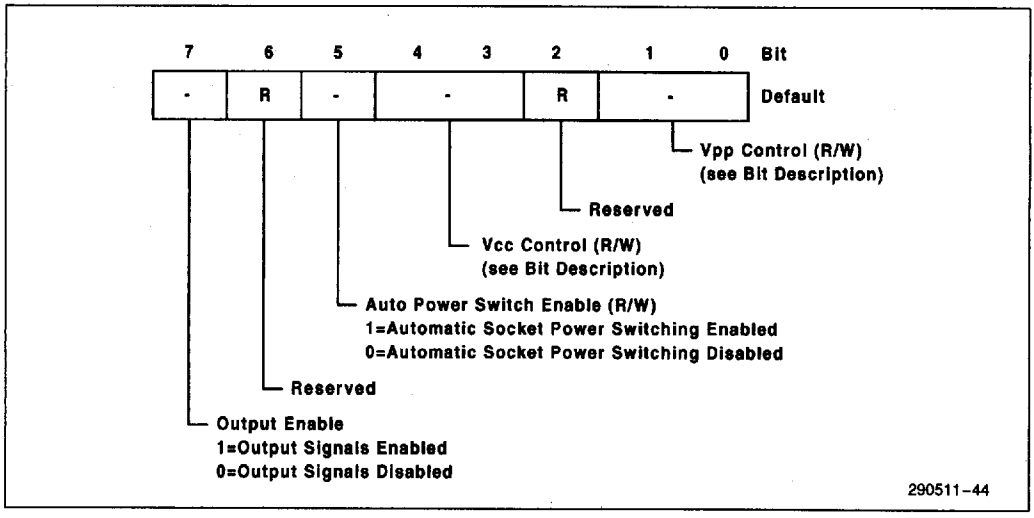

Figure 26. Power Control Register

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Bit 7: Output Enable
When this bit is set to 0, the PPEC output signals that are directly connected to the socket (Mode 0) or are shared by other sockets (Mode 1) are tri-stated, and the ENABLE# signal to the socket is inactive. When the bit is set to 1, the signals are not tri-stated, and the ENABLE# signal is asserted. Output Enable should be set to 0 when the socket is not powered.

Bit 6: Reserved

Bit 5: Auto Power Switch Enable
When this bit is set to 0, automatic socket power switching based on card detects is disabled. When the bit is set to 1, automatic socket power switching is enabled. Automatic socket power switching function controls the V_{CC}xV and V_{PP}ENx power control bits. V_{CC} is 5V or 3.3V depending on the sampled states of the VS1 and VS2 signals provided in the Card Detect and General Control Register.

Bits[4:3]: V_{CC} Control
These bits control the power to the PC Card via the external V_{CC}-3V and V_{CC}-5V control logic (External Power Latch). The two bits are encoded as follows:

Bit 4	Bit 3	V_{CC}5V	V_{CC}3V	Description
0	0	0	0	No Connect
0	1	0	0	Reserved
1	0	1	0	5.0V
1	1	0	1	3.3V

Bit 2: Reserved

Bits[1:0]: V_{PP} Control
These bits switch V_{PP} power using the external Vpp control logic (External Power Latch). The two bits are encoded together with bit 4 to implement the following control functions:

Bit 4	Bit 1	Bit 0	V_{PP} EN1	V_{PP} EN0	Applied Voltage
1	0	0	0	0	No Connect
1	0	1	0	1	5.0V
1	1	0	1	0	12.0V
1	1	1	0	0	Reserved
0	x	x	0	0	No Connect

For more details on V_{CC}/V_{PP} control functions, see the Power Control description in Section 1.4.2 of this document.

3.2.1.4 CSTCH—Card Status Change Register

Register Offset: Socket A—04h
Socket B—44h
Socket C—84h
Socket D—C4h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register contains the status of the sources for the Card Status Change Interrupts. These sources can be enabled to generate a Card Status Change Interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register. The bits in this register read back as 0 when the corresponding status enable bits in the Card Status Change Interrupt Configuration Register are set to 0.

When the Explicit Write Back Card Status Change Acknowledge bit is set in the Global Control Register, the acknowledgment of sources for the Card Status Change Interrupt is performed by writing back 1 to the appropriate bit in the Card Status Change Register that was read as a 1. Once the interrupt source is acknowledged by writing a 1 to the bit, the bit reads back as 0. The interrupt signal responding to the card status change remains active, if enabled on a system IRQ line, until all of the bits in this register are zero.

When the Explicit Write Back Card Status Acknowledge bit is not set, the Card Status Change Interrupt remains active, if enabled on a system IRQ line, until the Card Status Change Register is read. The read operation to the Card Status Change Register resets all bits in the register.

If two or more Card Status Change Interrupts are pending or a Card Status Change Interrupt condition occurs while another is being serviced, the PPEC does not generate a second interrupt.

The Interrupt Service Routine must read the Card Status Change Register to ensure that all interrupt requests are serviced before exiting the service routines.

Asserted PCIRST# (PCI reset) clears all bits in this register.

In the following bit descriptions, bits names that are in parenthesis are valid when the interface is configured for I/O PC Cards.

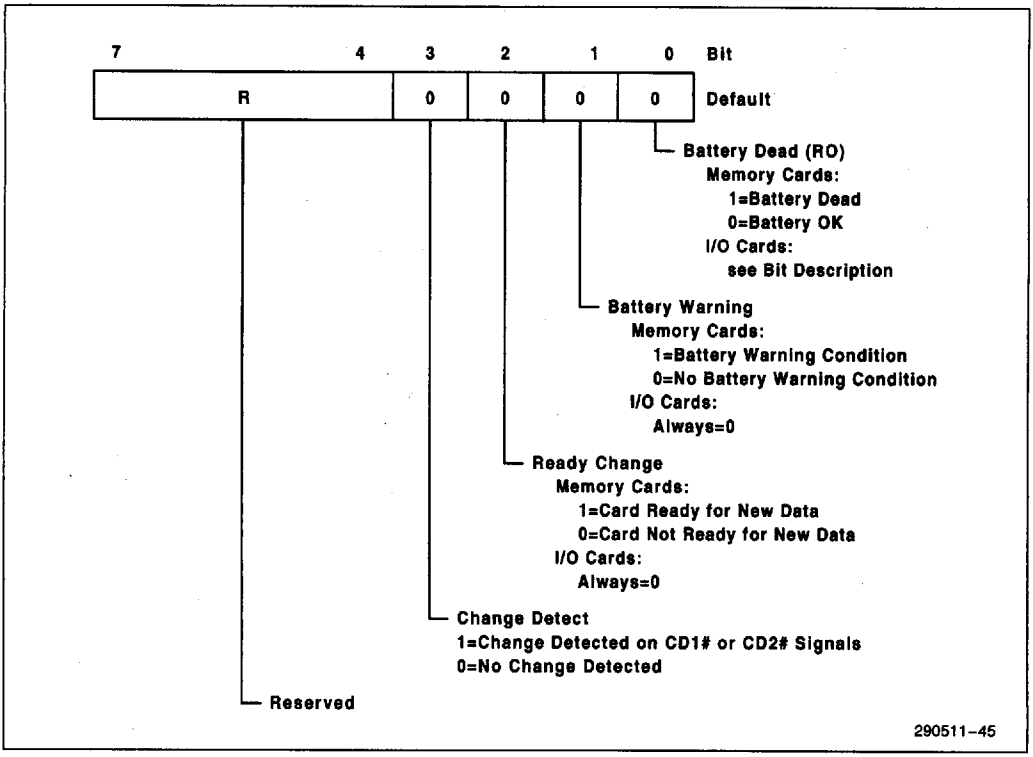

Figure 27. Card Status Change Register

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Bits[7:4]: Reserved

Bit 3: Change Detect
This bit is set to 1 when a change occurs in either the CD1# or CD2# signal, or when a Software Interrupt is generated.

Bit 2: Ready Change
This bit is set to 1 when a low-to-high transition occurs on the RDY-BSY# signal, indicating that the memory PC Card is ready to accept a new data transfer. The bit reads 0 for I/O PC Cards.

Bit 1: Battery Warning
This bit is set to 1 when a battery warning condition is detected. The bit reads 0 for I/O PC Cards.

Bit 0: Battery Dead
For memory PC Cards, this bit is set to 1 when a battery dead condition has been detected. For I/O PC Cards, it is set to 1 when the STSCHG# signal from the I/O PC Card has been asserted low. The system software must then read the status change register in the PC Card to determine why the status change signal (STSCHG#) has been asserted.

3.2.1.5 ADWEN—Address Window Enable Register

Register Offset:	Socket A—06h Socket B—46h Socket C—86h Socket D—C6h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register controls enabling of the memory and I/O mapping windows to the PC Card memory or I/O space. All bits in this register are cleared after reset.

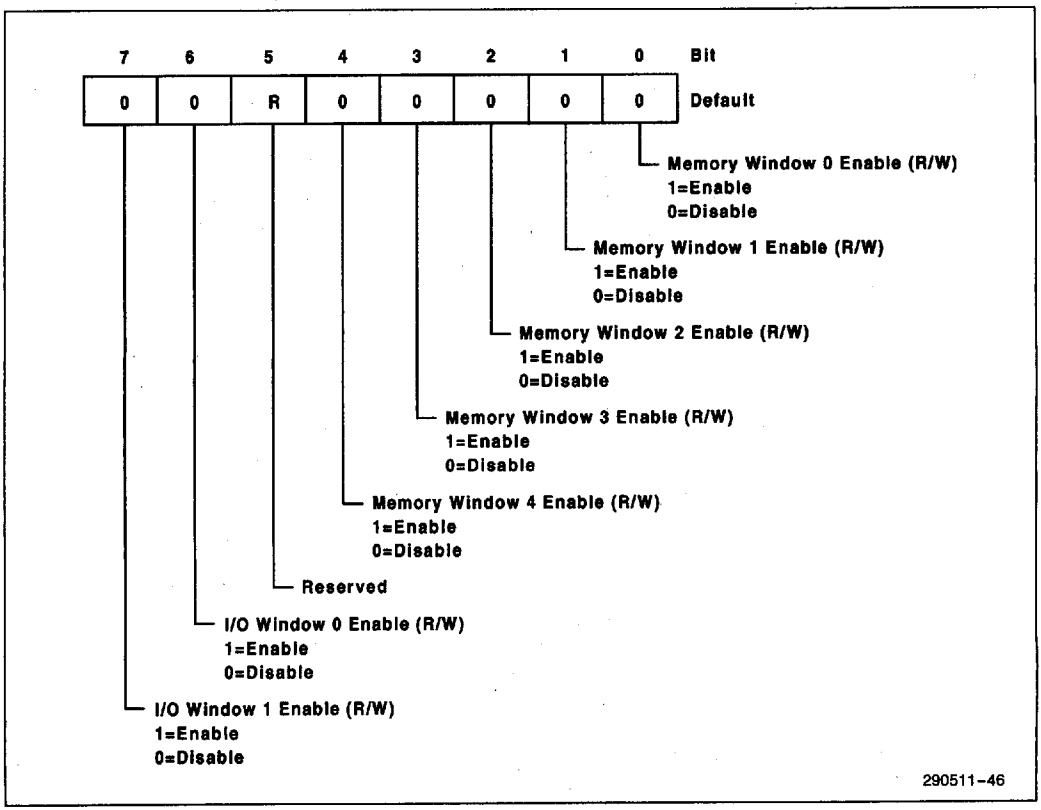

Figure 28. Address Window Enable Register

Bit 7–Bit 6: I/O Window 1 and Window 0 Enables
Bits[7:6] function identically and independently. Bit 7 applies to I/O Window 1; Bit 6 applies to I/O Window 0. When the bits are set to 0, the card enable signals to the PC cards that are accessed through the corresponding I/O windows are inhibited. When set to one, the card enable signals are not inhibited. I/O accesses pass addresses from the system bus directly through to the PC cards. The corresponding Start and Stop register pairs must all be set to the desired window values before setting either of the bits to one.

Bit 5: Reserved

Bit 4–Bit 0: Memory Window 4 - Memory Window 0 Enables
Bits[4:0] function identically and independently. Bit 4 applies to Memory Window 4, bit 3 applies to Memory Window 3, etc. When the bits are set to 0, the card enable signals to PC cards that are accessed through the corresponding memory windows are inhibited. When set to one, the card enable signals are not inhibited. The corresponding start, stop, and offset register pairs must all be set to the desired window values before setting any of the bits to 1. When one of the bits is set to 1 and the system address is within the corresponding window, the computed address will be generated for the accessed PC Card.

3.2.1.6 GCTRL—Global Control Register

Register Offset:	Socket A—1Eh
	Socket B—5Eh
	Socket C—9Eh
	Socket D—DEh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is not duplicated for each socket, but can be accessed with the Socket A, B, C or D index. PCI reset clears all bits in this register.

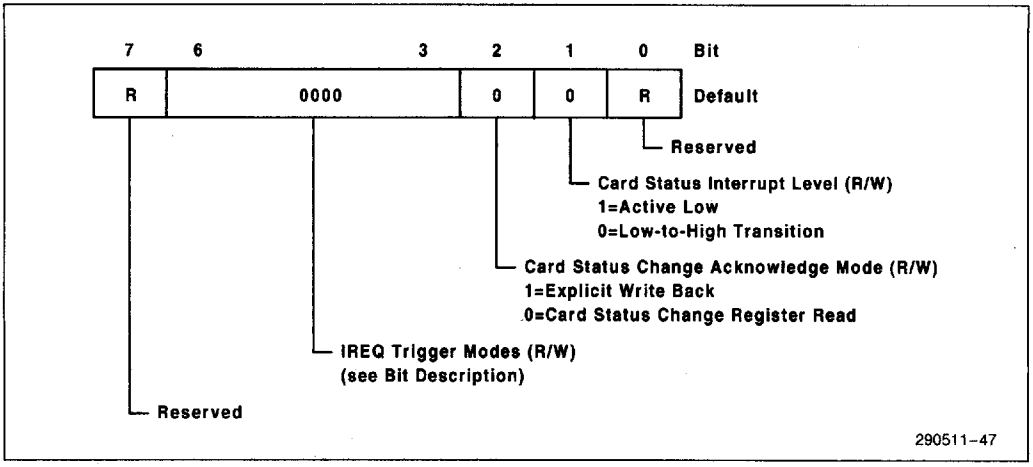

Figure 29. Global Control Register

Bit 7: Reserved

Bits[6:3]: IREQ Trigger Modes
When set to 1, these bits select level mode interrupts for IRQs generated by the particular PC card interrupts. When set to 0 (default), they select edge mode interrupts. Bit 3 is used for Socket A, Bit 4 for Socket B, Bit 5 for Socket C, and Bit 6 for Socket D

Bit 2: Card Status Change Acknowledge Mode
When this bit is set to 1, each Card Status Change Interrupt is acknowledged with an explicit write of 1 to the Card Status Change Register bit that identifies the interrupt. When this bit is set to 0 (default state), each Card Status Change Interrupt is acknowledged by reading the Card Status Change Register. Reading the Card Status Change Register clears the register.

Bit 1: Card Status Interrupt Level
When this bit is set to 1, the mode of the IRQ outputs used to signal the Card Status Change (CSC) Interrupt is active low level. In this mode, the IRQs remain tri-stated until there is a card status change condition, at which time the asserted IRQ output goes low. The IRQ remains low until the interrupt is acknowledged (serviced). Once serviced, the IRQ output will change from low to tri-state.

When this bit is set to its default state of 0, the CSC IRQ outputs are low-to-high edge triggered interrupts. In this mode, the IRQ signals remain tri-stated until enabled for CSC interrupt, at which time the IRQ outputs are asserted low. The outputs stay low until there is a card status change condition, which causes the appropriate IRQ output to transition to the high level. It will remain high until the interrupt is acknowledged (serviced), then transitions to the low state. When disabled, the IRQ signals are tri-stated.

Bit 0: Reserved

3.2.1.7 GSCTRL—Global Security Control Register

Register Offset:	Socket A—2Eh
	Socket B—6Eh
	Socket C—AEh
	Socket D—EEh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is not duplicated for each socket, but can be accessed with the Socket A, B, C or D index. PCI reset clears all bits in this register.

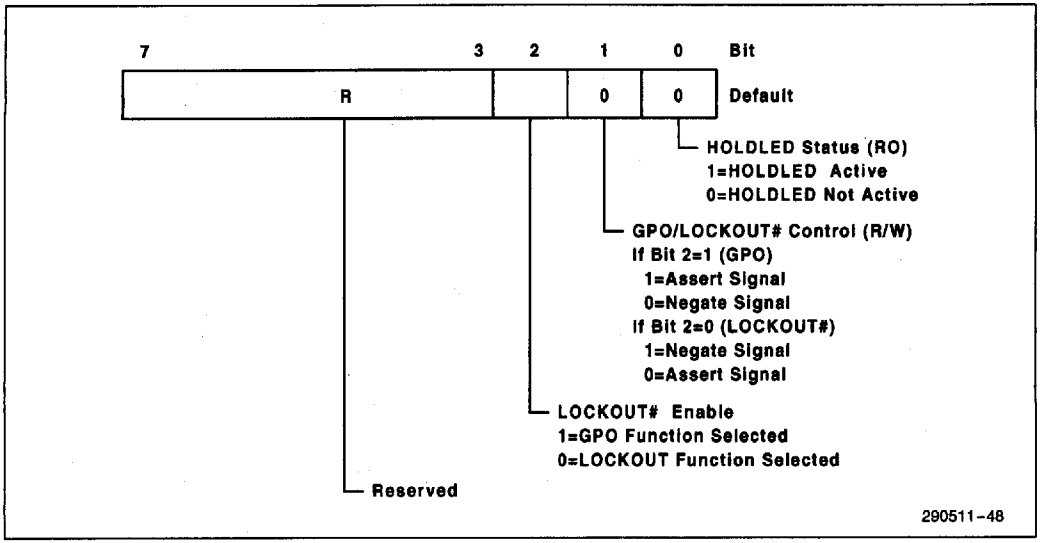

Figure 30. Global Security Control Register

Bits[7:3]: Reserved

Bit 2: Lockout# Enable
This bit configures bit 1 to function as GPO control when set to 1, and as LOCKOUT# control when set to 0.

Bit 1: General Purpose Output Control
When bit 2 is set to 1, this bit allows software control of the General Purpose Output control signal. When bit 2 is set to 0, this bit allows software control of the LOCKOUT# output signal. When bit 2 is 0 (LOCKOUT function) and this bit is 0, the LOCKOUT# signal is asserted, and the xCD2# signals function as "eject request". When bit 2 is 0 and this bit is 1, LOCKOUT# is negated, and the xCD2# signals retain their original function as Card Detect signals. See the PPEC Design Guide for details.

Bit 0: HOLDLED Status
This bit provides the status of the HOLDLED# output signal (pin), and is valid only in Mode 1.

3.2.1.8 CDGEN—Card Detect and General Control Register

Register Offset:	Socket A—16h
	Socket B—56h
	Socket C—96h
	Socket D—D6h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register is used to reset configuration registers and store voltage select signal status. It is necessary that the Configuration Reset Enable bit is set to 1 by the card detect change interrupt service routine only when a PC Card is inserted, and set to 0 when the card is removed.

Bit 7: VS2 Voltage Select Status
This bit indicates the status of the VS2 multifunctional signal, which is used with VS1 to select proper V_{CC} voltage (5V or 3.3V or disable) at a socket.

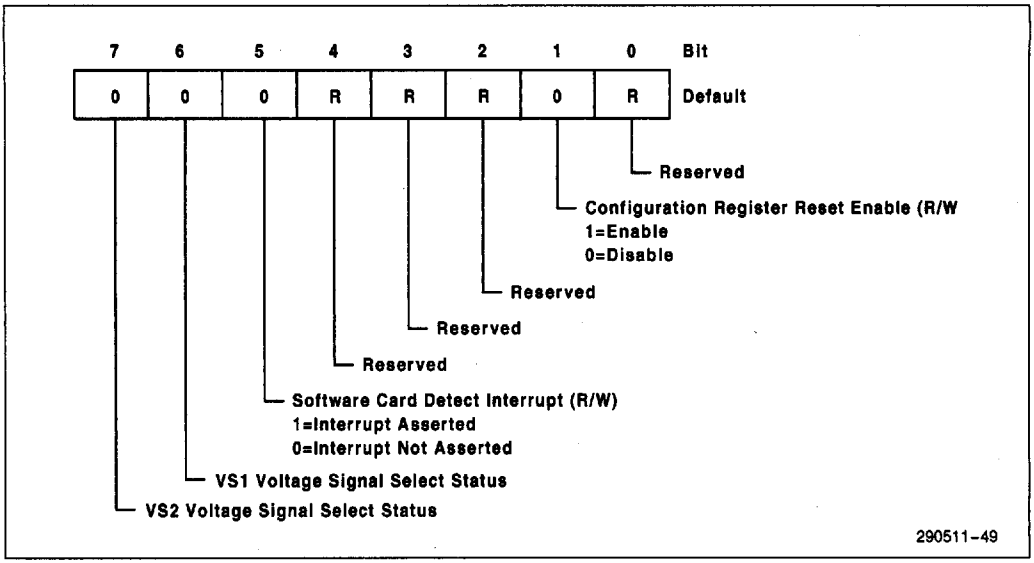

Figure 31. Card Detect and General Control Register

Bit 6: VS1 Voltage Select Status
This bit indicates the status of the VS1 voltage select signal, which is used to select proper V_{CC} voltage (5V or 3.3V or disable) at a socket.

Bit 5: Software Card Detect Interrupt
Setting this bit to 1 causes a Card Detect Card Status Change Interrupt for the associated socket if the Card Detect Enable bit is set to 1 in the Card Status Change Interrupt Configuration Register. The software interrupt functions and is acknowledged in the same manner as the hardware-generated interrupt.

The Hardware Card Detect Card Status Change Interrupt is not affected by the Software Card Detect Interrupt. The previous state of the CD1 and CD2 inputs are latched so that though a Card Detect Card Status Change Interrupt occurs and is serviced and the CD1 and CD2 inputs change from the previous state, a Hardware Card Detect Card Status Change Interrupt is still generated. If the Card Detect Enable bit is set to 0 in the Card Status Change Interrupt Configuration Register,. writing a 1 to the Software Card Detect Interrupt bit has no effect.

The Software Card Detect Interrupt bit always reads back as a 0.

Bit 4: Reserved

Bit 3: Reserved

Bit 2: Reserved

Bit 1: Configuration Register Reset Enable
When this bit is set to 0, the configuration register reset function that is based on card detect is disabled. When it is set to 1, a reset pulse is generated to reset the configuration registers for the socket to their default state (zero's) when both the CD1 and CD2 inputs for the socket go high. There is one Configuration Register Reset Enable for each socket.

Bit 0: Reserved

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3.2.1.9 CPAGE—Card Memory Page Address Register

Register Offset: Socket A—26h
Socket B—66h
Socket C—A6h
Socket D—E6h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register holds an 8-bit page address that allows selection of a 16 MByte window page in the 4 GByte memory address space in which socket memory windows are mapped. Access to a window is allowed only when the page address in the corresponding Card Memory Page Address Register matches PCI memory address bits A[31:24], indicating a page hit. Reset clears all bits in this register, so that the default page is the first page (i.e., 0-16 MByte address range).

Bits[7:0]: Page Address
Page Address bits[7:0] correspond to system address lines A[31:24]. Access to one of the five memory windows is allowed only if a match between the page address and system address lines A[31:24] occurs.

3.2.2 INTERRUPT REGISTERS

The Interrupt Registers are listed in Table 9. The registers are 8-bit, read/write registers.

Table 9. Interrupt Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
03h	43h	83h	C3h	IGENC	Interrupt and General Control	R/W
05h	45h	85h	C5h	CSCICR	Card Status Change Interrupt Configuration	R/W

3.2.2.1 IGENC—Interrupt and General Control Register

Register Offset: Socket A—03h
Socket B—43h
Socket C—83h
Socket D—C3h
Default value: 00h
Access: Read/Write
Size: 8 bits

The Interrupt and General Control Register controls card type selection, card reset, and interrupt steering for the PC Card I/O interrupts.

Bit 7: Reserved

Bit 6: Card Reset
Setting this bit to 0 resets the PC Card by activating the RESET signal to the card. The RESET signal remains active until bit is set to 1.

Bit 5: Card Type
Setting this bit to 1 selects I/O PC Card, enabling the PC Card interface multiplexer to route PC Card I/O signals. Setting the bit to 0 selects Memory PC Card. When the bit is set to 1 (I/O PC Card), the STSCHG# signal from the I/O PC Card is used as the STSCHG status change signal. The current status of the signal is then available to be read from the Interface Status Register (01H), and the STSCHG signal can be configured as a source for the Card Status Change Interrupt.

Bit 4: Reserved

Bits[3:0]: IRQ Level Selection
This field selects interrupt routing for I/O PC Cards only.

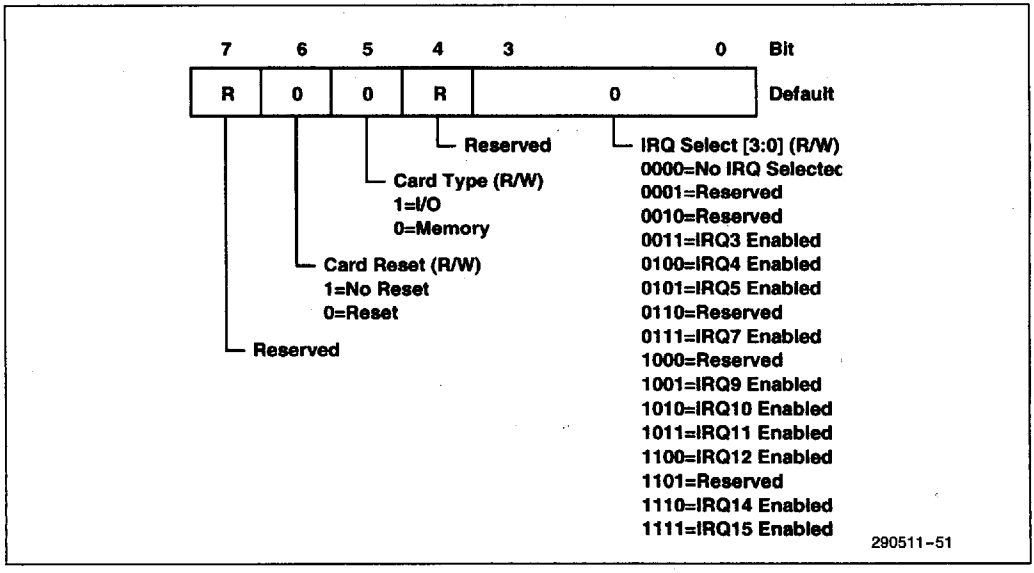

Figure 32. I/O Control Register

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3.2.2.2 CSCICR—Card Status Change Interrupt Configuration Register

Register Offset: Socket A—05h
Socket B—45h
Socket C—85h
Socket D—C5h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register controls Card Status Change Interrupt steering and the Card Status Change Interrupt enables.

Bits[7:4]: Card Status Change Interrupt Select
This field selects Card Status Change Interrupt routing.

Bit 3: Card Status Change Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a change in the CD1 or CD2 signal occurs, or when a Software Interrupt is generated by writing to bit 5 of the CDGEN register. Setting the bit to 0 disables the generation of a card status change interrupt when the CD1 or CD2 signals change state, or upon software command.

Bit 2: Ready Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a low to high transition occurs on the RDY-BSY# signal. Setting the bit to 0 disables the interrupt. The bit has no effect when the interface is configured for I/O PC Cards.

Bit 1: Battery Warning Interrupt Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a battery warning condition is detected. Setting the bit to 0 disables the interrupt.

Bit 0: Battery Dead Enable
Setting this bit to 1 enables a Card Status Change Interrupt when a battery dead condition is detected in a memory PC Card, and when the STSCHG# signal is pulled low by an I/O PC Card. Setting the bit to 0 disables the interrupt.

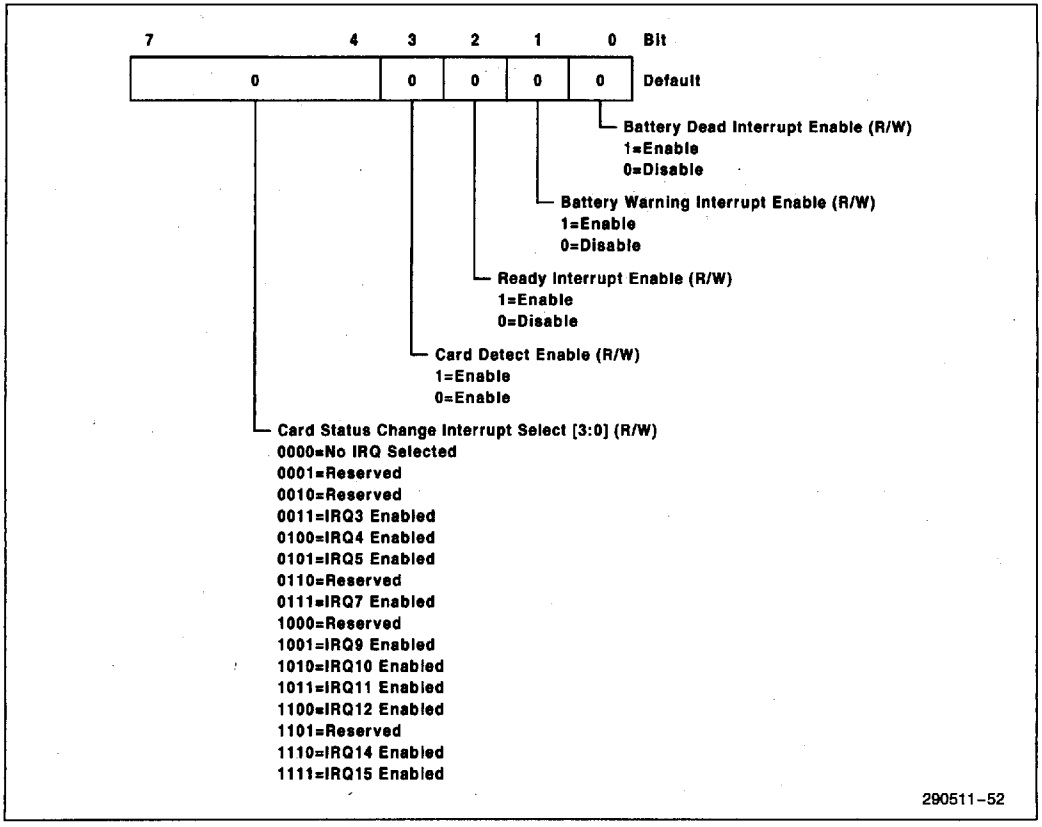

Figure 33. Card Status Change Interrupt Configuration Register

3.2.3 I/O MAPPING CONTROL REGISTERS

The I/O Mapping Control Registers are listed in Table 10. The registers are 8 bit read/write registers that specify data path sizes and start and stop addresses for the two I/O windows.

Table 10. I/O Mapping Control Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
07h	47h	87h	C7h	IOCREG	I/O Control	R/W
08h	48h	88h	C8h	IOSL0	I/O Address 0 Start Low Byte	R/W
09h	49h	89h	C9h	IOSH0	I/O Address 0 Start High Byte	R/W
0Ah	4Ah	8Ah	CAh	IOSTL0	I/O Address 0 Stop Low Byte	R/W
0Bh	4Bh	8Bh	CBh	IOSTH0	I/O Address 0 Stop High Byte	R/W
0Ch	4Ch	8Ch	CCh	IOSL1	I/O Address 1 Start Low Byte	R/W
0Dh	4Dh	8Dh	CDh	IOSH1	I/O Address 1 Start High Byte	R/W
0Eh	4Eh	8Eh	CEh	IOSTL1	I/O Address 1 Stop Low Byte	R/W
0Fh	4Fh	8Fh	CFh	IOSTH1	I/O Address 1 Stop High Byte	R/W

5

3.2.3.1 IOCREG—I/O Control Register

Register Offset: Socket A—07h
Socket B—47h
Socket C—87h
Socket D—C7h
Default value: 00h
Access: Read/Write
Size: 8 bits

This register controls the I/O data path size for I/O windows 0 and 1. In order to be compatible with some software and hardware implementations such as an IDE interface, it is necessary that the PC Card decode two consecutive I/O addresses to determine the cycle data width. To meet the system bus timings, this type of PC Card must decode address lines A[9:0] before the card enable signal becomes active at the interface. The card decodes the address and responds to a 16-bit cycle by asserting the IOIS16# signal. The PPEC qualifies IOIS16# with the card enable signals to control internal data assembly/disassembly logic.

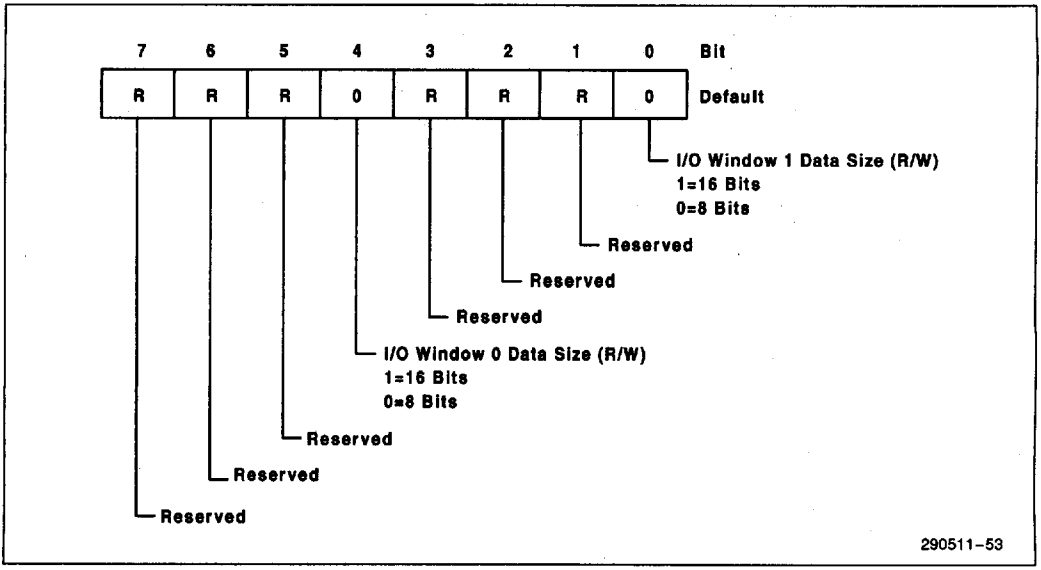

Figure 34. I/O Control Register

Bits[7:5]: Reserved

Bit 4: I/O Window 1 Data Size
This bit selects a 16-bit I/O data path to the PC Card when set to 1, and an 8-bit path when set to 0.

Bits[3:1]: Reserved

Bit 0: I/O Window 0 Data Size
This bit selects a 16-bit I/O data path to the PC Card when set to 1, and an 8-bit path when set to 0.

3.2.3.2 IOSL0—I/O Address 0 Start Low Byte Register

Register Offset:	Socket A—08h Socket B—48h Socket C—88h Socket D—C8h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Start Address Low Bytes
This field holds start address bits A[7:0] of I/O address window 0.

3.2.3.3 IOSH0—I/O Address 0 Start High Byte Register

Register Offset:	Socket A—09h Socket B—49h Socket C—89h Socket D—C9h
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the start address of I/O address window 0.

Bits[7:0]: I/O Window 0 Start Address High Bytes
This field holds start address bits A[15:8] of I/O address window 0.

3.2.3.4 IOSTL0—I/O Address 0 Stop Low Byte Register

Register Offset:	Socket A—0Ah Socket B—4Ah Socket C—8Ah Socket D—CAh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Stop Address Low Bytes
This field holds stop address bits A[7:0] of I/O address window 0.

3.2.3.5 IOSTH0—I/O Address 0 Stop High Byte Register

Register Offset:	Socket A—0Bh Socket B—4Bh Socket C—8Bh Socket D—CBh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the stop address of I/O address window 0. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 0 Stop Address High Bytes
This field holds stop address bits A[15:8] of I/O address window 0.

3.2.3.6 IOSL1—I/O Address 1 Start Low Byte Register

Register Offset:	Socket A—0Ch
	Socket B—4Ch
	Socket C—8Ch
	Socket D—CCh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 0 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Start Address Low Bytes
This field holds start address bits A[7:0] of I/O address window 1.

3.2.3.7 IOSH1—I/O Address 1 Start High Byte Register

Register Offset:	Socket A—0Dh
	Socket B—4Dh
	Socket C—8Dh
	Socket D—CDh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the start address of I/O address window 1.

Bits[7:0]: I/O Window 1 Start Address High Bytes
This field holds start address bits A[15:8] of I/O address window 1.

3.2.3.8 IOSTL1—I/O Address 1 Stop Low Byte Register

Register Offset:	Socket A—0Eh
	Socket B—4Eh
	Socket C—8Eh
	Socket D—CEh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the low order address bits that are used to determine the start address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Stop Address Low Bytes
This field holds stop address bits A[7:0] of I/O address window 1.

3.2.3.9 IOSTH1—I/O Address 1 Stop High Byte Register

Register Offset:	Socket A—0Fh
	Socket B—4Fh
	Socket C—8Fh
	Socket D—CFh
Default value:	00h
Access:	Read/Write
Size:	8 bits

This register holds the high order address bits that are used to determine the stop address of I/O address window 1. This provides a minimum 1 byte window for I/O address window 1 if the Start and Stop addresses are the same.

Bits[7:0]: I/O Window 1 Stop Address High Bytes
This field holds stop address bits A[15:8] of I/O address window 1.

3.2.4 MEMORY MAPPING CONTROL REGISTERS

The Memory Mapping Control Registers are 8 bit, read/write registers that specify the starting and stopping addresses of the five memory windows. The registers are listed in Table 11.

The registers are identical for each window. Therefore, only one of each type of register is shown in the following descriptions. The addresses for all five windows for each socket are shown, however, in the *Register Offset* section of each register description.

Table 11. Memory Mapping Control Registers

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
10h	50h	90h	D0h	SMSL0	System Memory Address Mapping Window 0 Start Low Byte	R/W
18h	58h	98h	D8h	SMSL1	System Memory Address Mapping Window 1 Start Low Byte	R/W
20h	60h	A0h	E0h	SMSL2	System Memory Address Mapping Window 2 Start Low Byte	R/W
28h	68h	A8h	E8h	SMSL3	System Memory Address Mapping Window 3 Start Low Byte	R/W
30h	70h	B0h	F0h	SMSL4	System Memory Address Mapping Window 4 Start Low Byte	R/W
11h	51h	91h	D1h	SMSH0	System Memory Address Mapping Window 0 Start High Byte	R/W
19h	59h	99h	D9h	SMSH1	System Memory Address Mapping Window 1 Start High Byte	R/W
21h	61h	A1h	E1h	SMSH2	System Memory Address Mapping Window 2 Start High Byte	R/W
29h	69h	A9h	E9h	SMSH3	System Memory Address Mapping Window 3 Start High Byte	R/W
31h	71h	B1h	F1h	SMSH4	System Memory Address Mapping Window 4 Start High Byte	R/W
12h	52h	92	D2h	SMSTL0	System Memory Address Mapping Window 0 Stop Low Byte	R/W
1Ah	5Ah	9Ah	DAh	SMSTL1	System Memory Address Mapping Window 1 Stop Low Byte	R/W
22h	62h	A2h	E2h	SMSTL2	System Memory Address Mapping Window 2 Stop Low Byte	R/W
2Ah	6Ah	AAh	EAh	SMSTL3	System Memory Address Mapping Window 3 Stop Low Byte	R/W
32	72h	B2h	F2h	SMSTL4	System Memory Address Mapping Window 4 Stop Low Byte	R/W
13h	53h	93h	D3h	SMSTH0	System Memory Address Mapping Window 0 Stop High Byte	R/W
1Bh	5Bh	9Bh	DBh	SMSTH1	System Memory Address Mapping Window 1 Stop High Byte	R/W
23h	63h	A3h	E3h	SMSTH2	System Memory Address Mapping Window 2 Stop High Byte	R/W

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Table 11. Memory Mapping Control Registers (Continued)

Register Offset Sockets A:D				Mnemonic	Register Name	Access
A	B	C	D			
2Bh	6Bh	ABh	EBh	SMSTH3	System Memory Address Mapping Window 3 Stop High Byte	R/W
33h	73h	B3h	F3h	SMSTH4	System Memory Address Mapping Window 4 Stop High Byte	R/W
14h	54h	94h	D4h	OFFL0	Card Memory Offset Address 0 Low Byte	R/W
1Ch	5Ch	9Ch	DCh	OFFL1	Card Memory Offset Address 1 Low Byte	R/W
24h	64h	A4h	E4h	OFFL2	Card Memory Offset Address 2 Low Byte	R/W
2Ch	6Ch	ACh	ECh	OFFL3	Card Memory Offset Address 3 Low Byte	R/W
34h	74h	B4h	F4h	OFFL4	Card Memory Offset Address 4 Low Byte	R/W
15h	55h	95h	D5h	OFFH0	Card Memory Offset Address 0 High Byte	R/W
1Dh	5Dh	9Dh	DDh	OFFH1	Card Memory Offset Address 1 High Byte	R/W
25h	65h	A5h	E5h	OFFH2	Card Memory Offset Address 2 High Byte	R/W
2Dh	6D	ADh	EDh	OFFH3	Card Memory Offset Address 3 High Byte	R/W
35h	75h	B5h	F5h	OFFH4	Card Memory Offset Address 4 High Byte	R/W

3.2.4.1 SMSL[4:0]—System Memory Address Mapping Windows 0-4 Start Low Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	10h	18h	20h	28h	30h
Socket B	50h	58h	60h	68h	70h
Socket C	90h	98h	A0h	A8h	B0h
Socket D	D0h	D8h	E0h	E8h	F0h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the low order address bits that determine the start address of the corresponding system memory address mapping windows. The register contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory accesses are valid.

Bits[7:0]: System Memory Window Start Address This field holds the system memory window start address bits A[19:12].

3.2.4.2 SMSH[4:0]—System Memory Address Mapping Windows 0-4 Start High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	11h	19h	21h	29h	31h
Socket B	51h	59h	61h	69h	71h
Socket C	91h	99h	A1h	A9h	B1h
Socket D	D1h	D9h	E1h	E9h	F1h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the high order address bits that determine the start address of the corresponding system memory address mapping windows. The address bits correspond to PCI memory address bits A[23:20], and are used to determine whether memory accesses are valid. The data path size of each window is controlled by a bit in its corresponding register.

Bit 7: Data Size
This bit selects an 8-bit memory data path to the PC Card when set to 0, and a 16-bit memory data path when set to 1.

Bit 6: Reserved

Bits[5:4]: Scratch Bits

These bits can be used for general-purpose register storage and retrieval.

Bits[3:0]: Memory Window Start Address
These are high order address bits that determine the start address of the system memory address mapping window.

3.2.4.3 SMSTL[4:0]—System Memory Address Mapping Windows 0–4 Stop Low Byte Register

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	12h	1Ah	22h	2Ah	32h
Socket B	52h	59h	62h	6Ah	72h
Socket C	91h	99h	A2h	AAh	B2h
Socket D	D2h	D9h	E2h	EAh	F2h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers hold the low order address bits that determine the stop address of the corresponding system memory address mapping windows. The register contents correspond to PCI memory address bits A[19:12], and are used to determine whether memory accesses are valid.

Bits[7:0]: System Memory Window Stop Address
This field holds the system memory window stop address bits A[19:12].

3.2.4.4 SMSTH[4:0]—System Memory Address Mapping Windows 0–4 Stop High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	13h	1Bh	23h	2Bh	33h
Socket B	53h	5Bh	63h	6Bh	73h
Socket C	93h	9Bh	A3h	ABh	B3h
Socket D	D3h	DBh	E3h	EBh	F3h

Default value: 10100000b
Access: Read/Write
Size: 8 bits

These five registers contain the high order address bits that determine the stop address of the corresponding system memory address mapping windows. The address bits correspond to PCI memory address bits A[23:20], and are used to determine whether memory accesses are valid. Two bits in each of the registers select delays for 16-bit accesses to the corresponding system memory window.

Bits[7:5]: Memory Window Timing Select
PCMCIA timing parameters are independently configured for each Common Memory Window by programming these timing bits. Timing Mode 101 is the default for this field, and cannot be changed (i.e. writes to the bits 5-7 are ignored) until PPEC-PCMCIA PCICON register bit 5 (Enhanced PCMCIA Timing Mode Enable) is set to 1.

Bit 4: Reserved

Bits[3:0]: Memory Window Stop Address
This field holds system memory window stop address bits A23:A20.

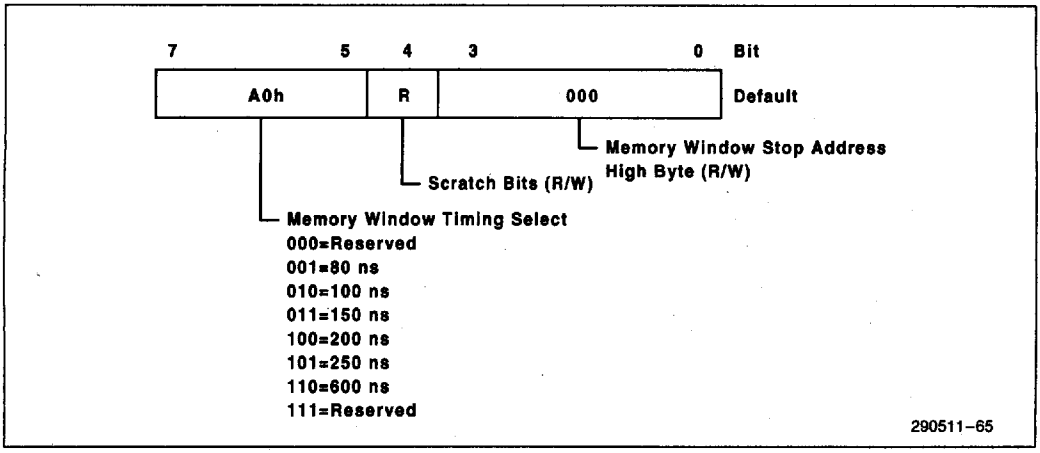

Figure 35. System Memory Address Mapping Windows 0–4 Stop High Byte Registers

3.2.4.5 OFFL[4:0]—Card Memory Offset Address 0-4 Low Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	14h	1Ch	24h	2Ch	34h
Socket B	54h	5Ch	64h	6Ch	74h
Socket C	94h	9Ch	A4h	ACh	B4h
Socket D	D4h	DCh	E4h	ECh	F4h

Default value: 00h
Access: Read/Write
Size: 8 bits

These five registers contain the low order address bits that are added to system address bits A[19:12] to generate the memory addresses for the PC Cards.

Bits[7:0]: Card Memory Offset Address
These bits are added to PCI memory address bits A[19:12] to generate the memory address for the PC Card.

3.2.4.6 OFFH[4:0]—Card Memory Offset Address 0 High Byte Registers

Register Offset:

	Window 0	Window 1	Window 2	Window 3	Window 4
Socket A	15h	1Dh	25h	2Dh	35h
Socket B	55h	5Dh	65h	6Dh	75h
Socket C	95h	9Dh	A5h	ADh	B5h
Socket D	D5h	DDh	E5h	EDh	F5h

Default value: 00h
Access: Read/Write
Size: 8 bits

Bits[5:0] of the registers are added to PCI memory address bits A[23:20] to generate the memory addresses for the PC Cards. The registers also control the PC Card memory software write protect for the corresponding system memory windows, and select whether the memory windows are mapped to attribute memory, or to common memory on the PC Cards.

Bit 7: Write Protect
When this bit is set to 1, write operations to the PC Card through the corresponding system memory window are inhibited. When set to 0, write operations are allowed. The WP Switch on the memory card sets the Memory Write Protect bit in the Interface Status Register, but does not alone block memory write cycles.

Bit 6: Register Active
When this bit is set to 1, accesses to the system memory window result in attribute memory on the PC Card being accessed by asserting REG low. When set to 0, accesses to the system memory result in common memory on the PC Card being accessed by driving REG high.

Bits[5:0]: Card Memory Offset Address
These bits are added to PCI memory address bits A[23:20] to generate the memory address for the PC Card.

4.0 ELECTRICAL CHARACTERISTICS

4.1 Maximum Ratings

Case Temperature Under Bias . . . −65°C to +110°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltages
with Respect to Ground . . . −0.5V to V_{CC} + 0.5V
Voltage On Any Pin . . . . . −0.5V to V_{CC} + 0.5V
Power Dissipation 1.0W

The junction temperature for the PPEC is 95°C with a case temperature of 85°C.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Characteristics

4.2.1 PCI INTERFACE DC SPECIFICATIONS

Table 12. PCI Interface DC Characteristics (V_{CC} = 5V*5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
V_{IL}	Input Low Voltage		0.8	V		
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V		
V_{OL}	Output Low Voltage		0.55	V	I_{OL} = 6 mA	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2.0 mA	
I_{IL}	Low-Level Input Current		−70	μA	V_{IN} = 0.5V	
I_{IH}	High-Level Input Current		70	A	V_{IN} = 2.7V	
C_{IN}	Input Capacitance		10	pF		
C_{OUT}	Output Capacitance		10	pF		
C_{CLK}	PCICLK Input Capacitance		12	pF		
I_{CC}	V_{CC} Supply Current		200	mA		

4.2.2 PCMCIA INTERFACE DC SPECIFICATIONS

Table 13. PCMCIA Interface DC Specifications (V_{CC} = 5V*5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Test Condition	Note
V_{IL}	Input Low Voltage		0.8	V		
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V		
V_{OL1}	Output Low Voltage		0.5	V	I_{OL} = −8 mA	1
V_{OH1}	Output High Voltage	2.4 2.8	V_{CC}3/5	V	I_{OH} = 4 mA I_{OH} = 2 mA	1,3,4
V_{OL2}	Output Low Voltage		0.5	V	I_{OL} = −4 mA	2
V_{OH2}	Output High Voltage	2.4 2.8	V_{CC}3/5	V	I_{OH} = 2 mA I_{OH} = 1 mA	2,3,4
I_{IL}	Low-level Input Current		−10	A		
I_{IH}	High-level Input Current		10	A		
C_{IN}	Capacitance Input		10	pF		
C_{OUT}	Capacitance Output		10	pF		
I_{CC}	V_{CC} Supply Current		200	mA		

NOTES:
1. V_{OL1} and V_{OH1} apply to PCMCIA signals that are shared in Mode 1: REG#, OE#, IOWR#, IORD#, CDATA[15:0], CADR[25:0].
2. V_{OL2} and V_{OH2} apply to all PCMCIA signals that are not listed in Note 1.
3. V_{OH} = 2.8V is the minimum high-state voltage specified by the PCMCIA specification.
4. V_{CC}3/5 is the voltage applied to the SOCKETPWR pins. This voltage may be set at 5V ±10% or 3.3V ±0.3V.

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4.3 AC Characteristics

4.3.1 CLOCK SIGNAL AC SPECIFICATIONS

Table 14. Clock Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
t1a	Cycle Time	30		ns		36
t1b	High Time	12		ns	At 2.0V	36
t1c	Low Time	12		ns	At 0.8V	36
t1d	Rise Time		3	ns	0.8V to 2.0V	36
t1e	Fall Time		3	ns	2.0V to 0.8V	36

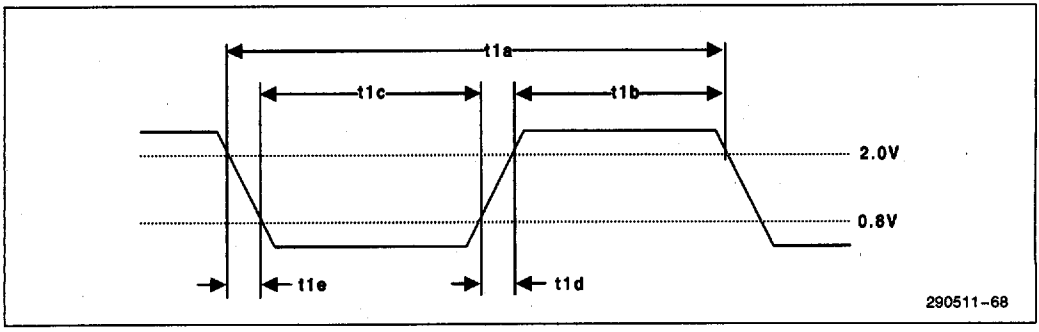

Figure 36. PCICLK Timing

4.3.2 PCI INTERFACE AC SPECIFICATIONS

Table 15. PCI Interface AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	PCIRST#					
t2a	Pulse Width	1		ms		37
t2b	PCICLK Active Setup to PCIRST# Negated	100		s		37
	AD[31:0], C/BE[3:0], FRAME#, IRDY#, PAR, PERR#, SERR#, TRDY#, DEVSEL#, STOP#, PCILOCK#, IDSEL					
t3a	Delay from PCICLK Rising	2	11	ns		38
t3b	Setup to PCICLK Rising	7		ns		38
t3c	Hold from PCICLK Rising	0		ns		38

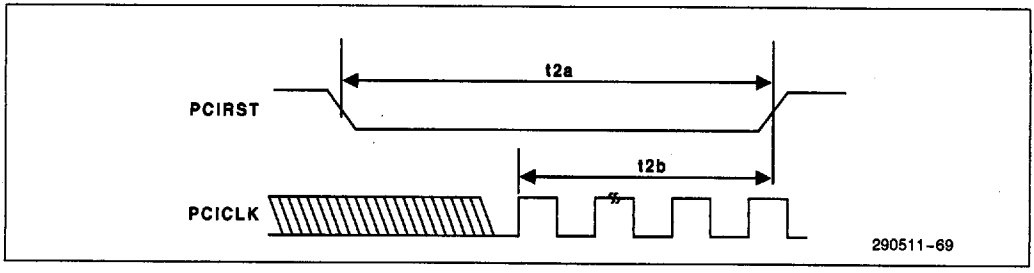

Figure 37. PCIRT# Timing

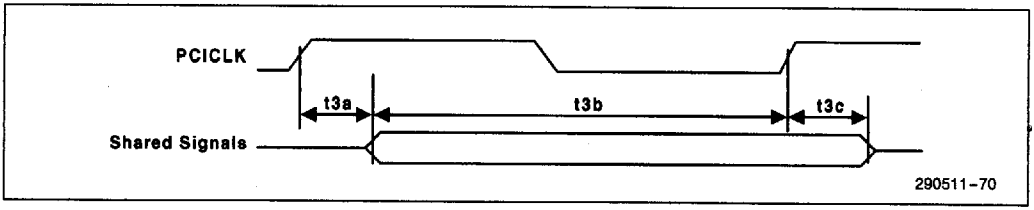

Figure 38. Shared Signal Timing

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4.3.3 SYSTEM SIGNAL AC SPECIFICATIONS

Table 16. System Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	IRQx					
t4a	Card Status change to IRQx/INTx# Valid		2 CLKs + 20	ns	Card Status change can be caused by any CSC event, such as the assertion of BVD[1,0], CD[1,0], STSCHG#, etc.	39
t4b	PC Card IREQ# to IRQx/INTx# Delay		35	ns		39
	SPKROUT#					
t4c	SPKR# to SPKROUT# Delay		35	ns		39

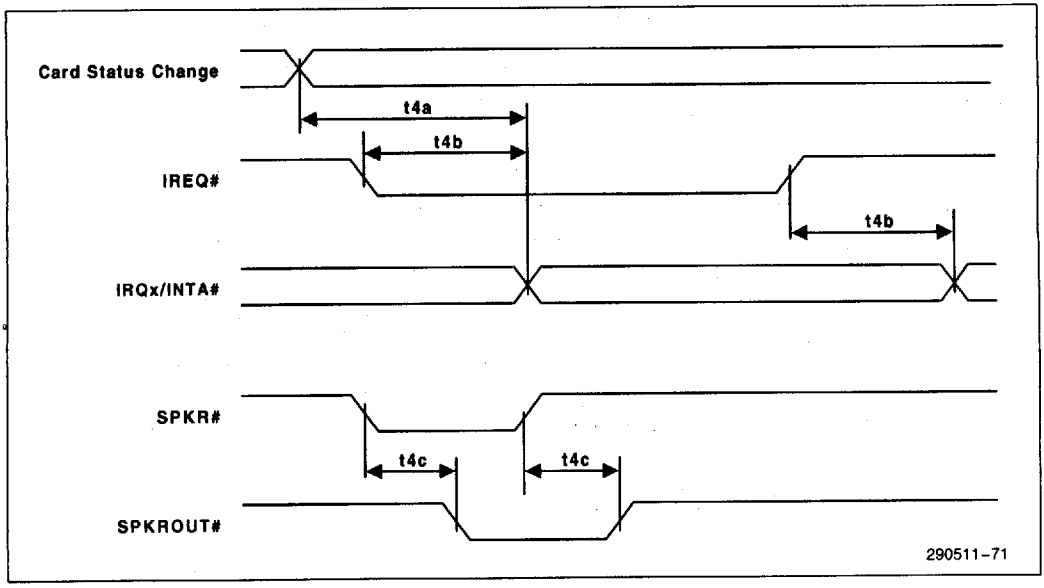

Figure 39. System Signal Timing

4.3.4 POWER WRITE SIGNAL AC CHARACTERISTICS

Table 17. Power Write Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
t5a	Data Valid Setup to PWRWR# Asserted	5		ns		40
t5b	Data Valid Hold from PWRWR# Negated	1		CLK		40
t5c	Pulse Width	5		CLK		40

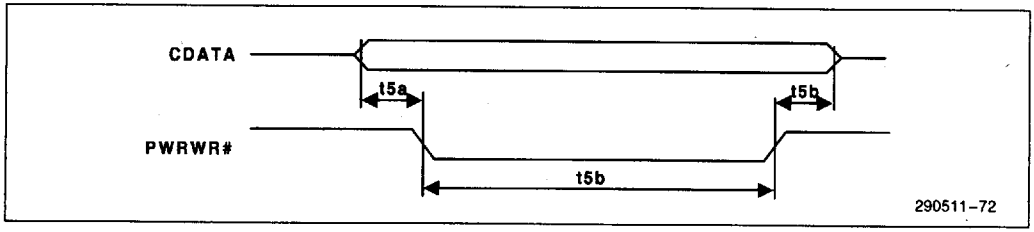

Figure 40. Power Write Signal Timing

4.3.5 PCMCIA MEMORY SIGNAL AC CHARACTERISTICS

Table 18 lists signal timing parameters for memory read and write operations. All of the parameters listed in the table apply to Common Memory operations.

Attribute Memory writes and 5.0V Attribute Memory reads use the timing for 250ns cards (see *Notes* column); 3.3V Attribute Memory reads use the timing for 600 ns cards.

Table 18. PCMCIA Memory Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CDATA[15:0]					
t7a	Valid Setup to WE# Asserted	2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
t7b	Hold from WE# Negated	1 CLK − 10 1 CLK − 10 2 CLKs − 10 2 CLKs − 10 2 CLKs − 10(1) 5 CLKs − 10(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42

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Table 18. PCMCIA Memory Signal AC Characteristics (V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C)
(Continued)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CADR[25:0],REG#,CE[2:1]#,EXTDIR					
t6a	Valid Setup to OE# Asserted	1 CLK − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t6b	Valid Setup to data Latched	4 CLKs − 20 5 CLKs − 20 6 CLKs − 20 8 CLKs − 20 10 CLKs − 20(1) 22 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t7c	Valid Setup to WE# Asserted	2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 2 CLKs − 20 3 CLKs − 20(1) 4 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
t7d	Hold from WE# Negated	1 CLK − 10 1 CLK − 10 2 CLKs − 10 2 CLKs − 10 2 CLKs − 10(1) 5 CLKs − 10(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42
	OE#					
t6c	OE# Asserted to Data Latched	3 CLKs − 20 3 CLKs − 20 4 CLKs − 20 6 CLKs − 20 7 CLKs − 20(1) 18 CLKs − 20(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	41
t6d	Data Latched to OE# Negated	0		ns		41
	WE#					
t7e	Pulse Width	3 CLKs + 0 3 CLKs + 0 3 CLKs + 0 5 CLKs + 0 6 CLKs + 0(1) 11 CLKs + 0(2)		ns	80 ns Card 100 ns Card 150 ns Card 200 ns Card 250 ns Card 600 ns Card	42

Table 18. PCMCIA Memory Signal AC Characteristics
(V_{CC} = 5V ±5%, T_{case} = 0°C to +85°C) (Continued)

Symbol	Parameter	Min	Max	Unit	Note	Figure
	WAIT#					
t6e	WAIT# Negated to Data Latched	1 CLK + 0	2 CLKs + 10	ns	All Cards	41
t7f	WAIT# Negated to WE# Negated	1 CLK + 0	2 CLKs + 10	ns	All Cards	42
t6f	Valid Delay from CADR[25:0] Valid		50			41

NOTES:
1. Applies to Common Memory reads and writes, Attribute Memory writes, and 5.0V Attribute Memory reads.
2. Applies to Common Memory reads and writes, and 3.3V Attribute Memory reads.

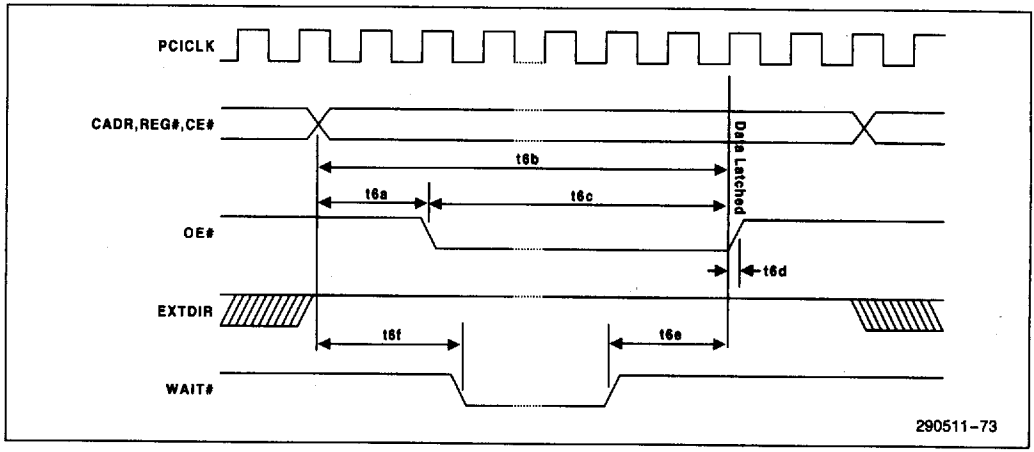

Figure 41. Memory Read Timing

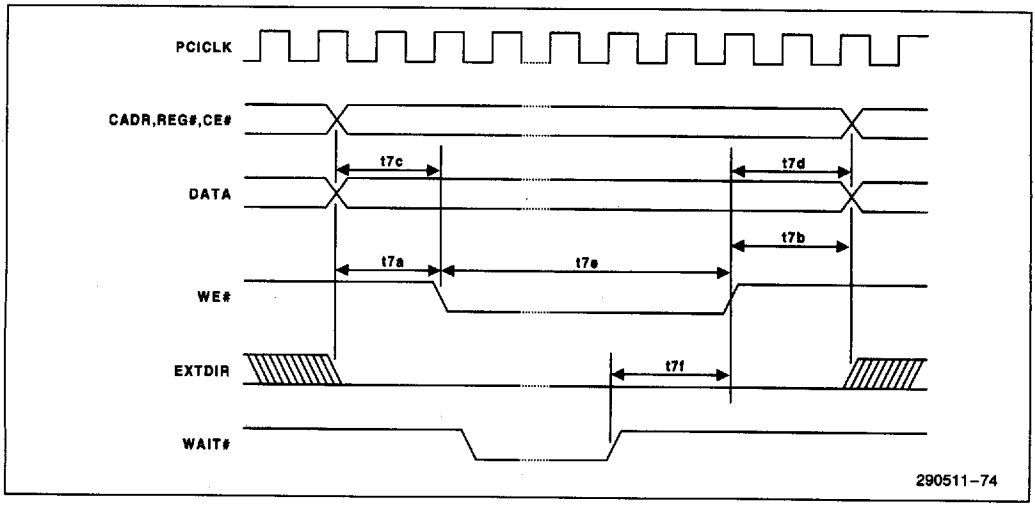

Figure 42. Memory Write Timing

4.3.6 PCMCIA I/O SIGNAL AC CHARACTERISTICS

Table 19 lists signal timing parameters for I/O read and write operations.

Table 19. PCMCIA I/O Signal AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note	Figure
	CDATA[15:0]					
t9a	Valid Setup to IOWR# Asserted	4 CLKs − 20		ns		44
t9b	Hold from IOWR# Negated	2 CLKs − 10		ns		44
	CADR[25:0],REG#,CE[2:1]#,EXTDIR					
t8a	Valid Setup to IORD# Asserted	4 CLKs − 20				43
t8b	Valid Setup to Data Latched	10 CLKs − 20				43
t9c	Valid Setup to IOWR# Asserted	4 CLKs − 20				44
t9d	Hold from IOWR# Negated	2 CLKs − 10				44
	IORD#					
t8c	IORD# Asserted to Data Latched	6 CLKs − 20				43
t8d	Data Latched to OE# Negated	0				43
	IOWR#					
t9e	Pulse Width	6 CLKs + 0				44
	WAIT#					
t8e	WAIT# Negated to Data Latched	1 CLK + 0				43
t9f	WAIT# Negated to IOWR# Negated	1 CLK + 0				44
t8f,t9g	Valid Delay from IORD#/IOWR# Valid		50			43, 44
	IOIS16#					
t10g	Valid Delay from CADR[25:0] Valid		50			44

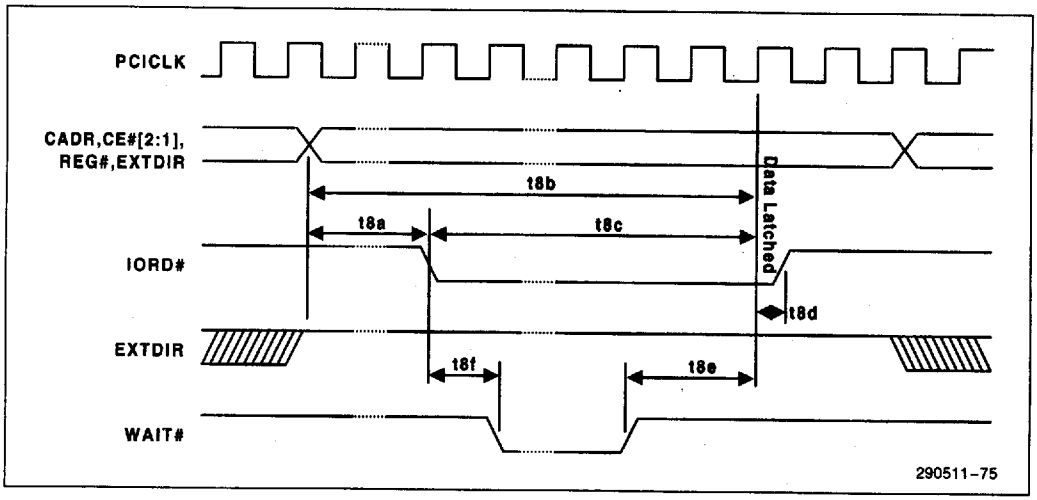

Figure 43. I/O Read Timing

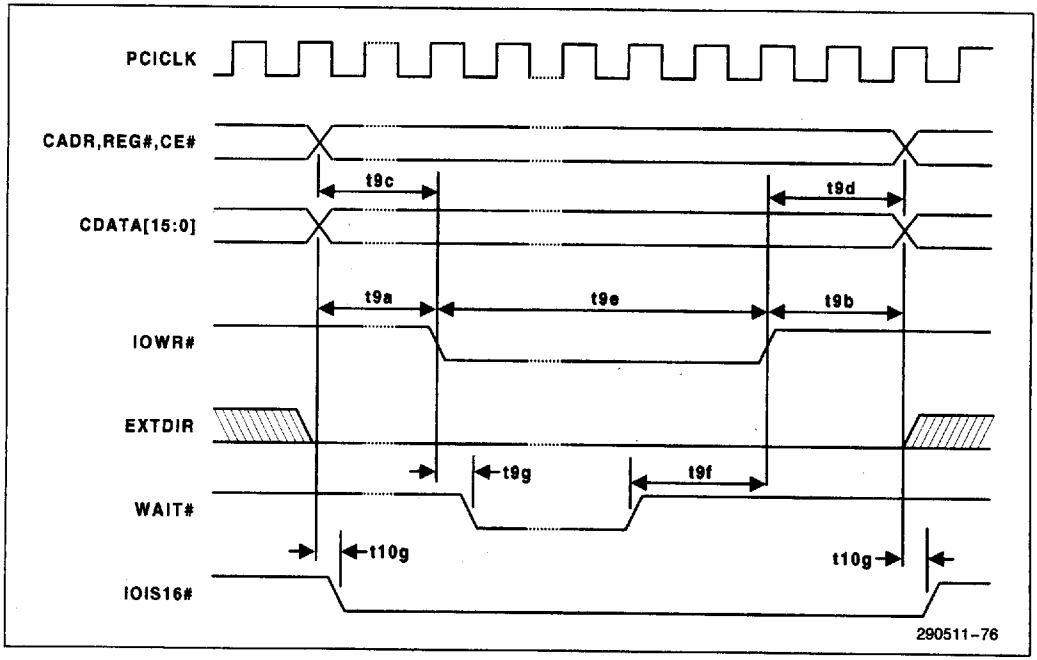

Figure 44. I/O Write Timing

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4.3.7 IDE SIGNAL AC CHARACTERISTICS

Table 20 lists signal timing parameters with respect to PCI clock edges for IDE read and write operations. Note that integral number of clock delays are programmable for all IDE signals.

Table 20. IDE Signal AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note	Figure
t10a	DIOR#/DIOW# Delay from PCI Clock	2	20	ns		45
t10b	Address/Data/CS Delay from PCI Clock	2	30	ns		45
T_{pw}	DIOR#/DIOW# Duration	1	8	CLK	Programmable	45
T_{su}	Address/Data/CS Setup to DIOR#/DIOW#	1	4	CLK	Programmable	45
T_{cyc}	Address/Data/CS Cycle Time	5	31	CLK	Programmable	45

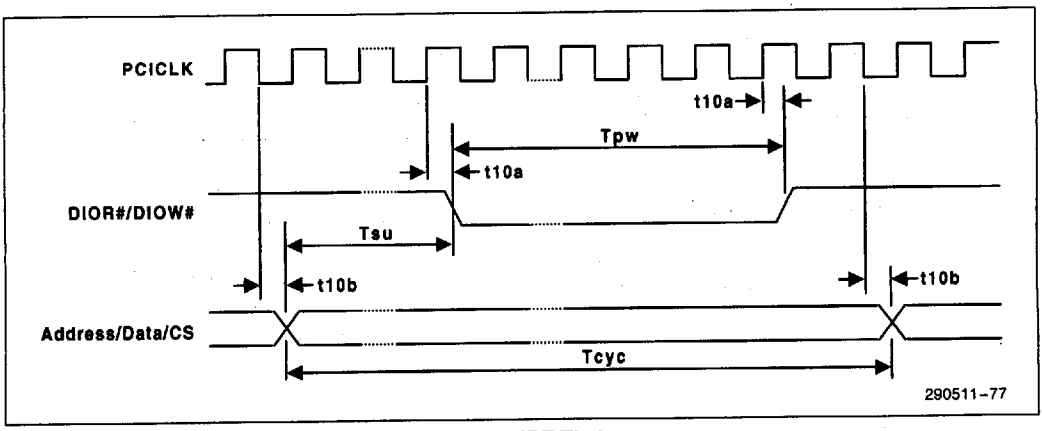

Figure 45. IDE Timing