STANDARD MICROSYSTEMS CORPORATION

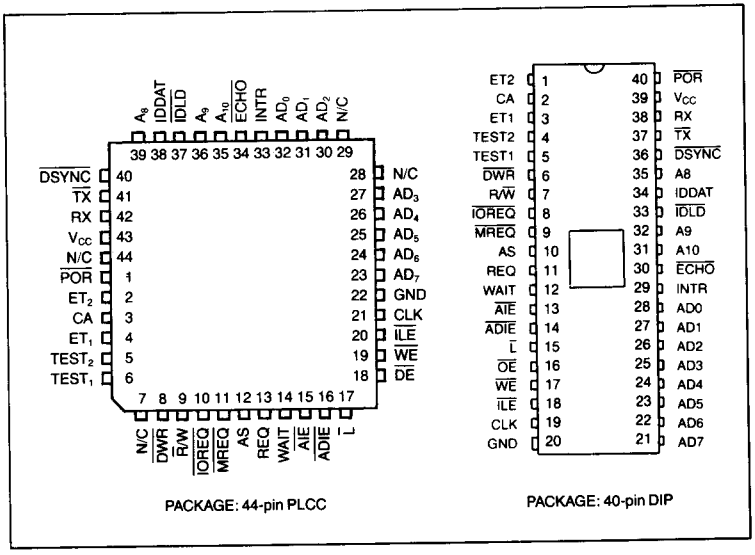
COM 90C26
PRELIMINARY

Local Area Network Controller
LANC™

FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET® local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 90C26
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)
- ☐ Low power CMOS technology
- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single +5 volt supply
- ☐ Compatible with HYC9058 (HITI) and HYC9068 (LAND)

PIN CONFIGURATION



PACKAGE: 44-pin PLCC

PACKAGE: 40-pin DIP

GENERAL DESCRIPTION

The COM 90C26 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The Com 90C26 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 90C26 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 90C26 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 90C26 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 90C26. The processor can write commands to the COM 90C26 and also read COM 90C26 status. The COM 90C26 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

ARCNET® is a registered trademark of the Datapoint Corporation.

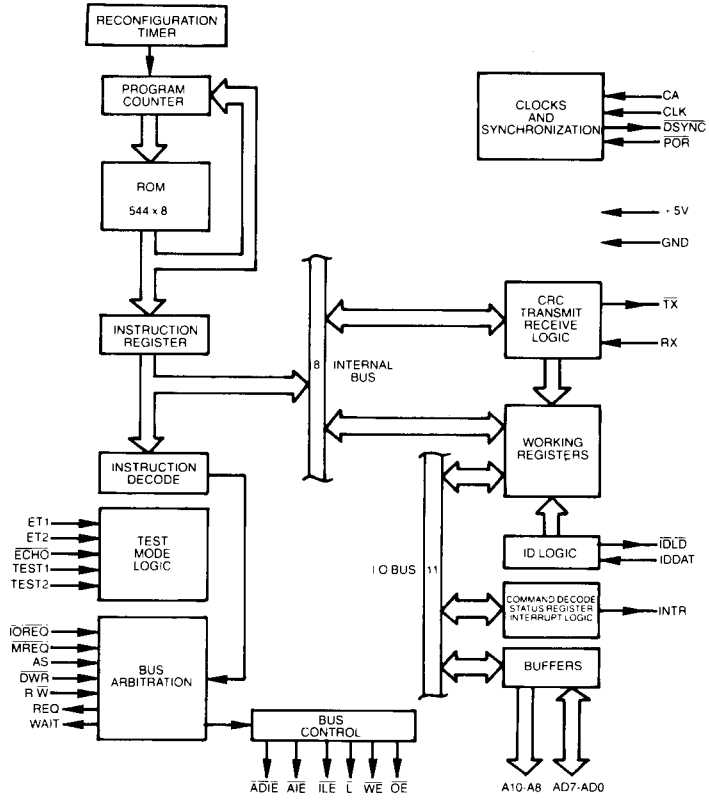


FIGURE 1—COM90C26 BLOCK DIAGRAM

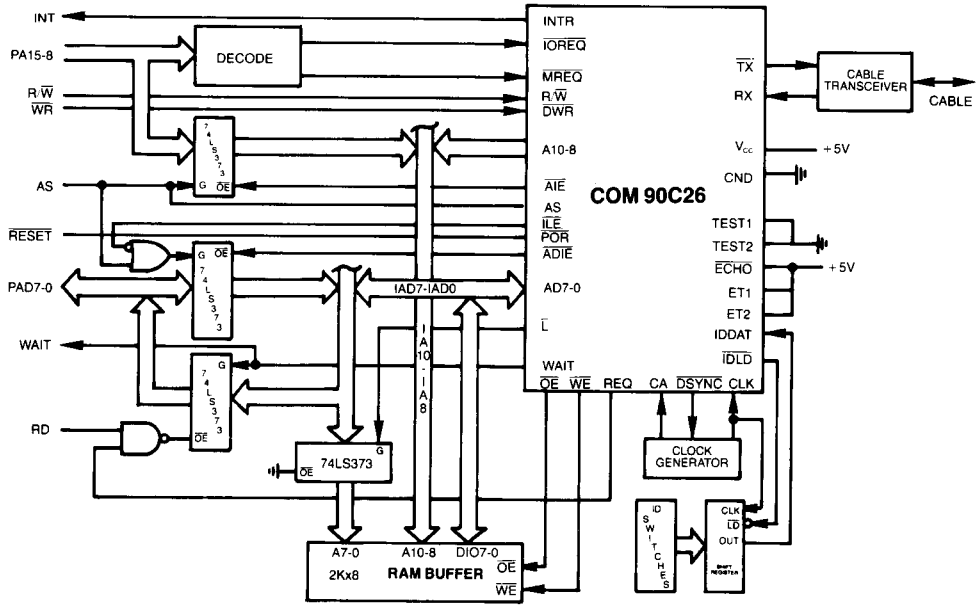


FIGURE 2—TYPICAL COM 90C26 INTERFACE

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

DIP PIN NO.	NAME	SYMBOL	FUNCTION
31, 32, 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 90C26 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21, 22, 23, 24, 25, 26, 27, 28	ADDRESS/ DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 90C26. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 90C26.
8	I/O REQUEST	$\overline{\text{IOREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 90C26. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{\text{MREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	A high level on this input signal indicates that the processor's access cycle to the COM 90C26 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 90C26. The write cycle will not completed, however, until the $\overline{\text{DWR}}$ input is asserted. This signal is sampled internally on falling edge of AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 90C26 to sample the state of the $\overline{\text{IOREQ}}$, $\overline{\text{MREQ}}$ and R/$\overline{\text{W}}$ inputs. The COM 90C26 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{\text{MREQ}}$ or $\overline{\text{IOREQ}}$ passed through an internal transparent latch gated with AS.
12	WAIT	$\overline{\text{WAIT}}$	This output signal is asserted by the COM 90C26 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 90C26 is ready for the processor to complete its cycle.
6	DELAYED WRITE	$\overline{\text{DWR}}$	This input signal informs the COM 90C26 that valid data is present on the processor's data bus for write cycles. The COM 90C26 will remain in the WAIT state until this signal is asserted. $\overline{\text{DWR}}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	$\overline{\text{INTR}}$	This output signal is asserted when an enabled interrupt condition has occured. $\overline{\text{INTR}}$ returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{\text{ILE}}$	This output signal, in conjunction with $\overline{\text{ADIE}}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 90C26 operations.
14	ADDRESS/ DATA INPUT ENABLE	$\overline{\text{ADIE}}$	This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{\text{ILE}}$ onto the interface address/data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{\text{AIE}}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	$\overline{\text{L}}$	This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{\text{WE}}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{\text{WE}}$.
16	OUTPUT ENABLE	$\overline{\text{OE}}$	This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{\text{IDLD}}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 90C26. The shift register is clocked with the same signal that feeds the COM 90C26 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2, 1	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 90C26 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.
37	TRANSMIT DATA	$\overline{\text{TX}}$	This output signal contains the serial transmit data to the CABLE TRANSCEIVER.
38	RECEIVE DATA	RX	This input signal contains the serial receive data from the CABLE TRANSCEIVER.

DESCRIPTION OF PIN FUNCTIONS (Continued)

PIN NO.	NAME	SYMBOL	FUNCTION
4, 5	TEST PIN 2 TEST PIN 1	TEST2 TEST1	These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing.
30	ECHO DIAGNOSTIC ENABLE	$\overline{\text{ECHO}}$	When this input signal is low, the COM 90C26 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 90C26 bus cycles, bus arbitration, serial ID input, and the internal timers.
2	CA	CA	This input signal is a 5 MHz clock used to control the operation of the COM 90C26 microcoded sequencer. This input is periodically halted in the high state by the $\overline{\text{DSYNC}}$ output.
36	DELAYED SYNC	$\overline{\text{DSYNC}}$	This output signal is asserted by the COM 90C26 to cause the external clock generator logic to halt the CA clock. Refer to figure 9.
40	POWER ON RESET	$\overline{\text{POR}}$	This input signal clears the COM 90C26 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	V_{CC}	Power Supply
20	GROUND	GND	Ground

PROTOCOL DESCRIPTION

LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 85 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 86 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 90C26's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 90C26 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will

verify the packet. If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsucessful delivery of the packet. An interrupt mask permits the COM 90C26 to generate an interrupt to the processor when selected status bits become true. Figure 4 is a flow chart illustrating the internal operation of the COM 90C26.

NETWORK RECONFIGURATION

A significant advantage of the COM 90C26 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 90C26 is turned on (creating a new active node on the network), or if the COM 90C26 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 90C26 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 90C26 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 90C26 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 90C26 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 90C26 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 90C26 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 90C26 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 90C26 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 90C26 on the network will finally have saved a NID value equal to the ID of the COM 90C26 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

BROADCAST MESSAGES

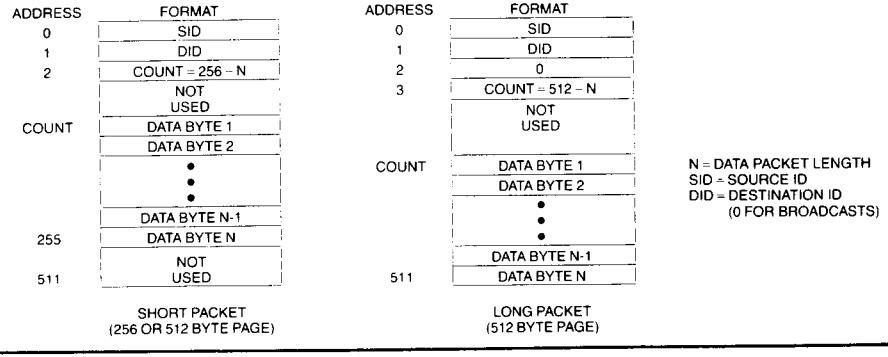
Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 3 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 90C26 COMMANDS") to a logic zero.

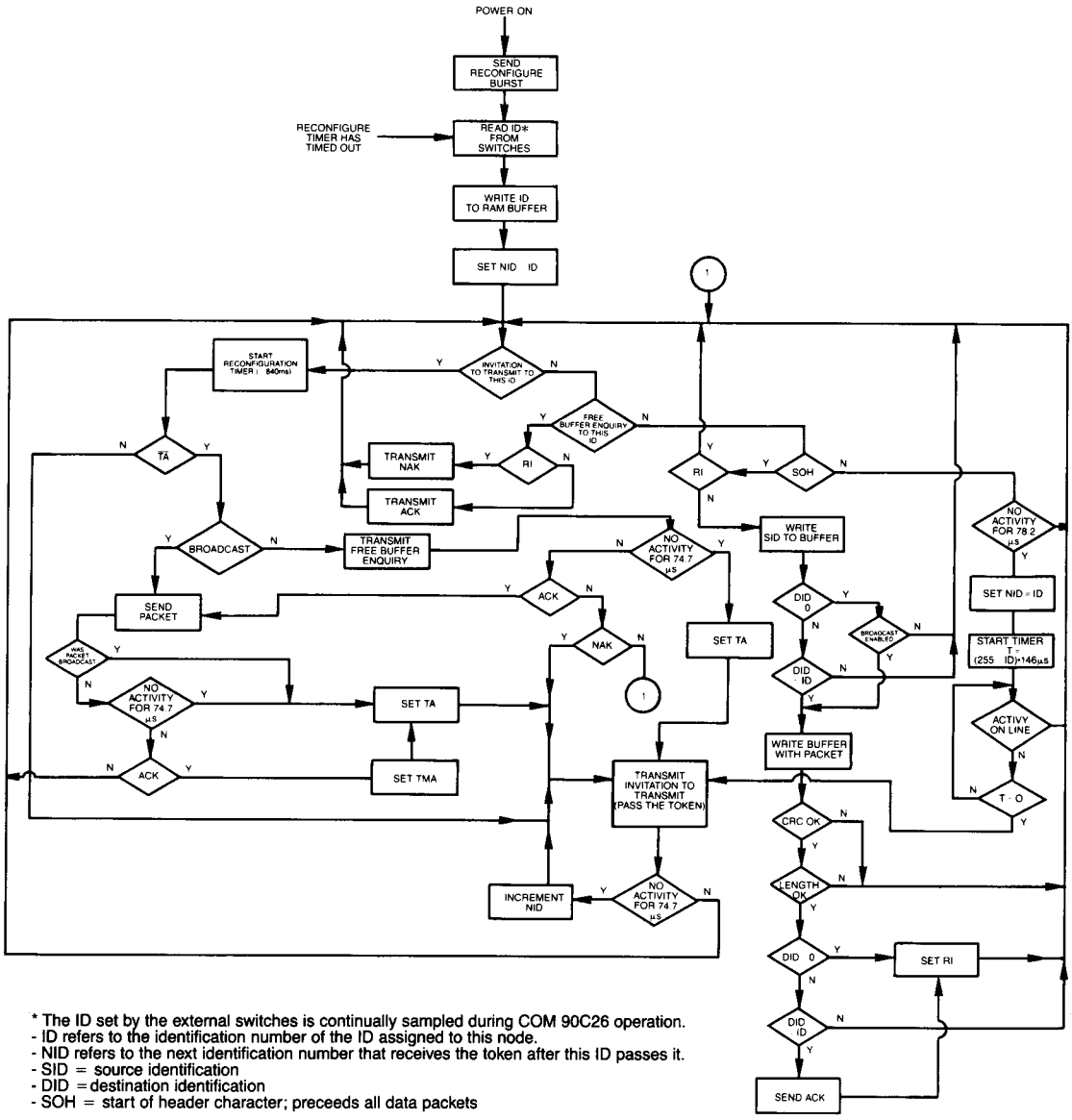
COM 90C26 OPERATION

BUFFER CONFIGURATION

During a transmit sequence, the COM 90C26 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 90C26 will interpret the packet as a long or short packet depending on whether the contents of buffer location 002 is zero or non zero. During a receive sequence, the COM 90C26 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 90C26 receiver or the COM 90C26 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512) byte are shown below.

FIGURE 3— RAM BUFFER PACKET CONFIGURATION





* The ID set by the external switches is continually sampled during COM 90C26 operation.
- ID refers to the identification number of the ID assigned to this node.
- NID refers to the next identification number that receives the token after this ID passes it.
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

FIGURE 4—90C26 OPERATION

PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 90C26 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 90C26, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 90C26.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 90C26 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multi-message transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 90C26, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 90C26 or command writes to the COM 90C26).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 90C26 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 90C26.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{\text{IOREQ}}$ or $\overline{\text{MREQ}}$ is asserted. These access cycles run completely asynchronous with respect to the COM 90C26. Because of this, upon processor access cycle requests, the COM 90C26 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 90C26 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 90C26, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{\text{AIE}}$ and $\overline{\text{ADIE}}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{\text{L}}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{\text{OE}}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

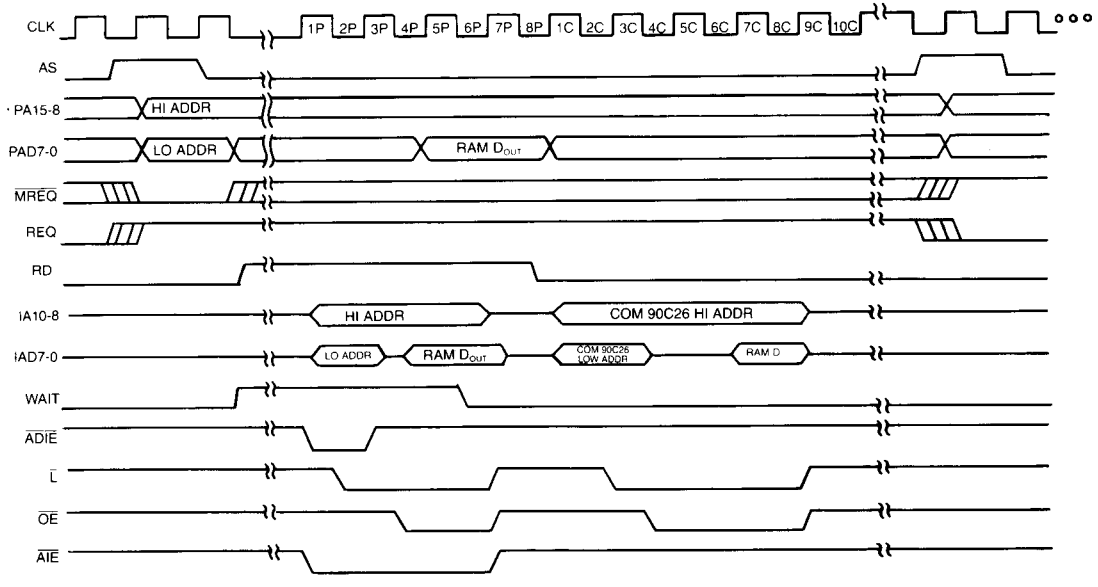


FIGURE 5—PROCESSOR READ RAM FOLLOWED BY COM 90C26 READ RAM

and driven out via the logic function RD ended with REQ. For processor I/O read cycles from the COM 90C26, ADIE and AIE are used to enable the processor address into the COM 90C26. Data out of the COM 90C26 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 90C26 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 90C26 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 90C26 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 90C26 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 90C26, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 90C26. Delaying the activation of DWR will hold up the COM 90C26 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 90C26 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 90C26 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 90C26 cycle will follow immediately after the processor cycle. Figure 5 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 90C26 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 5 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 90C26 access cycle will take 5 CLK periods to end. Figure 5 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 90C26 request has already been granted, the COM 90C26 cycle will occur first, as shown in figure 5. Figure 6 illustrates the timing relationship of a COM 90C26 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 90C26 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 6, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 90C26 produces a leading edge on both ADIE and AIE. If the processor request

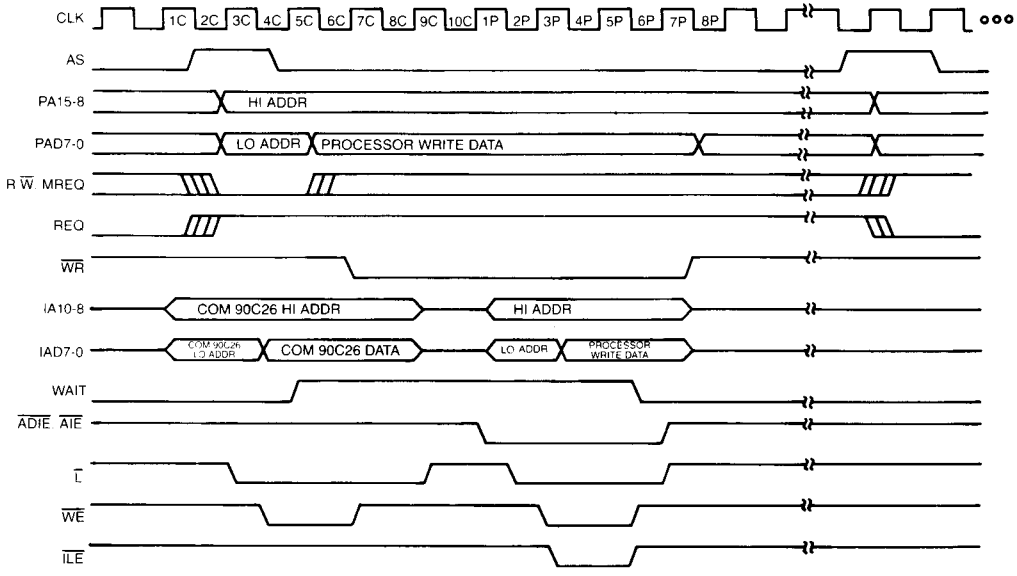


FIGURE 6—COM 90C26 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM

occurs before the end of half CLK interval 5C (figure 6 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 90C26 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 7 and 8 illustrate timing for Processor Read COM 90C26 and Processor Write COM 90C26 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 5 and 6 if these processor cycles occur.

POWER UP AND INITIALIZATION

The COM 90C26 has the following power up requirements:

1—The $\overline{POR}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the POR input is removed.
3—While $\overline{POR}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{POR}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{POR}$ may be released before CA begins running.

During $\overline{POR}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{DSYNC}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{POR}$ signal is removed, the COM 90C26 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 90C26 will start operation four CA clock cycles after the $\overline{POR}$ signal is removed. At this time, the COM 90C26, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 90C26 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

CLOCK GENERATOR

The COM 90C26 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 90C26 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{DSYNC}$ output and the RX input. The $\overline{DSYNC}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{DSYNC}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{DSYNC}$. (See figure 10 for an implementation of this circuit.)

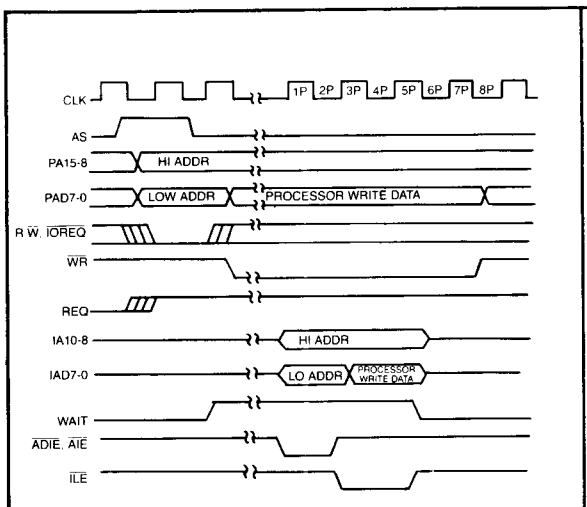


FIGURE 7—PROCESSOR READ COM 90C26

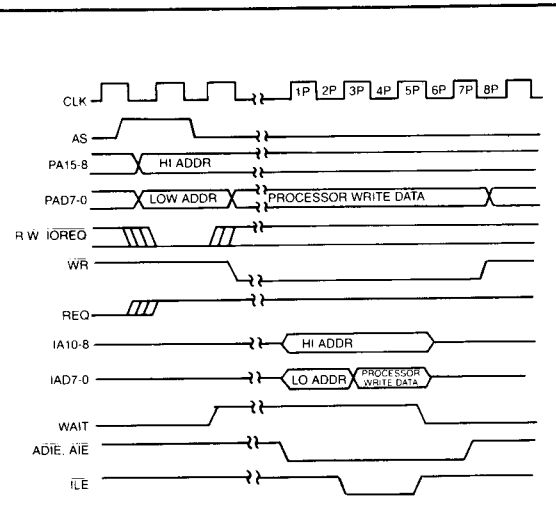


FIGURE 8—PROCESSOR WRITE COM 90C26

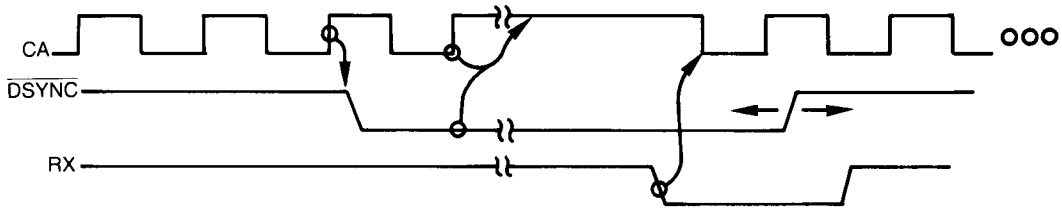


FIGURE 9—CA CLOCK GENERATOR TIMING

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 90C26 operation.

Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 90C26 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 4 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 4, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 90C26 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 90C26 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. It should be noted that for proper network operation, all COM 90C26's connected to the same network must have the same response time, idle time and reconfiguration time.

ET2	ET1	RESPONSE TIME (μs)	IDLE TIME (μS)	RECONFIGURATION TIME (ms)
1	1	78	86	840
1	0	285	316	1680
0	1	563	624	1680
0	0	1130	1237	1680

TABLE 1
COM 90C26 INTERNAL PROGRAMMABLE TIMER VALUES

I/O COMMANDS

I/O commands are executed by activating the $\overline{\text{IOREQ}}$ input. The COM 90C26 will interrogate the AD0 and the R/$\overline{\text{W}}$ inputs at the AS time to execute commands according to the following table:

$\overline{\text{IOREQ}}$	AD0	R/$\overline{\text{W}}$	FUNCTION
low	low	low	write interrupt mask
low	low	high	read status register
low	high	low	write COM 90C26 command
low	high	high	reserved for future use

READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 90C26 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 90C26 has received an active signal on the $\overline{POR}$ input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

WRITE INTERRUPT MASK

The COM 90C26 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	XXX	XXX	XXX	XXX	RECON TIMER	XXX	TRANSMITTER AVAILABLE

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

WRITE COM 90C26 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

WRITTEN DATA	COMMAND
00000000	reserved for future use
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 90C26 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 90C26 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 90C26 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "1". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 90C26 has received an acknowledgement from the destination COM 90C26. This acknowledgement is strictly hardware level which is sent by the receiving COM 90C26 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM 90C26 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 90C26 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If c is a logic "1", the COM 90C26 will handle short as well as long packets. If c is a logic "0", the COM 90C26 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "1", the RECON status flag is cleared.

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... V_{CC} +0.3V
Maximum V_{CC} ..... +7V
Negative Voltage on any pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	input low voltage	−0.3		0.8	V	
V_{IH1}	input high voltage 1	2.2		V_{CC}	V	except CA and CLK
V_{IH2}	input high voltage 2	V_{CC}−1.0		6.5	V	for CA or CLK
V_{OL1}	output low voltage 1			0.4	V	I_{OL} = 1.6ma
V_{OL2}	output low voltage 2			0.5	V	I_{OL} = 2.0ma
V_{OH1}	output high voltage	2.4			V	except $\overline{Tx}$ and $\overline{DSYNC}$ I_{OH} = −100μA
V_{OH2}	output high voltage	3.2			V	$\overline{Tx}$ and $\overline{DSYNC}$ only I_{OH} = −100μA
I_L	input leakage current			±10	μA	
C_{IN}	input capacitance			20	pf	
C_{DB}	data bus capacitance			50	pf	
C_L	all other capacitance			30	pf	
I_{CC}	power supply current		16		ma	

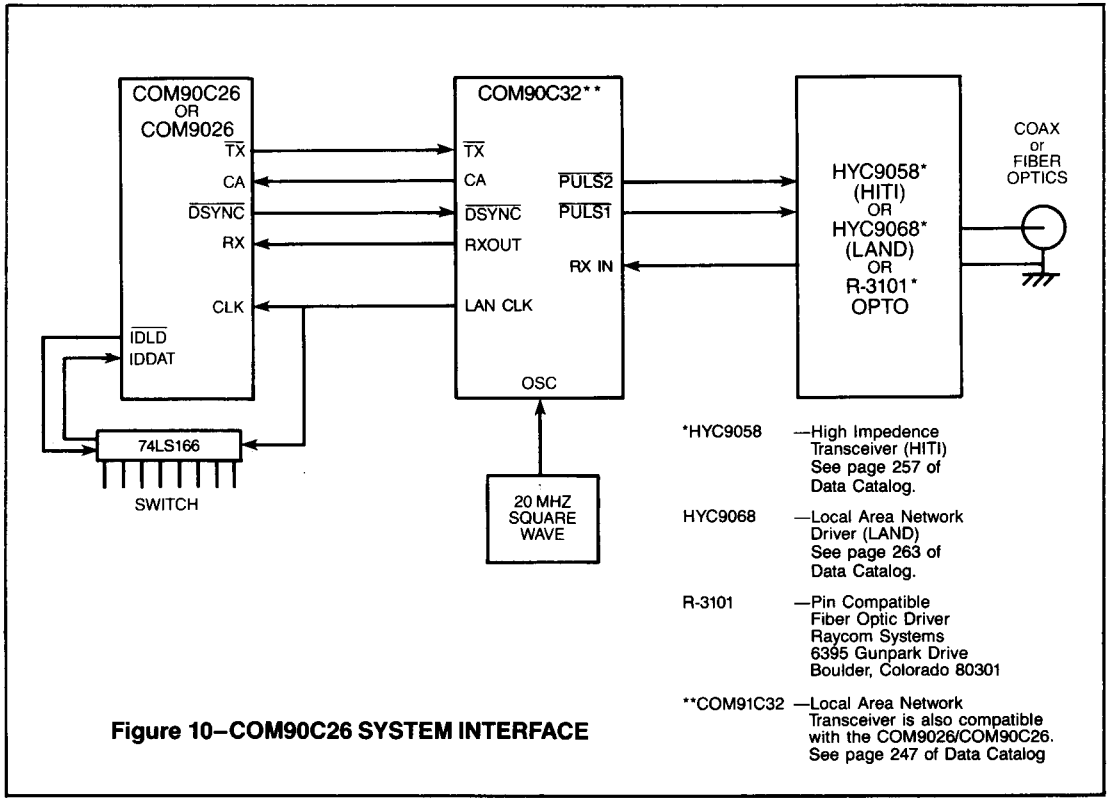


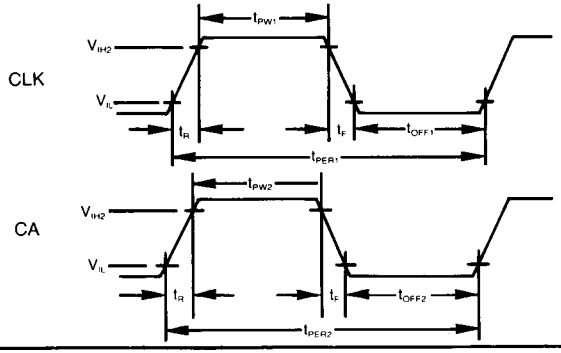
Figure 10–COM90C26 SYSTEM INTERFACE

AC ELECTRICAL CHARACTERISTICS ($T_A = 0°$ to 70°C, $V_{CC} = 5.0V \pm 5\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{PW1}	CLK pulse width	65			ns	
t_{PER1}	CLK period	190	200	600	ns	
t_{OFF1}	CLK off time	65			ns	
t_{PW2}	CA pulse width	60			ns	
t_{PER2}	CA period	190			ns	
t_{OFF2}	CA off time	60	100	300	ns	
t_R	CLK, CA rise time			20	ns	
t_F	CLK, CA fall time			20	ns	
t_1	width of addr. strobe	50		400	ns	
t_2	REQ output delay	0		100	ns	
t_3	WAIT assertion delay	0		200	ns	
t_4	delay to rising edge of processor cycle	t_P		$2t_P + 100$	ns	$t_P = t_{PER1}$
t_5	data hold into COM 9026	80			ns	
t_6	setup COM 9026 data out	60			ns	
t_7	$\overline{WE}$ delay from CLK	0		100	ns	
t_8	$\overline{TX}$ on delay from CA falling edge	10		150	ns	
t_9	$\overline{TX}$ off delay from CA falling edge	10		150	ns	
t_{10}	AS period	7/2 t_P			ns	$t_P = t_{PER2}$
t_{11}	$\overline{DSYNC}$ delay from CA rising edge	10		150	ns	
t_{12}	delay to wait off	20		100	ns	
t_{13}	$\overline{DWR}$ setup time	50			ns	
t_{14}	$\overline{ILE}$ delay from CLK	10		100	ns	
t_{15}	processor addr. setup from $\overline{ADIE}$,			50	ns	
t_{16}	processor command setup time	125			ns	
t_{17}	addr. enable setup time to $\overline{L}$	50			ns	
t_{18}	addr. hold time from $\overline{L}$	50			ns	
t_{19}	strobe and data hold for read	20			ns	
t_{20}	AD bus HI impedance to $\overline{OE}$s	0			ns	
t_{21}	delay of $\overline{IDLD}$ from CLK rising edge	0		120	ns	
t_{22}	delay of IDDAT from CLK rising edge	0		50	ns	
t_{23}	off delay from CLK rising edge	0		100	ns	
t_{24}	addr. to RAM data valid			300	ns	
t_{25}	$\overline{OE}$ setup to WAIT falling edge	140			ns	
t_{26}	strobe & data hold for write	50			ns	
t_{27}	addr. enable setup to WAIT	300			ns	
t_{28}	$\overline{ADIE}$ to $\overline{OE}$ delay	40			ns	
t_{29}	COM 9026 write data hold time	80			ns	
t_{30}	$\overline{OE}$ to RAM data valid	0		140	ns	
t_{31}	status setup to AS falling edge	50			ns	
t_{32}	status hold from AS falling edge	50			ns	
t_{33}	RX setup to CA rising edge	80			ns	
t_{34}	RX hold time from CA rising edge	30			ns	
t_{35}	$\overline{POR}$ active time	100			us	after V_{CC} has been stable for time t_{35}, the minimum $\overline{POR}$ active time is 10 cycles of CLK.

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

FIGURE 11— CLK, CA AC CHARACTERISTICS



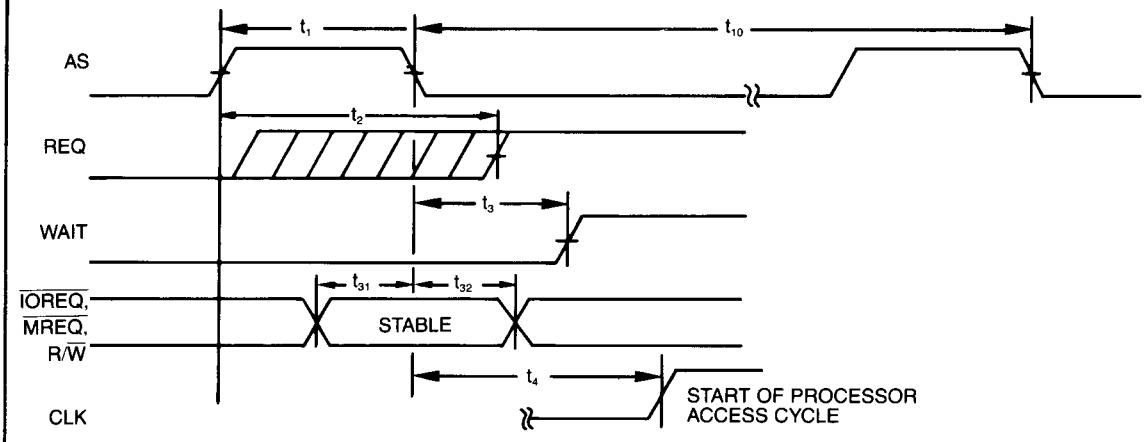


FIGURE 12—PROCESSOR ACCESS SYNCHRONIZATION

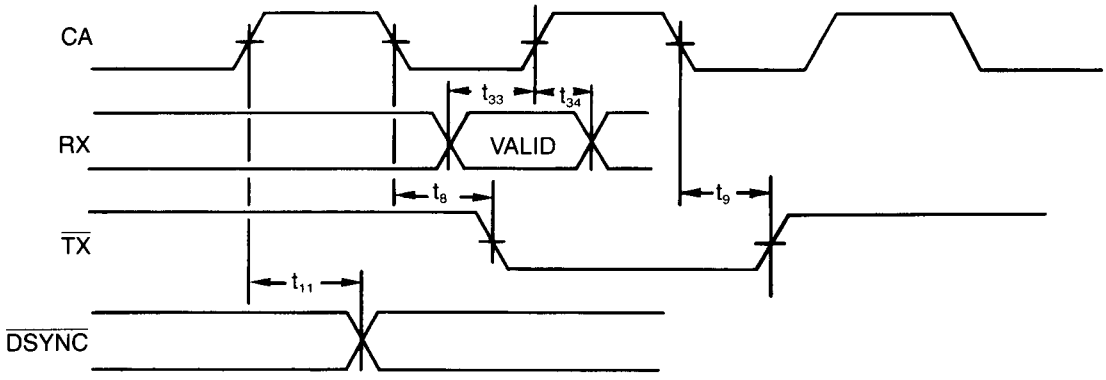


FIGURE 13—TRANSMIT AND RECEIVE TIMING

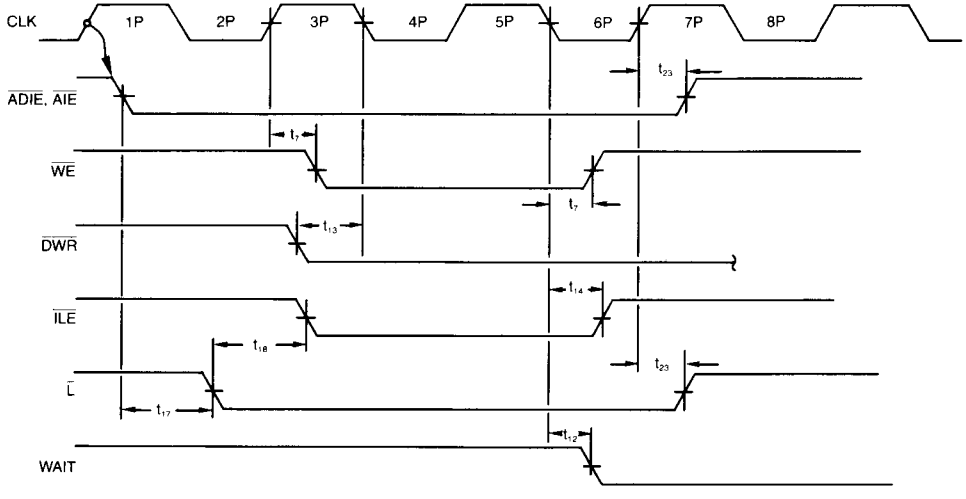


FIGURE 14—PROCESSOR WRITE RAM AC TIMING

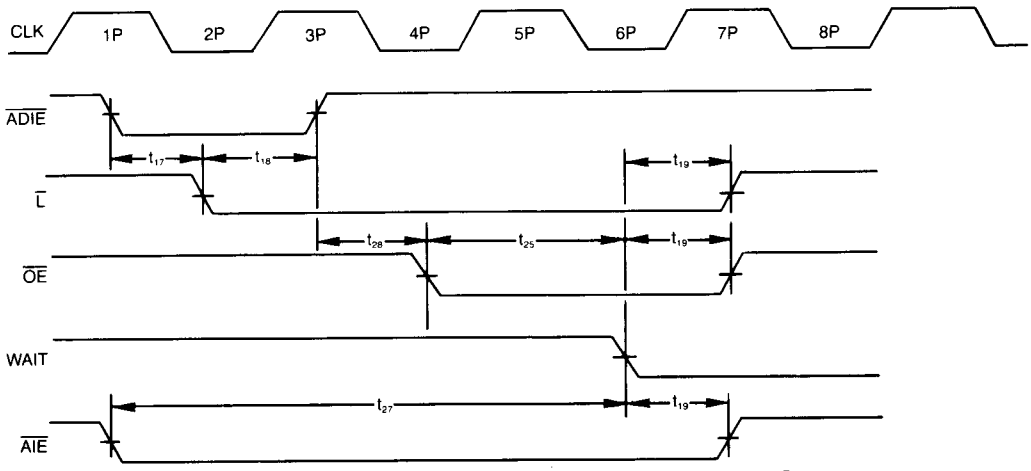


FIGURE 15—PROCESSOR READ RAM AC TIMING

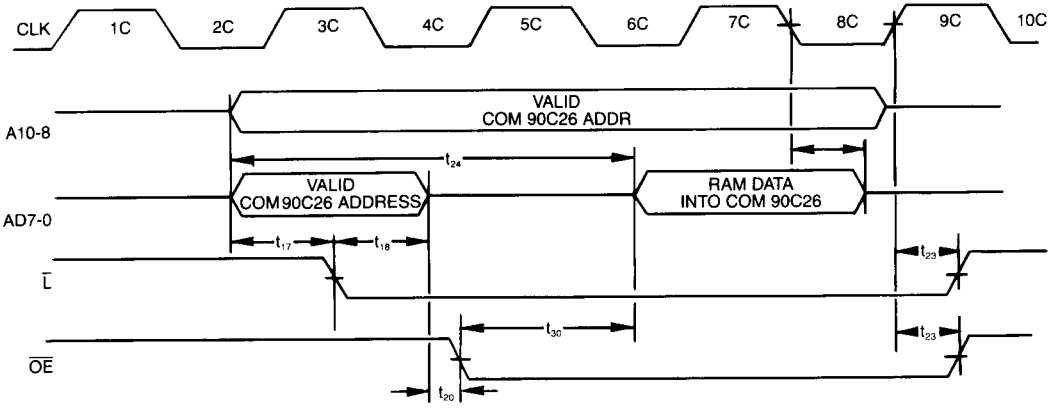


FIGURE 16—COM 90C26 READ RAM AC TIMING

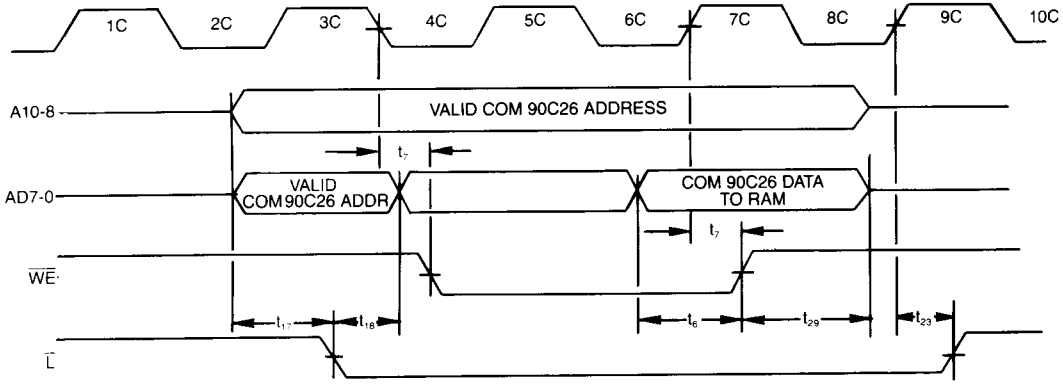


FIGURE 17—COM90C26 WRITE RAM AC TIMING

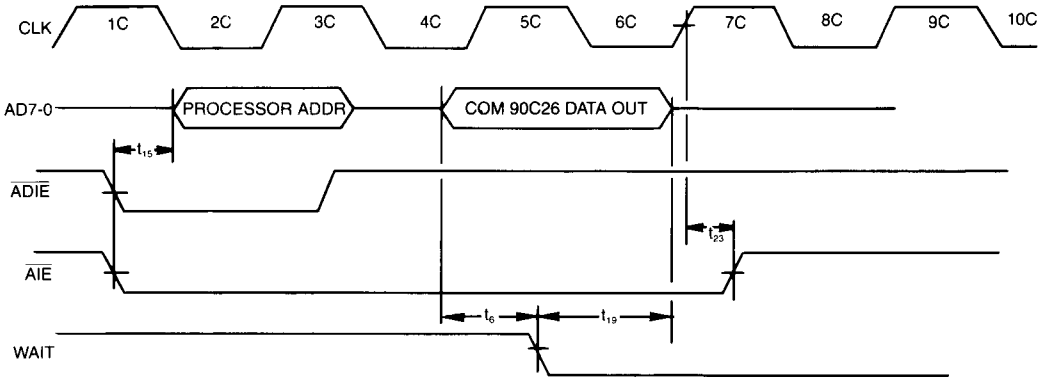


FIGURE 18—PROCESSOR READ COM 90C26 AC TIMING

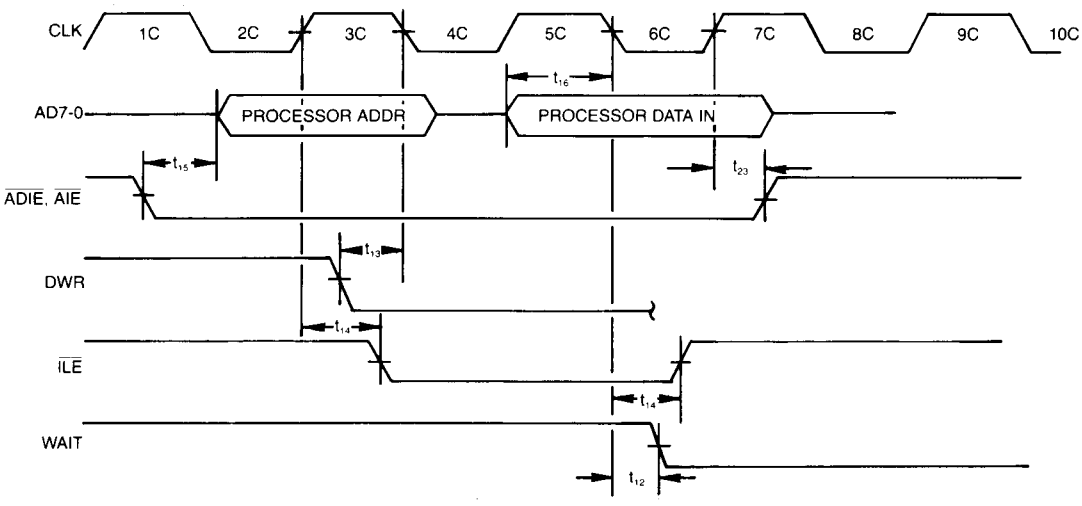


FIGURE 19—PROCESSOR WRITE COM 90C26 AC TIMING

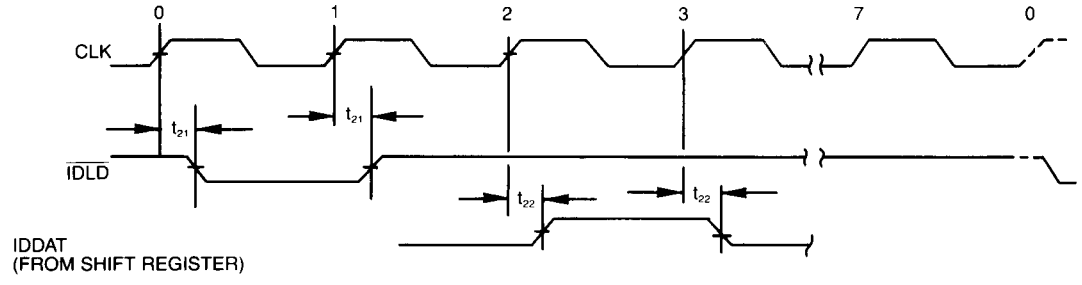


FIGURE 20—ID INPUT AC TIMING