

2/3-Port EtherCAT® Device Controller with Integrated PHYs & SAM E53J 32-bit ARM® Cortex®-M4F MCU

Highlights

- 2/3-port EtherCAT® device controller with 8 Fieldbus Memory Management Units (FMMUs) and 8 SyncManagers
- Integrated ARM Cortex-M4F MCU with 1 Msps 12-bit ADC, SQSPI, USB LS/Fs Host and Device, Ethernet MAC, and PTC
- Integrated EtherCAT PHYs with HP Auto-MDIX
- EtherCAT cable diagnostic support

Target Applications

- Motor Motion Control
- Process/Factory Automation
- Communication Modules, Interface Cards
- Sensors
- Hydraulic & Pneumatic Valve Systems
- Operator Interfaces

Key Benefits

- **Microchip SAM E53J ARM Cortex-M4F**
 - Memories
 - 1 MB/512 KB/256 KB in-system programmable flash
 - 256 KB /192 KB/128 KB SRAM main memory
 - System
 - Power-on Reset (POR) and Brown-out detection
 - Internal and external clock options
 - Power Supply
 - Idle, Standby, Hibernate, Backup, and Off sleep modes
 - SleepWalking peripherals
 - Embedded Buck/LDO regulator
 - Peripherals
 - 32-channel Direct Memory Access Controller (DMAC)
 - SD/MMC Host Controller (SDHC)
 - Quad I/O Serial Peripheral Interface (QSPI)
 - 10/100 Ethernet MAC with 1588 PTP/TSU
 - Full-Speed USB 2.0 interface
 - 32-channel Event System
 - Dual 1 MSPS 12-bit ADCs and DACs
 - Peripheral Touch Controller (PTC)

• Microchip LAN9253 2/3-Port EtherCAT Device

- Integrated 100Mbps Ethernet transceivers
 - Compliant with IEEE 802.3/802.3u (Fast Ethernet)
 - Signal Quality Index diagnostics
 - Loop-back modes
 - Automatic polarity detection and correction
 - HP Auto-MDIX
 - Compatible with EtherCAT P
- EtherCAT device controller
 - Supports 8 FMMUs
 - Supports 8 SyncManagers
 - Distributed clock support allows synchronization with other EtherCAT devices
 - 8K bytes of DPRAM
- Host Bus Interface
 - SPI / SQI (Quad SPI) support at up to 60MHz
- 3rd port for flexible network configurations
- Comprehensive power management features
 - 3 power-down levels
 - Wake on link status change (energy detect)
 - Magic packet wakeup, Wake on LAN (WoL), wake on broadcast, wake on perfect DA
 - Wakeup indicator event signal
- Power and I/O
 - Integrated power-on reset circuit
 - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
 - JEDEC Class 3A ESD performance
 - Single 3.3V power supply (integrated 1.2V regulator)
 - Option for external power supplies
 - Local host allowed to enter sleep mode until addressed by EtherCAT Host
- Additional Features
 - EEPROM emulation
 - Enhanced EtherCAT cycle time
 - Transformer-less link support
 - Multifunction GPIOs
 - Ability to use low cost 25MHz crystal for reduced BOM
 - 25MHz clock output for reference clock daisy chaining

• Packaging

- Pb-free RoHS compliant 128-pin TQFP (14mm x 14mm, 0.4mm pitch)

• Environmental

- Commercial (0°C to +70°C)
- Industrial (-40°C to +85°C)
- Extended industrial (-40°C to +105°C)

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1.0 PREFACE

1.1 References

- Microchip LAN9253 Data Sheet: <https://www.microchip.com/wwwproducts/en/LAN9253>
- Microchip SAM E53J Data Sheet: <http://ww1.microchip.com/downloads/en/DeviceDoc/60001507E.pdf>

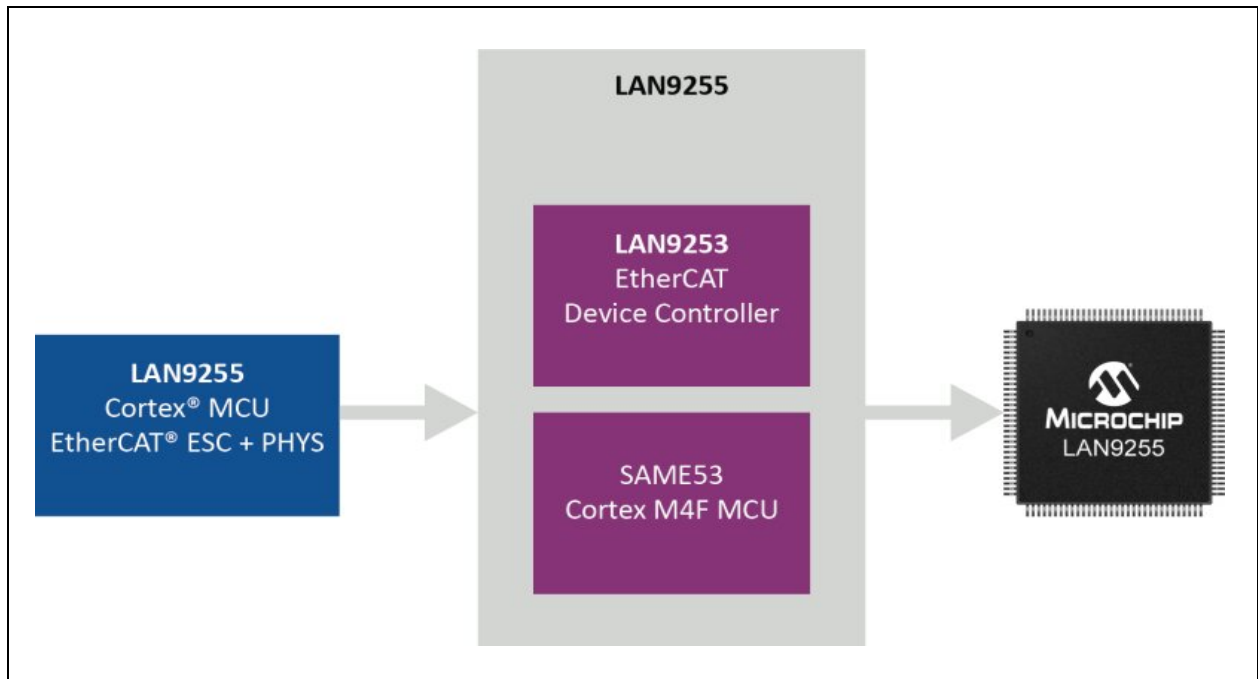
2.0 INTRODUCTION

The LAN9255 is a System-In-Package (SIP) design that combines the Microchip LAN9253 2/3-port EtherCAT device controller with dual integrated Ethernet PHYs and the Microchip SAM E53J ARM Cortex-M4F MCU into a single 128-pin TQFP package.

The LAN9255 is available in commercial (0°C to +70°C), industrial (-40°C to +85°C), and extended industrial (-40°C to +105°C) temperature ranges. A block diagram of the LAN9255 is provided in [Figure 2-1](#).

Details on each integrated device (LAN9253 & SAM E53J) can be referenced via their respective data sheets, as outlined in [Section 1.1, References](#). Any device specific details outside of those detailed in the respective data sheets are provided in [Section 3.0, LAN9255 Device Specifications](#). Pinout information for the LAN9255 is detailed in [Section 4.0, Pin Configuration](#).

FIGURE 2-1: LAN9255 BLOCK DIAGRAM



LAN9255

3.0 LAN9255 DEVICE SPECIFICATIONS

This section details device specifications that are unique to the LAN9255 and/or supersede those included in the LAN9253 and SAM E53J data sheets.

3.1 Optimal Interfacing between LAN9253 and SAM E53J

The following guidelines will provide optimal interfacing between the internal LAN9253 and SAM E53J die.

- The following connections are required between die for SPI/QSPI operation:

TABLE 3-1: SPI/QSPI CONNECTIONS

SPI Function	LAN9253 Pins	SAM E53J Pins
SCK	41	40
SCS#	101	42
SIO0	38	33
SIO1	26	34
SIO2	24	35
SIO3	71	36

- ESC EEPROM connected to the LAN9253 is optional
- Refer to the LAN9253 Data Sheet for information on configuration straps required to enable EEPROM emulation
- The 25MHz clock from the LAN9253 may be optionally used to feed the SAM E53J

3.2 Optimal EtherCAT Interfacing

- The EtherCAT RUN and EtherCAT ERROR LEDs can be used. Refer to the LAN9253 Data Sheet for additional information.

3.2.1 IMPLEMENTING ETHERNET

TABLE 3-2: RMII INTERFACE

RMII Function	Pin Name	LAN9255 Pin Number
TXEN	PA17	68
TXD0	PA18	69
TXD1	PA19	73
RXDV	PA16	67
RXD0	PA13	62
RXD1	PA12	61
RXER	PA15	64
MDIO	PA21	87
MDC	PA20	84

3.3 Device ID

- The LAN9255 provides a dedicated device ID returned by the integrated SAM E53J. This enables developers to distinguish between discrete SAM E53J implementations and those with the LAN9255. A list of the Device IDs for the various ordering options is detailed in [Table 3-3](#).
- The integrated LAN9253 returns its normal device ID.

TABLE 3-3: DEVICE ID

CPP Number	Temp/MEM Size	UNG Part ID
LAN9255-V/ZMX020	105°C 1024k Memory	0x61830355
LAN9255-I/ZMX020	85°C 1024k Memory	0x61830355
LAN9255/ZMX020	70°C 1024k Memory	0x61830355
LAN9255-V/ZMX019	105°C 512k Memory	0x61830356
LAN9255-I/ZMX019	85°C 512k Memory	0x61830356
LAN9255/ZMX019	70°C 512k Memory	0x61830356
LAN9255-V/ZMX018	105°C 256k Memory	0x61830357
LAN9255-I/ZMX018	85°C 256k Memory	0x61830357
LAN9255/ZMX018	70°C 256k Memory	0x61830357

3.4 Extended Temperature Operation

As also noted in the LAN9253 Data Sheet, for the extended industrial temperature range option, the following restrictions apply:

- Internal regulator disabled
- 2.5V (typical) Ethernet magnetics voltage required

Table 4-1 details the pin assignments in table format. As shown, select pin functions may change based on the device's mode of operation. For modes where a specific pin has no function, the table cell will be marked with "-". The source die and original source die pin number for each signal is also provided.

TABLE 4-1: LAN9255 PIN ASSIGNMENTS

LAN9255 Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name	Digital I/O Mode Pin Name	Source Die	Source Die Pin
1	OSCO					LAN9253	2
2	PB03					SAM E53J	64
3	PA00					SAM E53J	1
4	OSCVDD12					LAN9253	3
5	PA01					SAM E53J	2
6	OSCVSS					LAN9253	4
7	VDD33					LAN9253	5
8	PA02					SAM E53J	3
9	PA03					SAM E53J	4
10	PB04					SAM E53J	5
11	PB05					SAM E53J	6
12	VDDCR					LAN9253	6
13	REG_EN					LAN9253	7
14	CLK_25/CLK_25_EN/XTAL_MODE					LAN9253	8
15	GNDANA					SAM E53J	7
16	VDDANA					SAM E53J	8
17	ERRLED/PME/100FD_B/LEDPOL4			ERRLED/PME/LEDPOL4	ERRLED/100FD_B/LEDPOL4	LAN9253	9
18	WAIT_ACK/PME	WAIT_ACK/PME/EE_EMUL_SPI3		LATCH0		LAN9253	10
19	PB06					SAM E53J	9
20	PB07					SAM E53J	10
21	RST#					LAN9253	11
22	PB08					SAM E53J	11
23	PB09					SAM E53J	12
24	D2	AD2	SIO2/EE_EMUL_SPI0		SOF	LAN9253	12
25	PA04					SAM E53J	13
26	D1	AD1	SO/SIO1		EOF	LAN9253	13
27	PA05					SAM E53J	14
28	PA06					SAM E53J	15
29	VDDIO_J					LAN9253	14
30	PA07					SAM E53J	16

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TABLE 4-1: LAN9255 PIN ASSIGNMENTS (CONTINUED)

LAN9255 Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name	Digital I/O Mode Pin Name	Source Die	Source Die Pin
31	D14	AD14	GPI8/GPO8	MII_TXD3/ <u>TX_SHIFT1</u>	DIGIO8	LAN9253	15
32	D13	AD13	GPI7/GPO7	MII_TXD2/ <u>TX_SHIFT0</u>	DIGIO7	LAN9253	16
33	PA08					SAM E53J	17
34	PA09					SAM E53J	18
35	PA10					SAM E53J	19
36	PA11					SAM E53J	20
37	VDDIOB					SAM E53J	21
38	D0	AD0	SI/SIO0		WD_STATE	LAN9253	17
39	SYNC1/LATCH1/PME				SYNC1/ LATCH1	LAN9253	18
40	PB10					SAM E53J	23
41	D9	AD9	SCK		LATCH_IN	LAN9253	19
42	PB11					SAM E53J	24
43	PB12					SAM E53J	25
44	PB13					SAM E53J	26
45	VDDIO_J					LAN9253	20
46	PB14					SAM E53J	27
47	PB15					SAM E53J	28
48	NC					N/A	N/A
49	D12	AD12	GPI6/GPO6	MII_TXD1/ <u>100FD_B</u>	DIGIO6	LAN9253	21
50	D11	AD11	GPI5/GPO5	MII_TXD0/ <u>100FD_A</u>	DIGIO5	LAN9253	22
51	D10	AD10	GPI4/GPO4	MII_TXEN	DIGIO4	LAN9253	23
52	VDDCR					LAN9253	24
53	A1	ALELO	-	MII_CLK25/ <u>EE_EMUL_S</u> <u>PI2</u>	OE_EXT	LAN9253	25
54	A3	BE0	GPI11/GPO11	MII_RXDV	DIGIO11	LAN9253	26
55	A4	BE1	GPI12/ GPO12	MII_RXD0	DIGIO12	LAN9253	27
56	CS		GPI13/ GPO13	MII_RXD1	DIGIO13	LAN9253	28

TABLE 4-1: LAN9255 PIN ASSIGNMENTS (CONTINUED)

LAN9255 Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name	Digital I/O Mode Pin Name	Source Die	Source Die Pin
57	A2	ALEHI/ <u>EE_EMUL_A</u> <u>LELO_POL</u>	GPI10/ GPO10	LINKACT- LED2/ <u>MII_LINK-</u> <u>POL/LED-</u> <u>POL2</u>	DIGIO10	LAN9253	29
58	WR/ENB		GPI14/ GPO14	MII_RXD2	DIGIO14	LAN9253	30
59	RD/RD_WR		GPI15/ GPO15	MII_RXD3	DIGIO15	LAN9253	31
60	VDDIO_J					LAN9253	32
61	PA12					SAM E53J	29
62	PA13					SAM E53J	30
63	PA14					SAM E53J	31
64	PA15					SAM E53J	32
65	VDDIO_S					SAM E53J	34
66	A0/D15	AD15	GPI9/GPO9	MII_RXER	DIGIO9	LAN9253	33
67	PA16					SAM E53J	35
68	PA17					SAM E53J	36
69	PA18					SAM E53J	37
70	SYNC0/LATCH0/PME				SYNC0/ LATCH0	LAN9253	34
71	D3	AD3	<u>SIO3/EE_EMUL_SPI</u>		WD_TRIG	LAN9253	35
72	D6	AD6	GPI0/GPO0	MII_RXCLK	DIGIO0	LAN9253	36
73	PA19					SAM E53J	38
74	VDDIO_J					LAN9253	37
75	NC					N/A	N/A
76	VDDCR					LAN9253	38
77	PB16					SAM E53J	39
78	D7	AD7	GPI1/GPO1	MII_MDC	DIGIO1	LAN9253	39
79	PB17					SAM E53J	40
80	D8	AD8	GPI2/GPO2	MII_MDIO	DIGIO2	LAN9253	40
81	TESTMODE					LAN9253	41
82	<u>EESDA/TMS/EE_EMUL1</u>				EESDA/TMS	LAN9253	42
83	<u>EESCL/TCK/EE_EMUL2</u>				EESCL/TCK	LAN9253	43
84	PA20					SAM E53J	41
85	NC					N/A	N/A
86	NC					N/A	N/A

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TABLE 4-1: LAN9255 PIN ASSIGNMENTS (CONTINUED)

LAN9255 Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name	Digital I/O Mode Pin Name	Source Die	Source Die Pin
87	PA21					SAM E53J	42
88	IRQ				LATCH1	LAN9253	44
89	RUNLED/STATE_RUNLED/ <u>E2PSIZE/EE_EMUL0/LEDPOL3</u>				RUNLED/ STATE_RUN- LED/ <u>E2PSIZE/</u> <u>LEDPOL3</u>	LAN9253	45
90	LINKACTLED1/TDI/ <u>CHIP_MODE1/LEDPOL1</u>					LAN9253	46
91	PA22					SAM E53J	43
92	PA23					SAM E53J	44
93	PA24					SAM E53J	45
94	VDDIO_J					LAN9253	47
95	LINKACTLED0/TDO/ <u>CHIP_MODE0/100FD_A/LEDPOL0</u>		LINKACT- LED0/TDO/ <u>CHIP -</u> <u>MODE0/</u> <u>LEDPOL0</u>	LINKACT- LED0/TDO/ <u>CHIP -</u> <u>MODE0/</u> <u>100FD_A/</u> <u>LEDPOL0</u>	LAN9253	48	
96	PA25					SAM E53J	46
97	VDDIO_S					SAM E53J	48
98	PB22					SAM E53J	49
99	PB23					SAM E53J	50
100	D4	AD4	GPI3/GPO3	MII_LINK	DIGIO3	LAN9253	49
101	D5	AD5	SCS#		OUTVALID	LAN9253	50
102	VDD33TXRX1					LAN9253	51
103	TXNA					LAN9253	52
104	TXPA					LAN9253	53
105	RXNA					LAN9253	54
106	RXPA					LAN9253	55
107	PA27					SAM E53J	51
108	RESETN_E53					SAM E53J	52
109	VDDCORE					SAM E53J	53
110	VDD12TX1					LAN9253	56
111	RBIAS					LAN9253	57
112	VDD33BIAS					LAN9253	58
113	VDD12TX2					LAN9253	59
114	VSW					SAM E53J	55
115	RXPB					LAN9253	60

TABLE 4-1: LAN9255 PIN ASSIGNMENTS (CONTINUED)

LAN9255 Pin Number	HBI Indexed Mode Pin Name	HBI Multiplexed Mode Pin Name	SPI with GPIO Mode Pin Name	SPI with MII Mode Pin Name	Digital I/O Mode Pin Name	Source Die	Source Die Pin
116	RXNB					LAN9253	61
117	VDDIO_S					SAM E53J	56
118	TXPB					LAN9253	62
119	TXNB					LAN9253	63
120	PA30					SAM E53J	57
121	PA31					SAM E53J	58
122	PB30					SAM E53J	59
123	PB31					SAM E53J	60
124	VDD33TXRX2					LAN9253	64
125	PB00					SAM E53J	61
126	PB01					SAM E53J	62
127	PB02					SAM E53J	63
128	OSCI					LAN9253	1
Exposed Pad	VSS					LAN9253	ePad
						SAM E53J	22,33,47,54

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4.1.1 INTERNAL PIN MAPPING

Figure 4-2 and Figure 4-3 detail the LAN9255 internal pin mappings between the integrated LAN9253 and SAM E53J, respectively.

FIGURE 4-2: LAN9253 INTERNAL PIN MAPPING

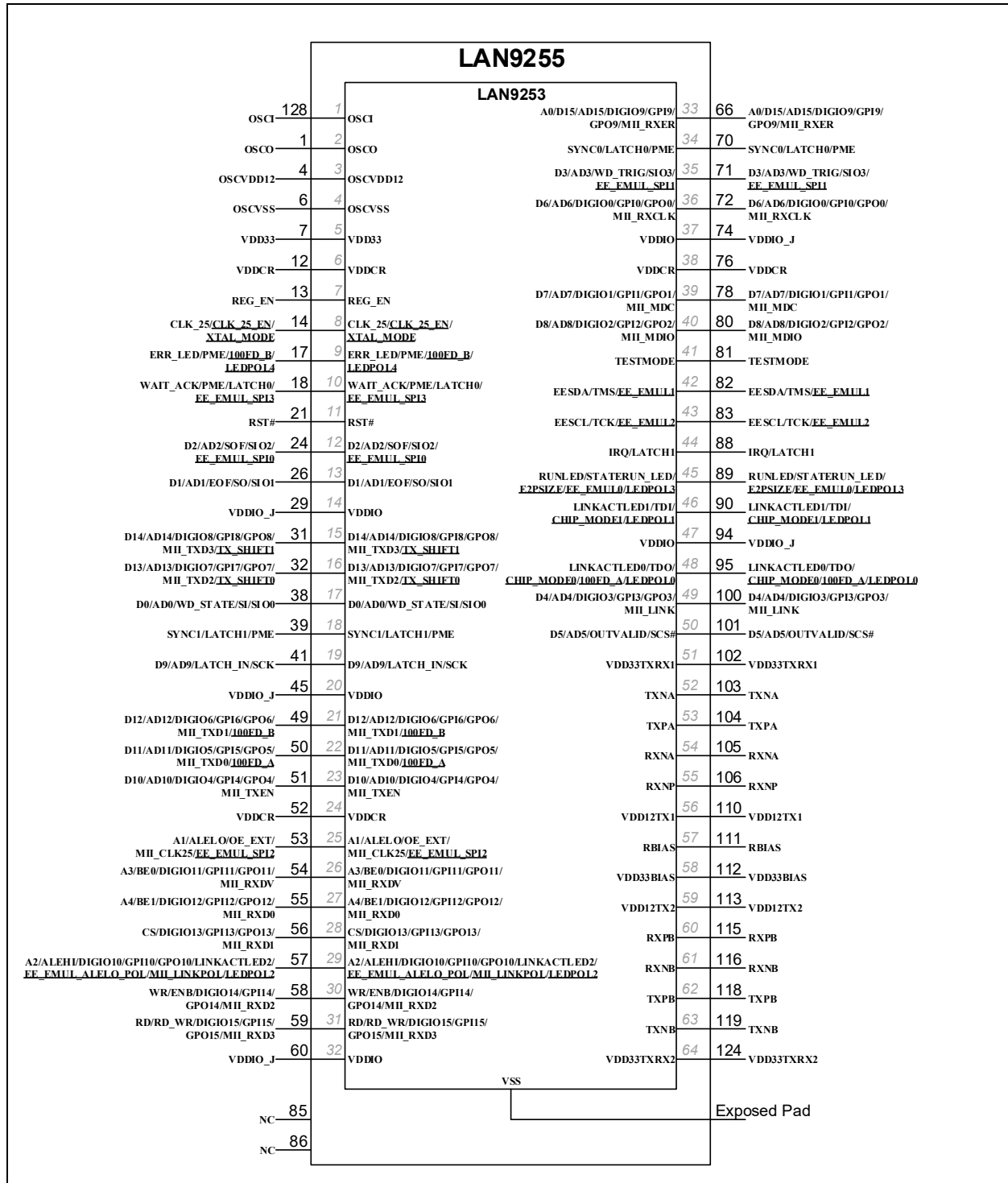
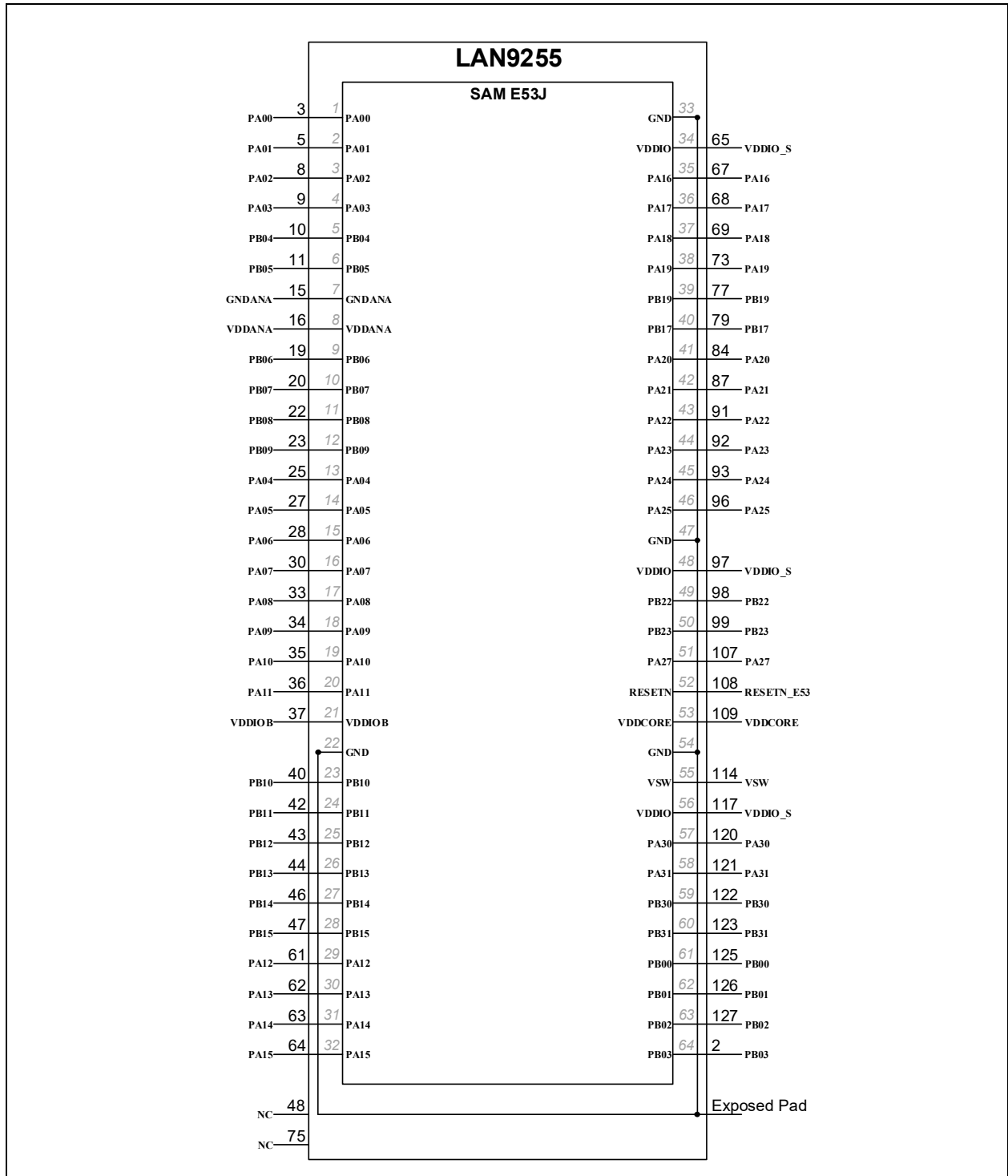


FIGURE 4-3: SAM E53J INTERNAL PIN MAPPING



LAN9255

5.0 PACKAGE INFORMATION

Note: For the most current package drawings, see the Microchip Packaging Specification at <http://www.microchip.com/packaging>.

FIGURE 5-1: 128-TQFP PACKAGE (DRAWING)

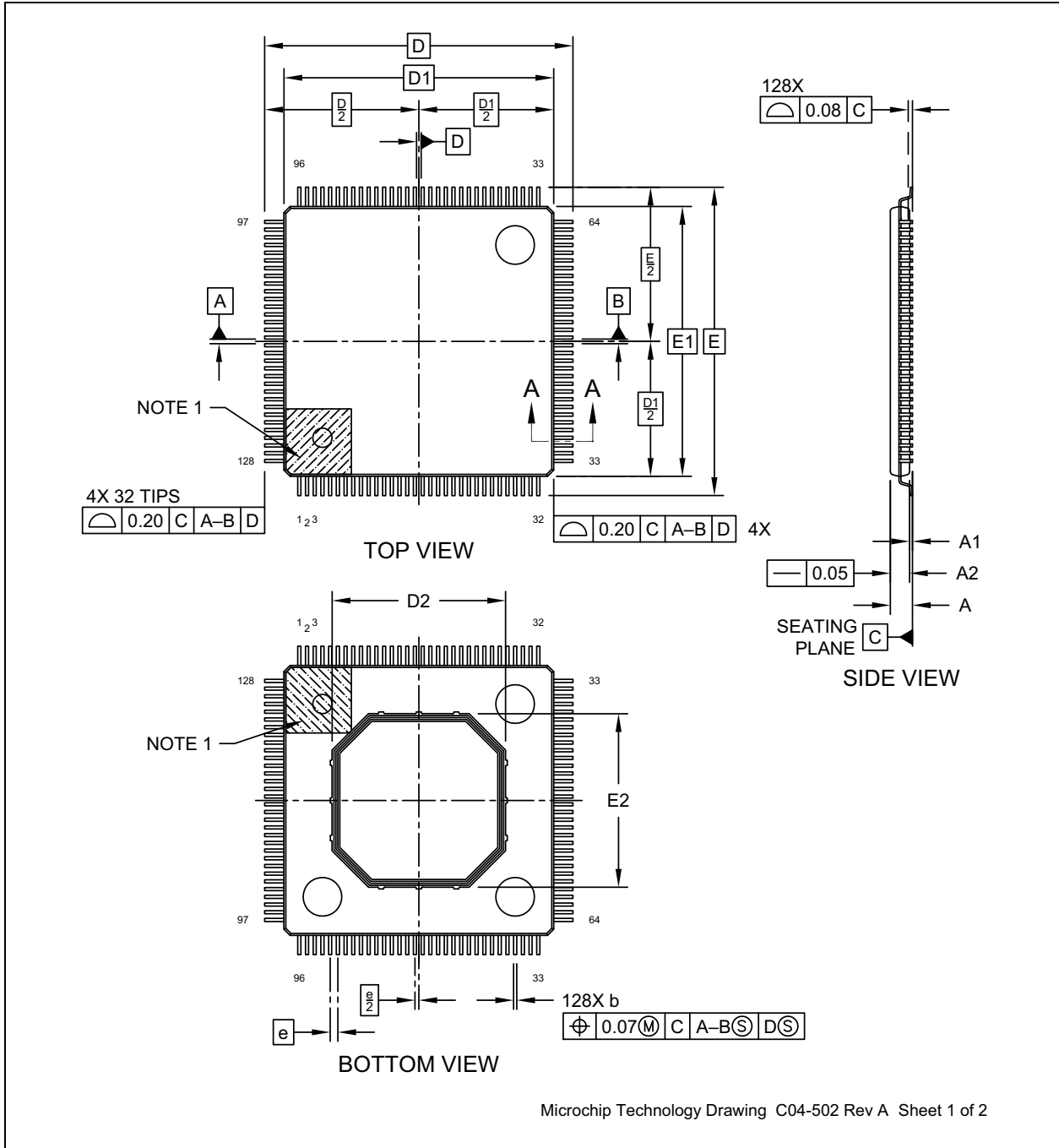
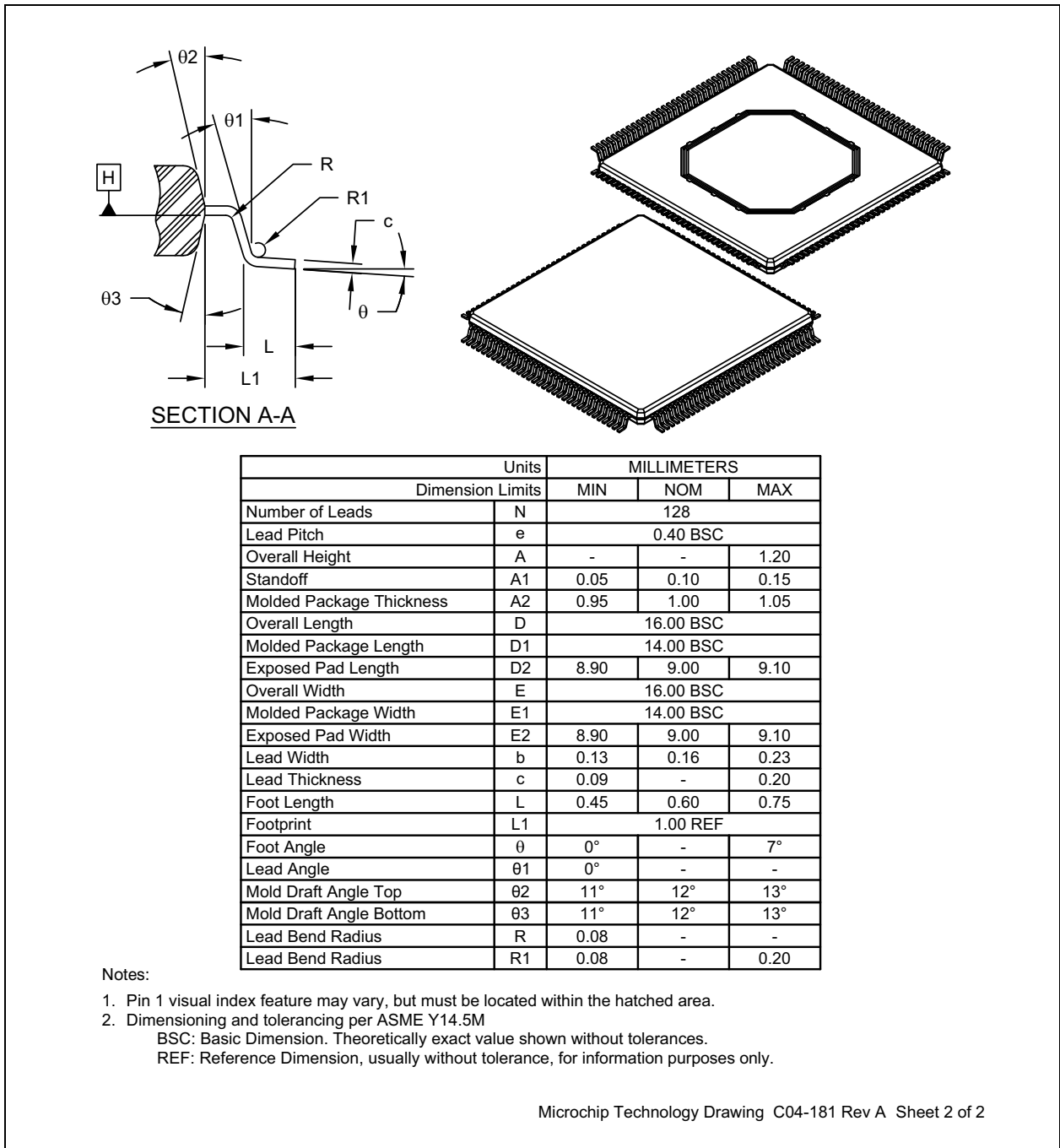
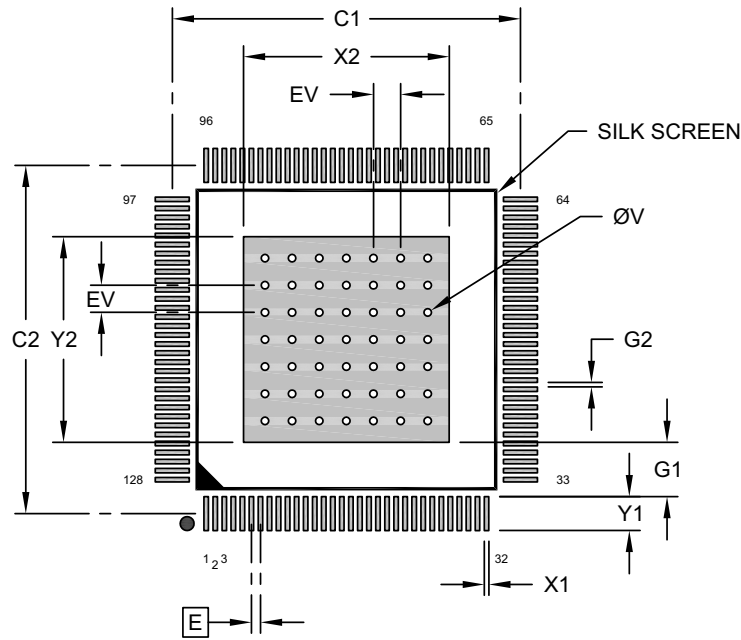


FIGURE 5-2: 128-TQFP PACKAGE (DIMENSIONS)



LAN9255

FIGURE 5-3: 128-TQFP PACKAGE (LAND PATTERN)



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	X2			9.10
Optional Center Pad Length	Y2			9.10
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X128)	X1			0.20
Contact Pad Length (X128)	Y1			1.50
Contact Pad to Center Pad (X128)	G1	2.40		
Contact Pad to Contact Pad (X124)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2502 Rev A

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level	Section/Figure/Entry	Correction
DS00003646B (04-09-21)		<ul style="list-style-type: none"> - Changed "EtherCAT Master" to "EtherCAT Host" in features - Title of Table 3-2 changed from "RGMII Interface" to "RMII Interface", first column heading changed from "RGMII Function" to "RMII Function" - Removed "slave" and replaced with "device" in Figure 2-1. - Added the following sentence to the end of the first bullet in Section 3.3 Device ID: "A list of the Device IDs for the various ordering options is detailed in Table 3-3, "Device ID" - Added Table 3-3, "Device ID" - Removed "Confidential - NDA Required" nomenclature from footer.
DS00003646A (09-15-20)	All	Initial Release

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	[X]	[-X]	/	XXX	XXX
Device	Tape and Reel Option	Temperature Range		Package	Mem. Cfg.
Device:	LAN9255				
Tape and Reel Option:	Blank = Standard packaging (Tray) T = Tape and Reel (Note 1)				
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial) V = -40°C to +105°C (Extended Industrial)				
Package:	ZMX = 128-pin TQFP (9.0mm ePad)				
Mem. Config:	018 = 256K Programmable Memory 019 = 512K Programmable Memory 020 = 1024K Programmable Memory				

Examples:
a) LAN9255/ZMX018 Standard Packaging (Tray), Commercial Temperature, 128-pin TQFP, 256K Memory
b) LAN9255-I/ZMX019 Standard Packaging (Tray) Industrial Temperature, 128-pin TQFP, 512K Memory
c) LAN9255-V/ZMX020 Standard Packaging (Tray) Extended Industrial Temperature, 128-pin TQFP, 1024K Memory
d) LAN9255T/ZMX018 Tape and Reel Commercial Temperature, 128-pin TQFP, 256K Memory
e) LAN9255T-I/ZMX019 Tape and Reel Industrial Temperature, 128-pin TQFP, 512K Memory
f) LAN9255T-V/ZMX020 Tape and Reel Extended Industrial Temperature, 128-pin TQFP, 1024K Memory

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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