



# AT17LV65<sup>(1)</sup>, AT17LV128<sup>(1)</sup>, AT17LV256, AT17LV512, AT17LV010, AT17LV002, AT17LV040

Note 1.  
AT17LV65 and AT17LV128  
are Not Recommended for  
New Designs (NRND) and  
are Replaced by AT17LV256.

## FPGA Configuration EEPROM Memory 3.3V and 5.0V System Support

### DATASHEET

#### Features

- EE Programmable Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
  - 65,536 x 1-bit<sup>(1)</sup>
  - 131,072 x 1-bit<sup>(1)</sup>
  - 262,144 x 1-bit
  - 524,288 x 1-bit
  - 1,048,576 x 1-bit
  - 2,097,152 x 1-bit
  - 4,194,304 x 1-bit
- Supports both 3.3V and 5.0V Operating Voltage Applications
- In-System Programmable (ISP) via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with the Atmel<sup>®</sup> AT6000, AT40K and AT94K Devices, Altera<sup>®</sup> FLEX<sup>®</sup>, APEX<sup>™</sup> Devices, ORCA<sup>®</sup>, Xilinx<sup>®</sup> XC3000, XC4000, XC5200, Spartan<sup>®</sup>, Virtex<sup>®</sup> FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density Arrays
- Very Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available in 6mm x 6mm x 1mm 8-lead LAP (Pin-compatible with 8-lead SOIC Package), 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC and 44-lead TQFP Packages
- Emulation of the Atmel AT24CXXX Serial EEPROMs
- Low-power Standby Mode
- High-reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 90 Years for Industrial Parts (at 85°C)
- Green (Pb/Halide-free/RoHS Compliant) Package Options Available

#### Description

The AT17LV FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory solution for Field Programmable Gate Arrays. The AT17LV devices are packaged in the 8-lead LAP, 8-lead PDIP, 8-lead SOIC, 20-lead PLCC, 20-lead SOIC and 44-lead TQFP options (Table 1). The AT17LV Configurators use a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function during programming. These devices also support a write protection mechanism within its programming mode.

The AT17LV configurators can be programmed with industry-standard programmers, the Atmel ATDH2200E Programming Kit, or the Atmel ATDH2225 ISP Cable.

**Table 1. AT17LV Packages**

| Package      | AT17LV65/128/256 <sup>(4)</sup> | AT17LV512/010                 | AT17LV002                     | AT17LV040      |
|--------------|---------------------------------|-------------------------------|-------------------------------|----------------|
| 8-lead LAP   | Yes                             | Yes                           | Yes                           | <sup>(3)</sup> |
| 8-lead PDIP  | Yes                             | Yes                           | —                             | —              |
| 8-lead SOIC  | Yes                             | Use 8-lead LAP <sup>(1)</sup> | Use 8-lead LAP <sup>(1)</sup> | <sup>(3)</sup> |
| 20-lead PLCC | Yes                             | Yes                           | Yes                           | —              |
| 20-lead SOIC | Yes <sup>(2)</sup>              | —                             | Yes <sup>(2)</sup>            | —              |
| 44-lead TQFP | —                               | —                             | Yes                           | Yes            |

- Notes:
1. The 8-lead LAP package has the same footprint as the 8-lead SOIC. Since an 8-lead SOIC package is not available for the AT17LV512/010/002 devices, it is possible to use an 8-lead LAP package instead.
  2. The pinout for the AT17LV65 (NRND), AT17LV128 (NRND), and AT17LV256 is not pin-for-pin compatible with the AT17LV512/010/002 devices.
  3. Refer to the AT17F datasheet which is available on the Atmel website.
  4. The AT17LV65 and AT17LV128 are not recommended for new designs (NRND).

# 1. Pin Configuration and Descriptions

Table 1-1. Pin Descriptions

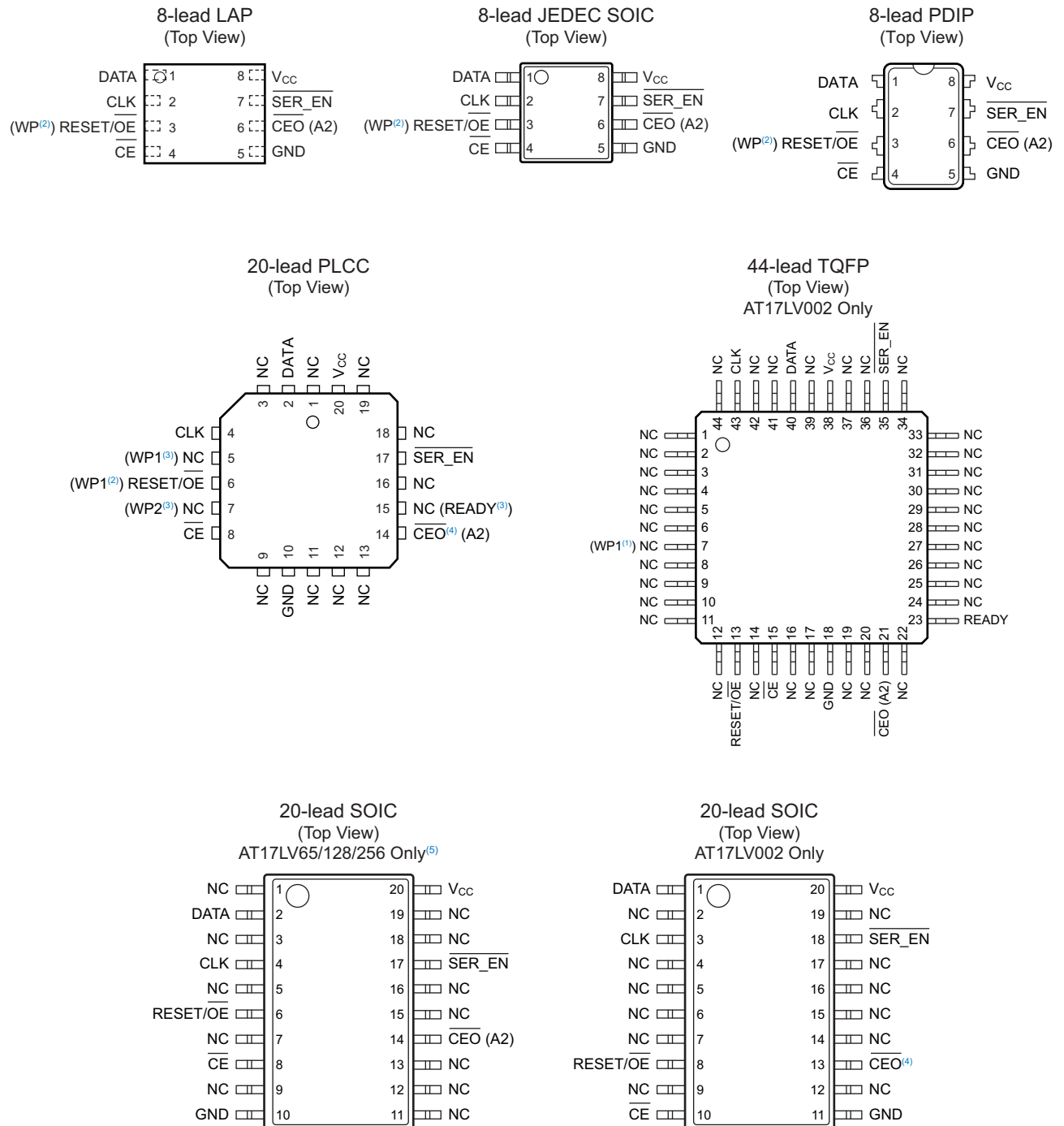
| Pin                         | Description   |
|-----------------------------|---|
| DATA                        | <b>Three-state Data Output for Configuration.</b> Open-collector bi-directional pin for programming.  |
| CLK                         | <b>Clock Input.</b> Used to increment the internal address and bit counter for reading and programming.   |
| WP1                         | <b>Write Protect (1).</b> Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on AT17LV512/010/002 devices.  |
| RESET/OE                    | <b>RESET (Active Low) / Output Enable (Active High)</b> when $\overline{\text{SER\_EN}}$ is High. A Low level on RESET/OE resets both the address and bit counters. A High level (with CE Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/OE or $\overline{\text{RESET/OE}}$ . For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{\text{RESET/OE}}$ .  |
| WP                          | <b>Write Protect Input</b> (when $\overline{\text{CE}}$ is Low) during programming only ( $\overline{\text{SER\_EN}}$ Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This pin is only available on the AT17LV65 (NRND), AT17LV128 (NRND), and the AT17LV256.  |
| WP2                         | <b>Write Protect (2).</b> Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on the AT17LV512/010.  |
| $\overline{\text{CE}}$      | <b>Chip Enable Input</b> (Active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. <i>Note that this pin will not enable/disable the device in the Two-Wire Serial Programming mode (<math>\overline{\text{SER\_EN}}</math> Low).</i>   |
| GND                         | <b>Ground.</b> A 0.2 $\mu$ F decoupling capacitor between $V_{\text{CC}}$ and GND is recommended.   |
| CEO                         | <b>Chip Enable Output</b> (Active Low). This output goes Low when the address counter has reached its maximum value. In a daisy chain of AT17LV devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is Low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire EEPROM is read again. This $\overline{\text{CEO}}$ feature is not available on the AT17LV65 (NRND). |
| A2                          | <b>Device Selection Input, A2.</b> This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.   |
| READY                       | <b>Open Collector Reset State Indicator.</b> Driven Low during power-up reset, released when power-up is complete. It is recommended to use a 4.7k $\Omega$ pull-up resistor when this pin is used.   |
| $\overline{\text{SER\_EN}}$ | <b>Serial Enable</b> must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to $V_{\text{CC}}$ .   |
| $V_{\text{CC}}$             | <b>Power Supply.</b> 3.3V ( $\pm 10\%$ ) and 5.0V ( $\pm 10\%$ ) power supply pin.  |

**Table 1-2. Pin Configurations**

| Name                          | I/O | AT17LV65/128/256 <sup>(2)</sup> |                 |                 | AT17LV512/010         |                 | AT17LV002     |                 |                 |                 | AT17LV040       |
|-------------------------------|-----|---------------------------------|-----------------|-----------------|-----------------------|-----------------|---------------|-----------------|-----------------|-----------------|-----------------|
|                               |     | 8-lead<br>DIP/LAP/<br>SOIC      | 20-lead<br>PLCC | 20-lead<br>SOIC | 8-lead<br>DIP/<br>LAP | 20-lead<br>PLCC | 8-lead<br>LAP | 20-lead<br>PLCC | 20-lead<br>SOIC | 44-lead<br>TQFP | 44-lead<br>TQFP |
| DATA                          | I/O | 1                               | 2               | 2               | 1                     | 2               | 1             | 2               | 1               | 40              | 40              |
| CLK                           | I   | 2                               | 4               | 4               | 2                     | 4               | 2             | 4               | 3               | 43              | 43              |
| WP1                           | I   | –                               | –               | –               | –                     | 5               | –             | 5               | –               | 7               | –               |
| $\overline{\text{RESET/OE}}$  | I   | 3                               | 6               | 6               | 3                     | 6               | 3             | 6               | 8               | 13              | 13              |
| WP2                           | I   | –                               | –               | –               | –                     | 7               | –             | 7               | –               | –               | –               |
| $\overline{\text{CE}}$        | I   | 4                               | 8               | 8               | 4                     | 8               | 4             | 8               | 10              | 15              | 15              |
| GND                           |     | 5                               | 10              | 10              | 5                     | 10              | 5             | 10              | 11              | 18              | 18              |
| $\overline{\text{CEO}}^{(1)}$ | O   |                                 |                 |                 |                       |                 |               |                 | 13              |                 |                 |
| A2                            | I   | 6                               | 14              | 14              | 6                     | 14              | 6             | 14              | –               | 21              | 21              |
| READY                         | O   | –                               | –               | –               | –                     | 15              | –             | 15              | –               | 23              | 23              |
| $\overline{\text{SER\_EN}}$   | I   | 7                               | 17              | 17              | 7                     | 17              | 7             | 17              | 18              | 35              | 35              |
| V <sub>CC</sub>               |     | 8                               | 20              | 20              | 8                     | 20              | 8             | 20              | 20              | 38              | 38              |

- Notes: 1. The  $\overline{\text{CEO}}$  feature is not available on the AT17LV65 (NRND).  
2. The AT17LV65 and AT17LV128 are not recommended for new designs.

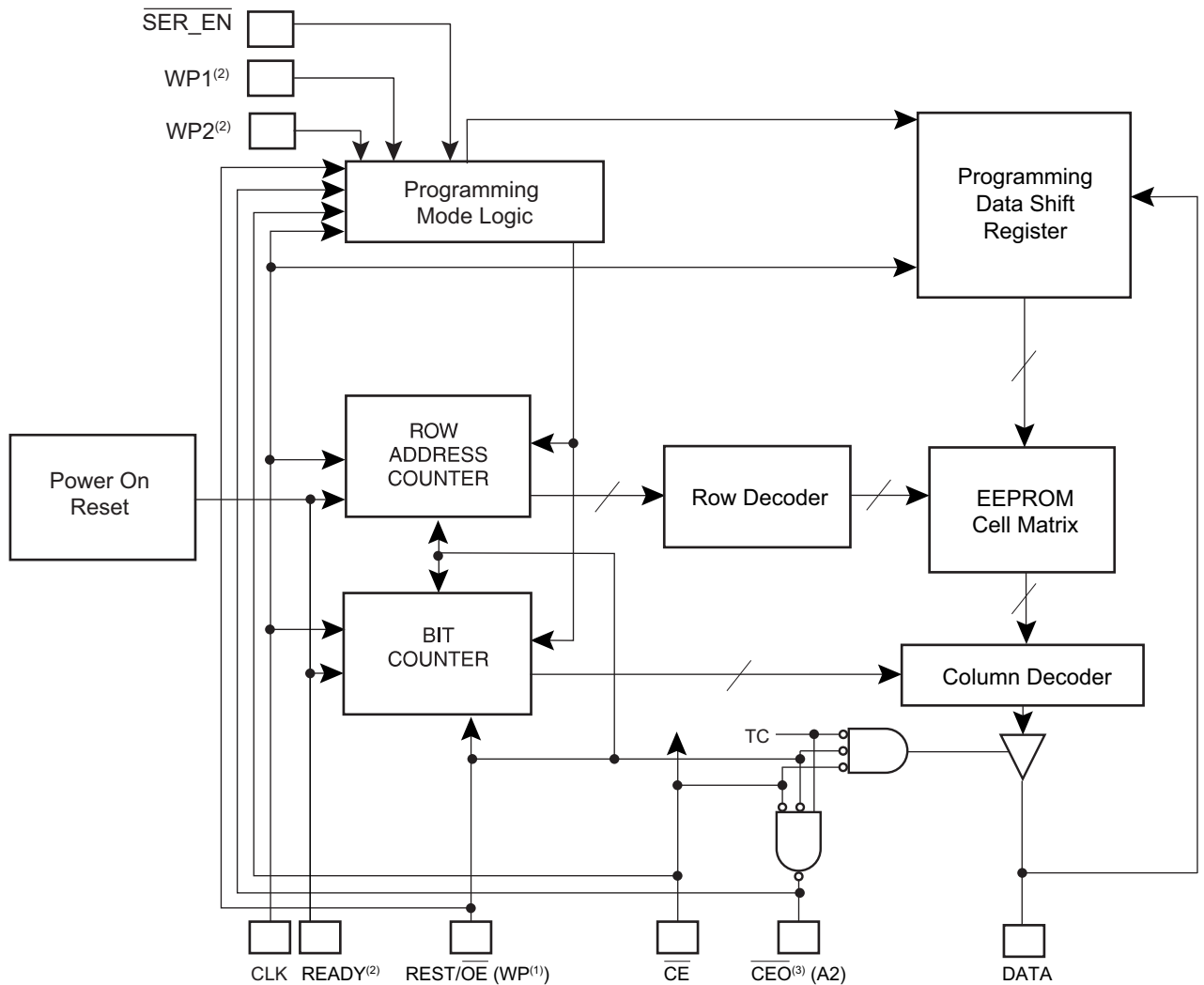
**Figure 1-1. Pinouts<sup>(1)</sup>**



- Notes:
1. Drawings are not to scale.
  2. This pin is only available on the AT17LV65 (NRND), AT17LV128 (NRND), and AT17LV256.
  3. This pin is only available on the AT17LV512/010/002.
  4. This pin is not available on the AT17LV65 (NRND).
  5. The AT17LV65 and AT17LV128 are not recommended for new designs.

## 2. Block Diagram

Figure 2-1. Block Diagram



- Notes:
1. This pin is only available on the AT17LV65 (NRND), AT17LV128 (NRND), and AT17LV256.
  2. This pin is only available on AT17LV512, AT17LV010, and AT17LV002.
  3. The CEO feature is not available on the AT17LV65 (NRND).

### 3. Device Description

The control signals for the configuration EEPROM ( $\overline{CE}$ ,  $\overline{RESET/OE}$  and CCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM  $\overline{RESET/OE}$  and  $\overline{CE}$  pins control the tri-state buffer on the DATA output pin and enable the address counter. When  $\overline{RESET/OE}$  is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The  $\overline{CE}$  pin also controls the output of the AT17LV configurator. If  $\overline{CE}$  is held High after the  $\overline{RESET/OE}$  reset pulse, the counter is disabled and the DATA output pin is tri-stated. When  $\overline{OE}$  is subsequently driven Low, the counter and the DATA output pin are enabled. When  $\overline{RESET/OE}$  is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of  $\overline{CE}$ .

When the configurator has driven out all of its data and  $\overline{CEO}$  is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe  $\overline{RESET/OE}$ .

### 4. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17LV Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Xilinx applications.

### 5. Control of Configuration

Most connections between the FPGA device and the AT17LV Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17LV configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17LV configurator.
- The  $\overline{CEO}$  output of any AT17LV configurator drives the  $\overline{CE}$  input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{SER\_EN}$  must be connected to  $V_{CC}$  (except during ISP).
- The  $\overline{READY}^{(1)}$  pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

Note: 1. This pin is not available for the AT17LV65 (NRND), AT17LV128 (NRND), and AT17LV256.

## 6. Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its  $\overline{CEO}$  output Low and disables its DATA line driver. The second configurator recognizes the Low level on its  $\overline{CE}$  input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the  $\overline{RESET/OE}$  on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the  $\overline{RESET/OE}$  input can be tied to its inactive (High) level.

The AT17LV65 (NRND) devices do not have the  $\overline{CEO}$  feature to perform cascaded configurations.

## 7. AT17LV Reset Polarity

The AT17LV configurator allows the user to program the reset polarity as either  $\overline{RESET/OE}$  or  $\overline{RESET/OE}$ . This feature is supported by industry-standard programmer algorithms.

## 8. Programming Mode

The programming mode is entered by bringing  $\overline{SER\_EN}$  Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at  $V_{CC}$  supply only. Programming super voltages are generated inside the chip.

## 9. Standby Mode

The AT17LV configurators enter a low-power standby mode whenever  $\overline{CE}$  is asserted High. In this mode, the AT17LV65 (NRND), AT17LV128 (NRND), or the AT17LV256 configurator consumes less than 50 $\mu$ A of current at 3.3V (100 $\mu$ A for the AT17LV512/010 and 200 $\mu$ A for the AT17LV002/040). The output remains in a high-impedance state regardless of the state of the  $\overline{OE}$  input.



## 10. Electrical Specifications

### 10.1 Absolute Maximum Ratings\*

|  |                               |
|--|-------------------------------|
| Operating Temperature                        | .....-40°C to +85°C           |
| Storage Temperature                          | .....-65°C to +150°C          |
| Voltage on Any Pin<br>with Respect to Ground | .....-0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage ( $V_{CC}$ )                  | ..... -0.5V to +7.0V          |
| Maximum Soldering Temp. (10s @ 1/16 in.)     | .....260°C                    |
| ESD ( $R_{ZAP} = 1.5K, C_{ZAP} = 100pF$ )    | .....2000V                    |

\*Notice: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

### 10.2 Operating Conditions

Table 10-1. Operating Conditions

| Symbol   | Description  | 3.3V |     | 5.0V |     | Units |
|----------|--|------|-----|------|-----|-------|
|          |  | Min  | Max | Min  | Max |       |
| $V_{CC}$ | Industrial<br>Supply voltage relative to GND<br>-40°C to +85°C | 3.0  | 3.6 | 4.5  | 5.5 | V     |

### 10.3 DC Characteristics

Table 10-2. DC Characteristics for  $V_{CC} = 3.3V \pm 10\%$

| Symbol    | Description  | AT17LV65/128/256 <sup>(1)</sup> |          | AT17LV512/010 |          | AT17LV002/40 |          | Units   |
|-----------|--|---------------------------------|----------|---------------|----------|--------------|----------|---------|
|           |  | Min                             | Max      | Min           | Max      | Min          | Max      |         |
| $V_{IH}$  | High-level Input Voltage                                       | 2.0                             | $V_{CC}$ | 2.0           | $V_{CC}$ | 2.0          | $V_{CC}$ | V       |
| $V_{IL}$  | Low-level Input Voltage  | 0                               | 0.8      | 0             | 0.8      | 0            | 0.8      | V       |
| $V_{OH}$  | High-level Output Voltage<br>( $I_{OH} = -2mA$ )               | 2.4                             |          | 2.4           |          | 2.4          |          | V       |
| $V_{OL}$  | Low-level Output Voltage<br>( $I_{OL} = +3mA$ )                |                                 | 0.4      |               | 0.4      |              | 0.4      | V       |
| $I_{CCA}$ | Supply Current, Active Mode                                    |                                 | 5        |               | 5        |              | 5        | mA      |
| $I_L$     | Input or Output Leakage Current<br>( $V_{IN} = V_{CC}$ or GND) | -10                             | 10       | -10           | 10       | -10          | 10       | $\mu A$ |
| $I_{CCS}$ | Supply Current, Standby Mode                                   |                                 | 100      |               | 100      |              | 150      | $\mu A$ |

Note: 1. The AT17LV65 and AT17LV128 are not recommended for new designs.

**Table 10-3. DC Characteristics for  $V_{CC} = 5.0V \pm 10\%$** 

| Symbol    | Description  | AT17LV65/128/256 <sup>(1)</sup> |          | AT17LV512/010 |          | AT17LV002/040 |          | Units   |
|-----------|--|---------------------------------|----------|---------------|----------|---------------|----------|---------|
|           |  | Min                             | Max      | Min           | Max      | Min           | Max      |         |
| $V_{IH}$  | High-level Input Voltage                                       | 2.0                             | $V_{CC}$ | 2.0           | $V_{CC}$ | 2.0           | $V_{CC}$ | V       |
| $V_{IL}$  | Low-level Input Voltage  | 0                               | 0.8      | 0             | 0.8      | 0             | 0.8      | V       |
| $V_{OH}$  | High-level Output Voltage<br>( $I_{OH} = -2mA$ )               | 3.60                            |          | 3.76          |          | 3.76          |          | V       |
| $V_{OL}$  | Low-level Output Voltage<br>( $I_{OL} = +3mA$ )                |                                 | 0.37     |               | 0.37     |               | 0.37     | V       |
| $I_{CCA}$ | Supply Current, Active Mode                                    |                                 | 10       |               | 10       |               | 10       | mA      |
| $I_L$     | Input or Output Leakage Current<br>( $V_{IN} = V_{CC}$ or GND) | -10                             | 10       | -10           | 10       | -10           | 10       | $\mu A$ |
| $I_{CCS}$ | Supply Current, Standby Mode                                   |                                 | 150      |               | 200      |               | 350      | $\mu A$ |

Note: 1. The AT17LV65 and AT17LV128 are not recommended for new designs.

## 10.4 AC Characteristics

**Table 10-4. AC Characteristics for  $V_{CC} = 3.3V \pm 10\%$** 

| Symbol          | Description  | AT17LV65/128/256 <sup>(3)</sup> |     | AT17LV512/010/002/040 |     | Units |
|-----------------|--|---------------------------------|-----|-----------------------|-----|-------|
|                 |  | Min                             | Max | Min                   | Max |       |
| $T_{OE}^{(1)}$  | OE to Data Delay   |                                 | 55  |                       | 55  | ns    |
| $T_{CE}^{(1)}$  | $\overline{CE}$ to Data Delay  |                                 | 60  |                       | 60  | ns    |
| $T_{CAC}^{(1)}$ | CLK to Data Delay  |                                 | 80  |                       | 60  | ns    |
| $T_{OH}$        | Data Hold from $\overline{CE}$ , OE, or CLK                          | 0                               |     | 0                     |     | ns    |
| $T_{DF}^{(2)}$  | $\overline{CE}$ or OE to Data Float Delay                            |                                 | 55  |                       | 50  | ns    |
| $T_{LC}$        | CLK Low Time   | 25                              |     | 25                    |     | ns    |
| $T_{HC}$        | CLK High Time  | 25                              |     | 25                    |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK<br>(to guarantee proper counting)  | 60                              |     | 35                    |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK<br>(to guarantee proper counting) | 0                               |     | 0                     |     | ns    |
| $T_{HOE}$       | OE High Time<br>(guarantees counter is reset)                        | 25                              |     | 25                    |     | ns    |
| $F_{MAX}$       | Maximum Clock Frequency  |                                 | 10  |                       | 10  | MHz   |

Notes: 1. AC test lead = 50pF.  
 2. Float delays are measured with 5pF AC loads. Transition is measured  $\pm 200mV$  from steady-state active levels.  
 3. The AT17LV65 and AT17LV128 are not recommended for new designs.

**Table 10-5. AC Characteristics when Cascading for  $V_{CC} = 3.3V \pm 10\%$** 

| Symbol          | Description                                     | AT17LV65/128/256 <sup>(3)</sup> |     | AT17LV512/010/002/040 |     | Units |
|-----------------|---|---------------------------------|-----|-----------------------|-----|-------|
|                 |   | Min                             | Max | Min                   | Max |       |
| $T_{CDF}^{(2)}$ | CLK to Data Float Delay                         |                                 | 60  |                       | 50  | ns    |
| $T_{OCK}^{(1)}$ | CLK to $\overline{CEO}$ Delay                   |                                 | 60  |                       | 55  | ns    |
| $T_{OCE}^{(1)}$ | $\overline{CE}$ to $\overline{CEO}$ Delay       |                                 | 60  |                       | 40  | ns    |
| $T_{OOE}^{(1)}$ | $\overline{RESET/OE}$ to $\overline{CEO}$ Delay |                                 | 45  |                       | 35  | ns    |
| $F_{MAX}$       | Maximum Clock Frequency                         |                                 | 8   |                       | 10  | MHz   |

- Notes: 1. AC test lead = 50pF.  
2. Float delays are measured with 5pF AC loads. Transition is measured  $\pm 200mV$  from steady-state active levels.  
3. The AT17LV65 and AT17LV128 are not recommended for new designs.

**Table 10-6. AC Characteristics for  $V_{CC} = 5V \pm 10\%$** 

| Symbol          | Description  | AT17LV65/128/256 <sup>(3)</sup> |      | AT17LV512/010/002/040 |     | Units |
|-----------------|--|---------------------------------|------|-----------------------|-----|-------|
|                 |  | Min                             | Max  | Min                   | Max |       |
| $T_{OE}^{(1)}$  | OE to Data Delay   |                                 | 35   |                       | 35  | ns    |
| $T_{CE}^{(1)}$  | $\overline{CE}$ to Data Delay  |                                 | 45   |                       | 45  | ns    |
| $T_{CAC}^{(1)}$ | CLK to Data Delay  |                                 | 55   |                       | 50  | ns    |
| $T_{OH}$        | Data Hold from $\overline{CE}$ , OE, or CLK                          | 0                               |      | 0                     |     | ns    |
| $T_{DF}^{(2)}$  | $\overline{CE}$ or OE to Data Float Delay                            |                                 | 50   |                       | 50  | ns    |
| $T_{LC}$        | CLK Low Time   | 20                              |      | 20                    |     | ns    |
| $T_{HC}$        | CLK High Time  | 20                              |      | 20                    |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK<br>(To Guarantee Proper Counting)  | 40                              |      | 25                    |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK<br>(To Guarantee Proper Counting) | 0                               |      | 0                     |     | ns    |
| $T_{HOE}$       | OE High Time<br>(Guarantees Counter is Reset)                        | 20                              |      | 20                    |     | ns    |
| $F_{MAX}$       | Maximum Clock Frequency  |                                 | 12.5 |                       | 15  | MHz   |

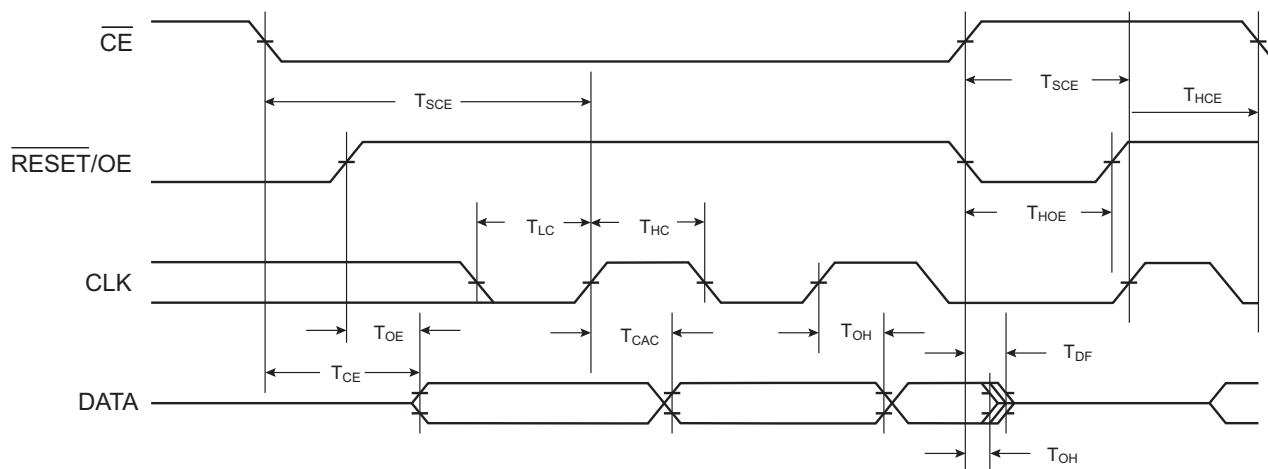
- Notes: 1. AC test lead = 50pF.  
2. Float delays are measured with 5pF AC loads. Transition is measured  $\pm 200mV$  from steady-state active levels.  
3. The AT17LV65 and AT17LV128 are not recommended for new designs.

**Table 10-7. AC Characteristics When Cascading for  $V_{CC} = 5V \pm 10\%$**

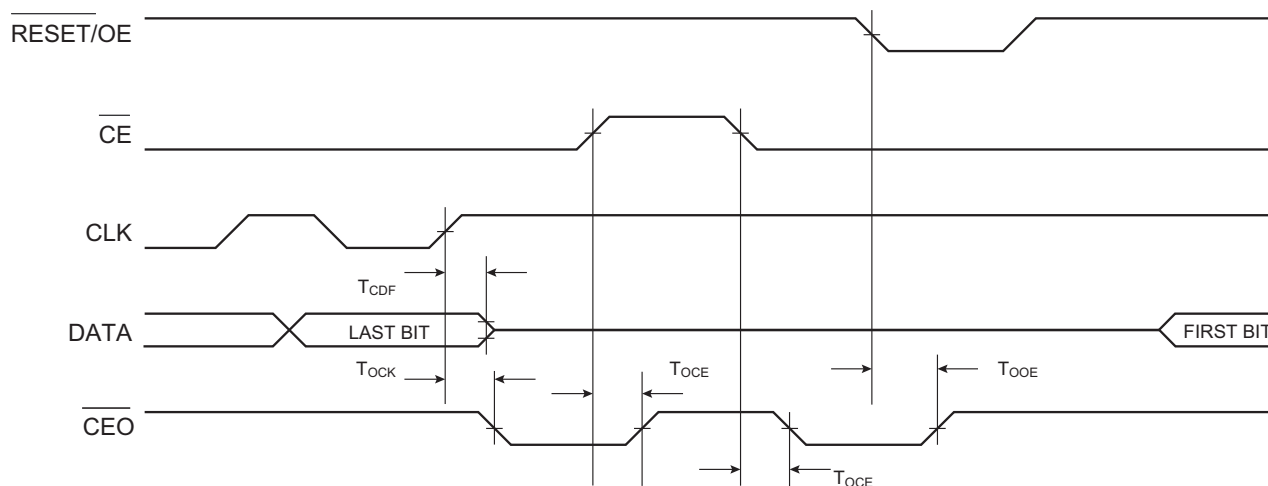
| Symbol          | Description                                     | AT17LV65/128/256 <sup>(3)</sup> |     | AT17LV512/010/002/040 |      | Units |
|-----------------|---|---------------------------------|-----|-----------------------|------|-------|
|                 |   | Min                             | Max | Min                   | Max  |       |
| $T_{CDF}^{(2)}$ | CLK to Data Float Delay                         |                                 | 50  |                       | 50   | ns    |
| $T_{OCK}^{(1)}$ | CLK to $\overline{CEO}$ Delay                   |                                 | 40  |                       | 40   | ns    |
| $T_{OCE}^{(1)}$ | $\overline{CE}$ to $\overline{CEO}$ Delay       |                                 | 35  |                       | 35   | ns    |
| $T_{OOE}^{(1)}$ | $\overline{RESET/OE}$ to $\overline{CEO}$ Delay |                                 | 35  |                       | 30   | ns    |
| $F_{MAX}$       | Maximum Clock Frequency                         |                                 | 10  |                       | 12.5 | MHz   |

- Notes: 1. AC test lead = 50pF.  
 2. Float delays are measured with 5pF AC loads. Transition is measured  $\pm 200mV$  from steady-state active levels.  
 3. The AT17LV65 and AT17LV128 are not recommended for new designs.

**Figure 10-1. AC Waveforms**



**Figure 10-2. AC Waveforms when Cascading**



## 10.5 Thermal Resistance Coefficients

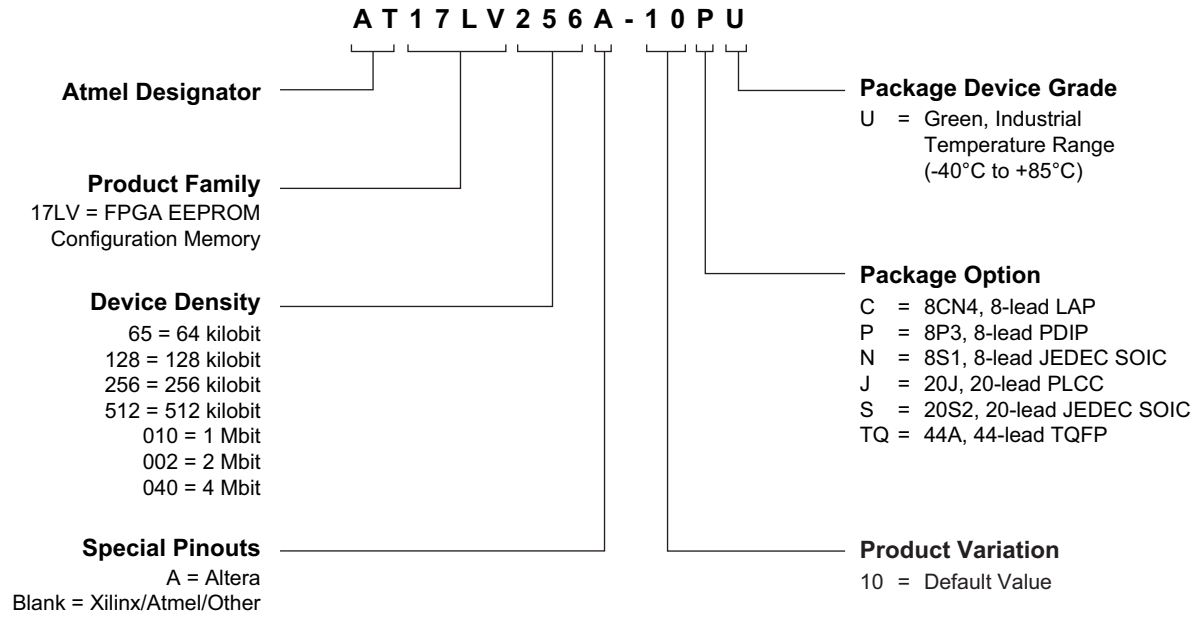
Table 10-8. Thermal Resistance Coefficients

| Package Type |  |                                     | AT17LV65/128/256 <sup>(2)</sup> | AT17LV512/010 | AT17LV002 | AT17LV040 |
|--------------|--|-------------------------------------|---------------------------------|---------------|-----------|-----------|
| 8CN4         | Leadless Array Package (LAP)           | $\theta_{JC}$ [°C/W]                | 45                              | 45            | 45        | —         |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> | 115.71                          | 135.71        | 159.60    | —         |
| 8P3          | Plastic Dual Inline Package (PDIP)     | $\theta_{JC}$ [°C/W]                | 37                              | 37            | —         | —         |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> | 107                             | 107           | —         | —         |
| 8S1          | Plastic Gull Wing Small Outline (SOIC) | $\theta_{JC}$ [°C/W]                | 45                              | —             | —         | —         |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> | 150                             | —             | —         | —         |
| 20J          | Plastic Leaded Chip Carrier (PLCC)     | $\theta_{JC}$ [°C/W]                | 35                              | 35            | 35        | —         |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> | 90                              | 90            | 90        | —         |
| 20S2         | Plastic Gull Wing Small Outline (SOIC) | $\theta_{JC}$ [°C/W]                |                                 |               |           | —         |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> |                                 |               |           | —         |
| 44A          | Thin Plastic Quad Flat Package (TQFP)  | $\theta_{JC}$ [°C/W]                | —                               | —             | 17        | 17        |
|              |  | $\theta_{JA}$ [°C/W] <sup>(1)</sup> | —                               | —             | 62        | 62        |

- Notes: 1. Airflow = 0ft/min.  
 2. The AT17LV65 and AT17LV128 are not recommended for new designs.

# 11. Ordering Information

## 11.1 Ordering Code Detail



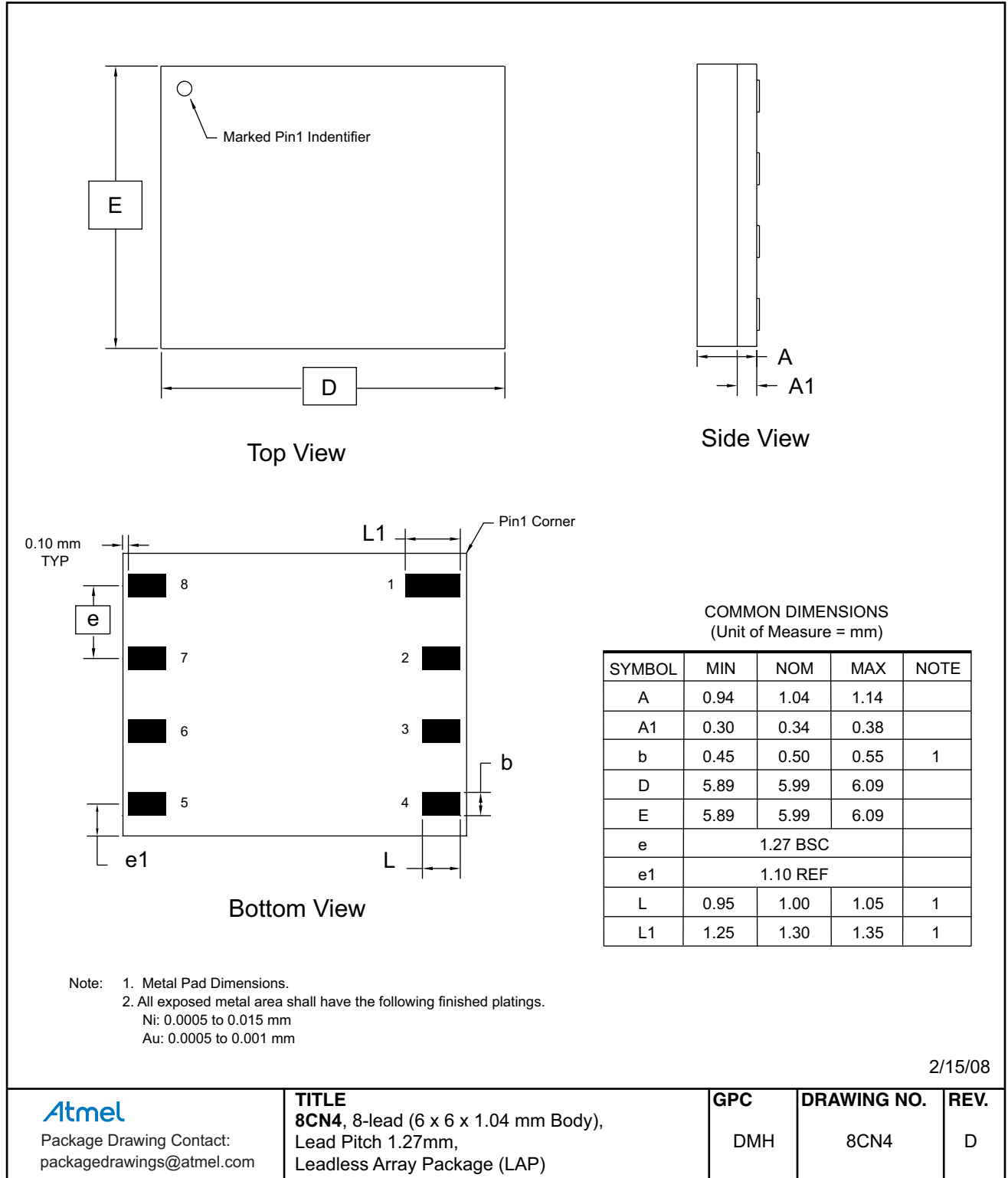
## 11.2 Ordering Information

| Memory Size | Atmel Ordering Code | Lead Finish                        | Package | Voltage      | Operation Range               |
|-------------|---------------------|------------------------------------|---------|--------------|-------------------------------|
| 256-Kbit    | AT17LV256-10CU      | CuNiAu<br>(Lead-free/Halogen-free) | 8CN4    | 3.0V to 5.5V | Industrial<br>(-40°C to 85°C) |
|             | AT17LV256-10JU      | Sn<br>(Lead-free/Halogen-free)     | 20J     |              |                               |
|             | AT17LV256-10NU      |                                    | 8S1     |              |                               |
|             | AT17LV256-10PU      |                                    | 8P3     |              |                               |
|             | AT17LV256-10SU      |                                    | 20S2    |              |                               |
| 512-Kbit    | AT17LV512-10CU      | CuNiAu<br>(Lead-free/Halogen-free) | 8CN4    | 3.0V to 5.5V | Industrial<br>(-40°C to 85°C) |
|             | AT17LV512-10JU      | Sn<br>(Lead-free/Halogen-free)     | 20J     |              |                               |
| 1-Mbit      | AT17LV010-10CU      | CuNiAu<br>(Lead-free/Halogen-free) | 8CN4    | 3.0V to 5.5V | Industrial<br>(-40°C to 85°C) |
|             | AT17LV010-10JU      | Sn<br>(Lead-free/Halogen-free)     | 20J     |              |                               |
|             | AT17LV010-10PU      |                                    | 8P3     |              |                               |
| 2-Mbit      | AT17LV002-10CU      | CuNiAu<br>(Lead-free/Halogen-free) | 8CN4    | 3.0V to 5.5V | Industrial<br>(-40°C to 85°C) |
|             | AT17LV002-10JU      | Sn<br>(Lead-free/Halogen-free)     | 20J     |              |                               |
|             | AT17LV002-10SU      |                                    | 20S2    |              |                               |
|             | AT17LV002-10TQU     |                                    | 44A     |              |                               |
| 4-Mbit      | AT17LV040-10TQU     | Sn<br>(Lead-free/Halogen-free)     | 44A     | 3.0V to 5.5V | Industrial<br>(-40°C to 85°C) |

| Package Type |  |
|--------------|--|
| <b>8CN4</b>  | 8-lead, 6mm x 6mm x 1mm, Leadless Array Package (LAP) (Pin-compatible with 8-lead SOIC Packages) |
| <b>8P3</b>   | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)  |
| <b>8S1</b>   | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)                                |
| <b>20J</b>   | 20-lead, Plastic J-leaded Chip Carrier (PLCC)  |
| <b>20S2</b>  | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)                                     |
| <b>44A</b>   | 44-lead, Thin (1.0mm) Plastic Quad Flat Package Carrier (TQFP)                                   |

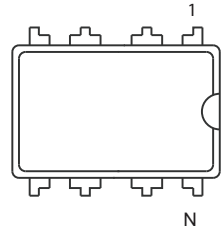
## 12. Packaging Information

### 12.1 8CN4 – LAP

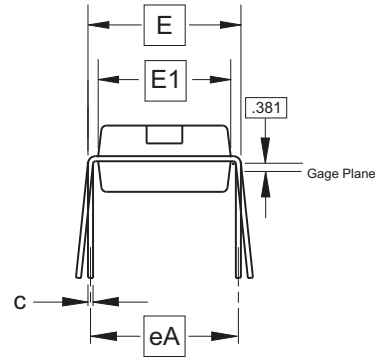




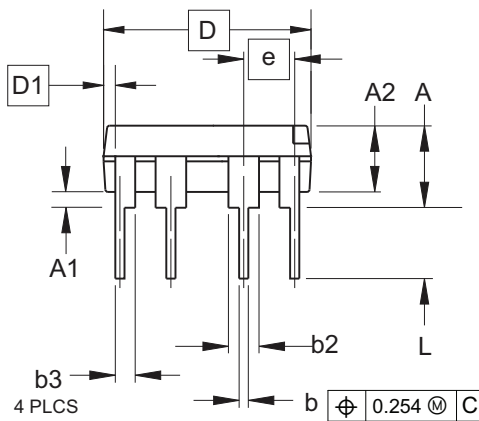
## 12.2 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM   | MAX    | NOTE |
|--------|-----------|-------|--------|------|
| A      | -         | -     | 5.334  | 2    |
| A1     | 0.381     | -     | -      |      |
| A2     | 2.921     | 3.302 | 4.953  |      |
| b      | 0.356     | 0.457 | 0.559  | 5    |
| b2     | 1.143     | 1.524 | 1.778  | 6    |
| b3     | 0.762     | 0.991 | 1.143  | 6    |
| c      | 0.203     | 0.254 | 0.356  |      |
| D      | 9.017     | 9.271 | 10.160 | 3    |
| D1     | 0.127     | 0.000 | 0.000  | 3    |
| E      | 7.620     | 7.874 | 8.255  | 4    |
| E1     | 6.096     | 6.350 | 7.112  | 3    |
| e      | 2.540 BSC |       |        |      |
| eA     | 7.620 BSC |       |        | 4    |
| L      | 2.921     | 3.302 | 3.810  | 2    |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
  2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
  3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
  4. E and eA measured with the leads constrained to be perpendicular to datum.
  5. Pointed or rounded lead tips are preferred to ease insertion.
  6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

07/31/14

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

TITLE  
8P3, 8-lead, 0.300" Wide Body, Plastic Dual  
In-line Package (PDIP)

GPC

DRAWING NO.

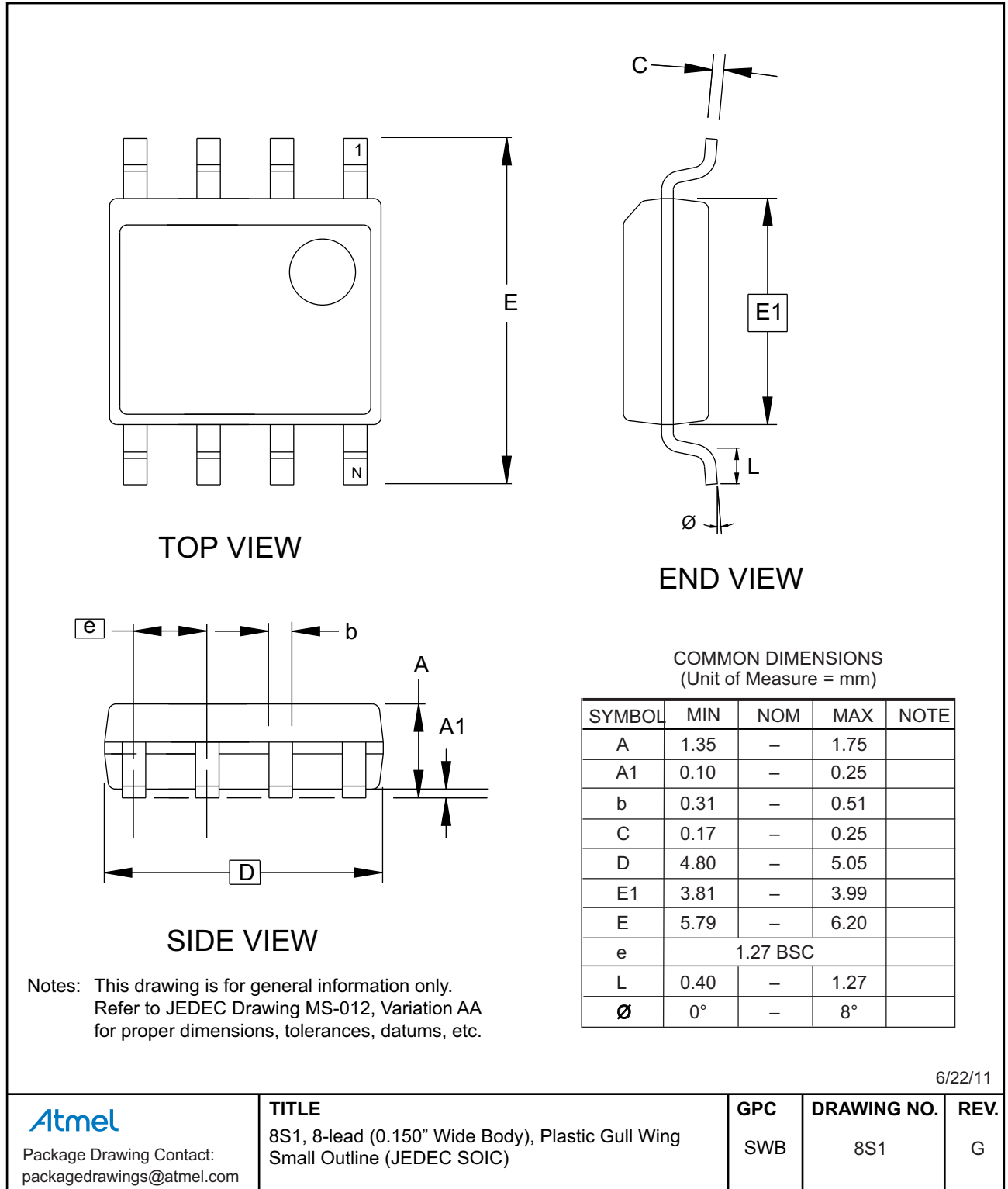
REV.

PTC

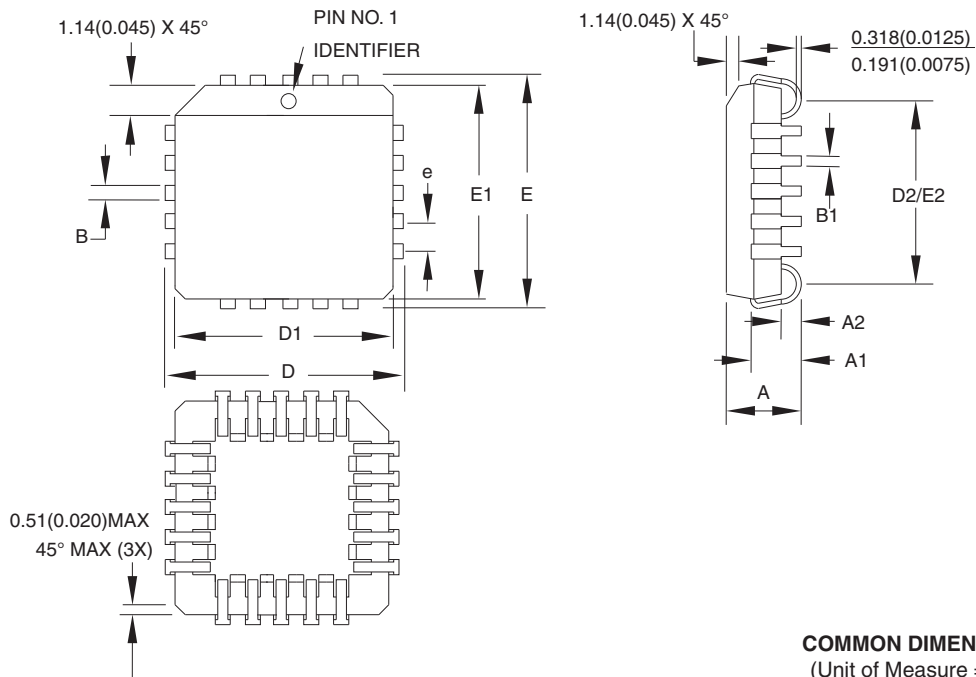
8P3

E

## 12.3 8S1 – SOIC



## 12.4 20J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | –   | 4.572  |        |
| A1     | 2.286     | –   | 3.048  |        |
| A2     | 0.508     | –   | –      |        |
| D      | 9.779     | –   | 10.033 |        |
| D1     | 8.890     | –   | 9.042  | Note 2 |
| E      | 9.779     | –   | 10.033 |        |
| E1     | 8.890     | –   | 9.042  | Note 2 |
| D2/E2  | 7.366     | –   | 8.382  |        |
| B      | 0.660     | –   | 0.813  |        |
| B1     | 0.330     | –   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102mm) maximum

10/04/01



Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**

**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)

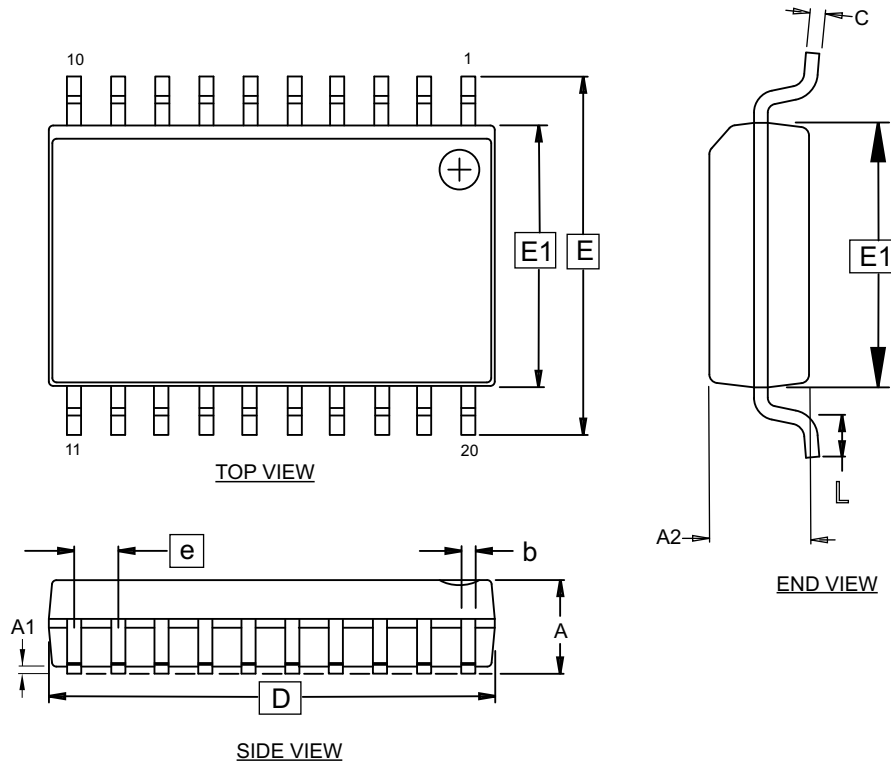
**DRAWING NO.**

20J

**REV.**

B

## 12.5 20S2 – SOIC



**Notes:**

1. This drawing is for general information only. Refer to JEDEC Drawing MS-013, Variation AC, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
3. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, the burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
4. The dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.
5. Dimension 'b' does not include the dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of the 'b' dimension at maximum material condition. The dambar may not be located on the lower radius of the foot.
6. 'A1' is defined as the vertical distance from the seating plane to the lowest point on the package body excluding the lid or thermal enhancement on the cavity down package configuration.

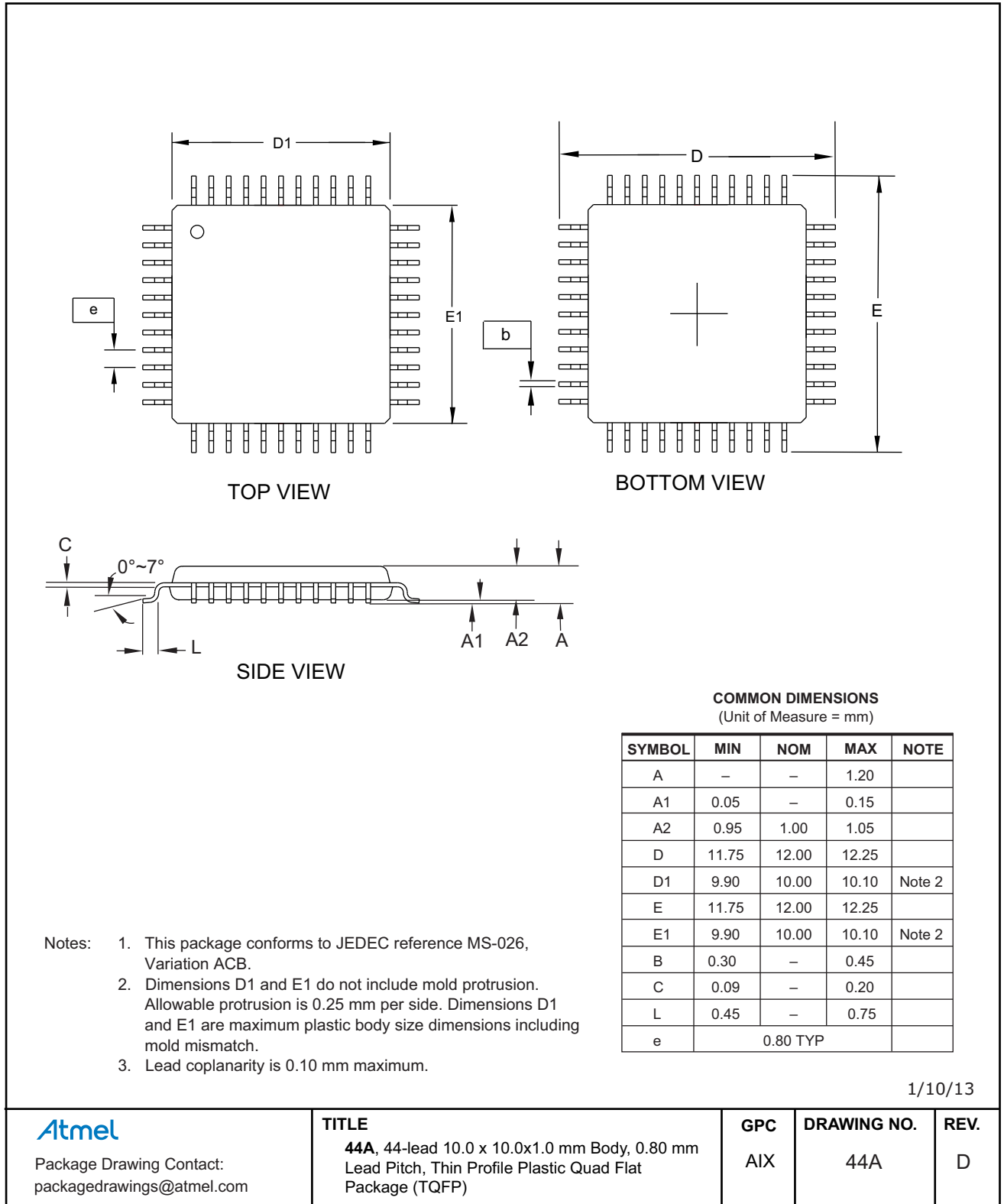
**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN  | NOM       | MAX  | NOTE |
|--------|------|-----------|------|------|
| D      |      | 12.80 BSC |      | 2,3  |
| E1     |      | 7.50 BSC  |      | 2,3  |
| E      |      | 10.30 BSC |      |      |
| A      | -    | -         | 2.65 |      |
| A1     | 0.10 | -         | 0.30 | 6    |
| A2     | 2.05 | -         | -    |      |
| e      |      | 1.27 BSC  |      |      |
| b      | 0.31 | -         | 0.51 | 4,5  |
| L      | 0.40 | -         | 1.27 |      |
| C      | 0.20 | -         | 0.33 | 4    |

7/1/14

|   |  |            |                    |             |
|---|--|------------|--------------------|-------------|
| <p>Package Drawing Contact:<br/>packagedrawings@atmel.com</p> | <b>TITLE</b>   | <b>GPC</b> | <b>DRAWING NO.</b> | <b>REV.</b> |
|   | <b>20S2, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)</b> | SRJ        | 20S2               | E           |

## 12.6 44A – TQFP



## 13. Revision History

| Rev. No. | Date    | History  |
|----------|---------|--|
| 2321J    | 10/2014 | The AT17LV65 and AT17LV128 are not recommended for new designs.<br>Removed the commercial options.<br>Updated the 8P3, 8S1, 20S2, and 44A package outline drawings, ordering code details, ordering code table, document's template, Atmel logos, disclaimer page. |
| 2321I    | 02/2008 | Removed -10SC, 10SI, -10TQC, -10TQI, -10BJC and -10BJI devices from ordering information.  |
| 2321H    | 03/2006 | Added last-time buy for AT17LVXXX-10CC and AT17LVXXX-10CI.   |



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