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TLC320AD77C

24-Bit 96 kHz Stereo Audio Codec

Data Manual

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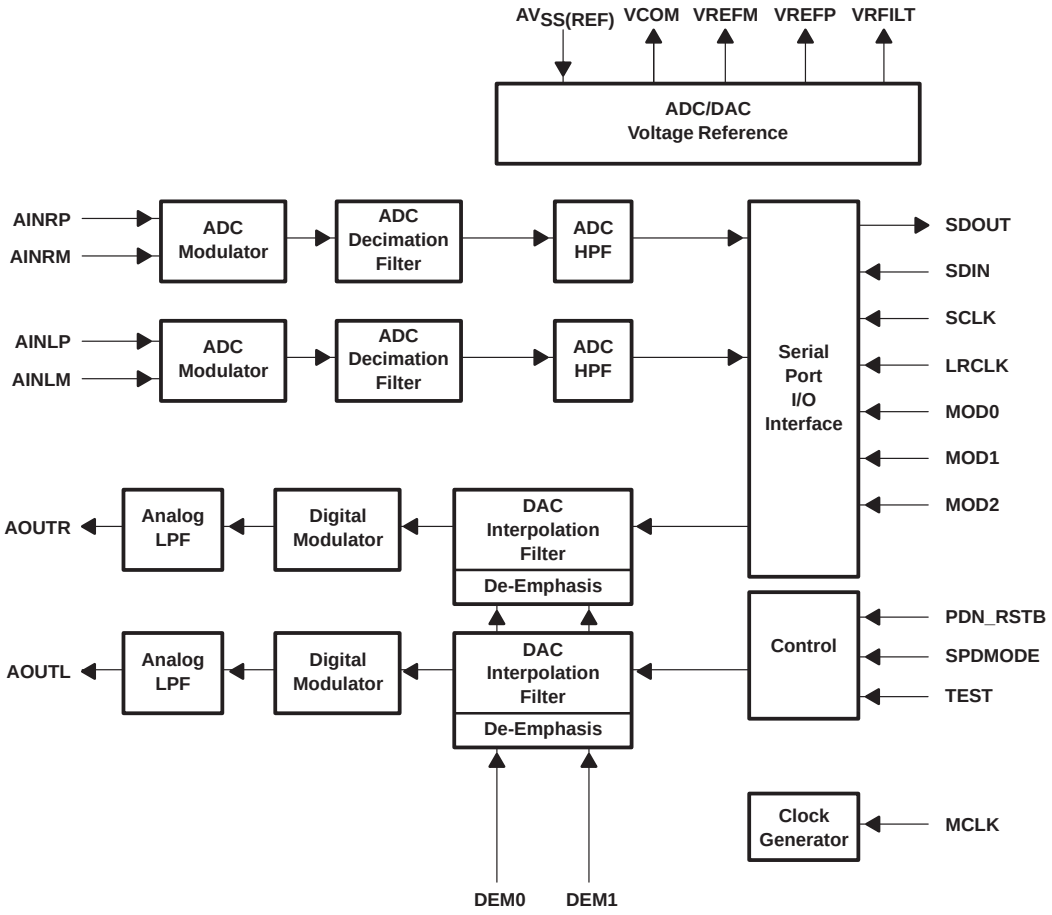
1 Introduction

The TLC320AD77C is a cost competitive stereo analog-to-digital (A/D) and digital-to-analog (D/A) 24-bit delta-sigma converter for consumer applications which demand excellent audio performance. It has a wide variety of serial input options including left justified, right justified, IIS, or DSP data formats for 16-, 20-, or 24-bit input/output data. It has an extremely wide range of sampling rates starting at 16 kHz and increasing upwards to 96 kHz. Its internal bandgap design provides a very clean voltage reference. The TLC320AD77C is primarily designed for mini-disks, audio/video receivers, musical instruments, and other end-equipments requiring high-performance digital audio conversion.

1.1 Features

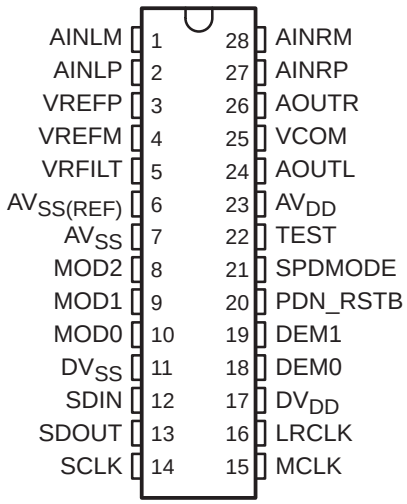
- 24-Bit Delta Sigma Stereo ADC and DAC:
  - 16-, 20-, or 24-Bit Input/Output Data
  - Wide Range of Sampling Rates: 16 kHz to 96 kHz
  - Master Clock: 256 f_S or 384 f_S
  - 3.3-V Power Supply Operation
  - Internal Bandgap Voltage Reference
  - Economical 28-Pin DB (SSOP) Package
- Stereo ADC:
  - Differential Input
  - 128× Oversampling (in normal speed mode)
  - High Performance: 100-dB Signal-to-Noise Ratio (SNR) (EIAJ), 100-dB Dynamic Range
  - Digital High-Pass Filter
- Stereo DAC:
  - Single-Ended Output
  - 128× Oversampling (in normal speed mode)
  - High Performance: 100-dB Signal-to-Noise Ratio (SNR) (EIAJ), 100-dB Dynamic Range
- Digital De-Emphasis:
  - 32-kHz, 44.1-kHz, and 48-kHz Selection
- Special Features:
  - High Jitter Tolerance
  - Good Phase Characteristics
  - Excellent Power Supply Rejection Ratio

1.2 Functional Block Diagram



1.3 Terminal Assignments

DB PACKAGE
(TOP VIEW)



1.4 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (DB)
0°C to 70°C	TLC320AD77C

1.5 Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AINLM	1	I	ADC analog differential negative input, left channel
AINLP	2	I	ADC analog differential positive input, left channel
AINRM	28	I	ADC analog differential negative input, right channel
AINRP	27	I	ADC analog differential positive input, right channel
AOUTL	24	O	DAC analog output, left channel
AOUTR	26	O	DAC analog output, right channel
AV_{DD}	23		Analog voltage supply
AV_{SS}	7		Analog voltage ground
$AV_{SS(REF)}$	6	I	Analog ground voltage reference
DEM0	18	I	De-emphasis selection
DEM1	19	I	De-emphasis selection
DV_{DD}	17		Digital voltage supply
DV_{SS}	11		Digital ground
LRCLK	16	I	Left/right clock
MCLK	15	I	Master clock
MOD0	10	I	Serial interface selection
MOD1	9	I	Serial interface selection
MOD2	8	I	Serial interface selection
PDN_RSTB	20	I	Power down/reset
SCLK	14	I	Shift or bit clock
SDIN	12	I	Serial data DAC input
SDOUT	13	O	Serial data ADC output
SPDMODE	21	I	Sampling frequency selection
TEST	22		Reserved, manufacturing test pin. Test should be connected to DV_{SS}.
VCOM	25	O	Common mode reference, provides a 1.5-V reference voltage (DAC only)
VREFM	4	O	ADC/DAC negative reference voltage
VREFP	3	O	ADC/DAC positive reference voltage
VRFILT	5	O	Voltage reference low pass noise filter

2 Functional Description

2.1 ADC Channel

To produce excellent common-mode rejection of unwanted signals, the analog signal is processed differentially until it is converted to digital data. A single-ended input signal must be converted into a differential input and filtered with a single-pole antialiasing filter before entering the ADC input. (See Section 2.7, *ADC Analog Input*). The ADC converts the signal into discrete output digital words in 2s-complement format, corresponding to the analog signal input. There is a high-pass filter to get rid of any offset that the ADC modulator may have caused. These digital words, representing sampled values of the analog input signal, are then clocked out the serial port, SDOUT, according to one of the eight allowable serial port protocols.

2.2 DAC Channel

SDIN receives a serial data word whose length is specified by one of the eight allowable serial port protocols, selected by the serial mode pins. The serial port latches the data on an edge of SCLK. The data goes through the sigma-delta DAC comprised of digital interpolation filters and a seventh order, 1-bit digital modulator. This oversampled signal is then passed through a switched capacitor FIR filter and RC low-pass filter which smoothes the output waveform, and performs the differential to single-ended conversion. The DAC outputs a stereo single-ended, inverted signal. This signal should be passed through an inverting, pseudo-differential, external low-pass filter, where the VCOM reference is subtracted out. (See Section 2.8, *DAC Analog Output*).

2.3 Serial Interface

The digital serial interface consists of a serial port, shift clock (SCLK), left/right frame synchronization clock (LRCLK), ADC-channel data output (SDOUT), and DAC-channel data input (SDIN). One of 8 different serial port modes may be selected including IIS, right/left justified, left/left justified, and a DSP mode for word lengths ranging from 16 to 24 bits. See Section 2.14, *Serial Interface Formats* for a description of serial interface formats.

2.4 Sampling Frequency

The sampling or conversion frequency is designated by the MCLK rate by the following equation.

f_S = MCLK frequency/ (256 or 384).

See Section 2.14, *Serial Interface Formats* for more information on the option of selecting an MCLK rate of 256 f_S or 384 f_S.

2.5 Speed Mode Options

In normal-speed mode (SPDMOD = 0), sampling frequencies ranging from 16 kHz up to 48 kHz should be used to achieve optimum performance.

In high-speed mode (SPDMOD = 1) the sampling frequencies are greater than 48 kHz and up to 96 kHz.

2.6 Voltage Reference

In order to achieve excellent noise rejection, a pseudo-differential reference is used with external capacitors connected to a differential low-pass filter. The application schematic shows the necessary capacitors needed to complete the filters found on the device. See Section 5, *Application Information* for the application schematic for the voltage reference.

2.7 ADC Analog Input

The ADC accepts a differential input with a maximum value that does not exceed approximately 4 V_{pp}. See Section 5.1, *Single-Ended to Differential External Analog Front-End Circuit* for a description of the recommended external analog front end.

2.8 DAC Analog Output

The DAC outputs a single-ended signal with a max value of 0.7 Vrms. See Section 5.2, *External Analog Back-End Circuit* for a description of the recommended back-end circuit.

2.9 Sigma-Delta ADC

The sigma-delta ADC is a third order modulator with 128 times oversampling in normal speed operation. The ADC provides high resolution and low noise performance using over-sampling techniques.

2.10 Decimation Filter

The decimation filter reduces the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:128. The output of this filter is a 2s complement 16-, 20-, 24-bit word clocking at the sample rate selected.

2.11 Sigma-Delta DAC

The sigma-delta DAC is a seventh order modulator with 128 times oversampling. The DAC provides high-resolution, low noise, from a 1-bit converter using over-sampling techniques.

2.12 Interpolation Filter

The interpolation filter resamples the digital data at a rate 128 times the incoming sample rate. The high-speed data output is then used in the sigma-delta DAC.

2.13 De-emphasis

De-emphasis is supported for three sampling rates: 32 kHz, 44.1 kHz, and 48 kHz and selected with the DEM0 and DEM1 pins.

2.14 Serial Interface Formats

The TLC320AD77C operates only in slave mode. It requires externally supplied MCLK (master clock), and LRCLK (left/right clock), and SCLK (shift clock) inputs. There are two options for selecting the clock rates. If a 384 f_S MCLK rate is selected, then a LRCLK frame of 48 SCLKs must be supplied. If a 256 f_S MCLK is selected, then a LRCLK of 64 SCLKs must be supplied.

- A detection circuit automatically senses at which rate the MCLK is operating.
- The MCLK and SCLK must be synchronous and their edges must be at least 3 ns apart.
- If the LRCLK phase changes more than 10 MCLKs then the device automatically resets.

The TLC320AD77C is compatible with eight different serial interfaces. Available interface options are IIS, right justified, left justified, and DSP frame. The following table indicates how the eight options are selected using the MOD0, MOD1, and MOD2 pins. All serial interface options at either 16-, 20-, or 24-bits can operate with SCLK at 48*f_S or 64*f_S except for the 16-bit DSP mode which should use SCLK = 64 f_S.

MODE	MOD2 PIN	MOD1 PIN	MOD0 PIN	SERIAL INTERFACE SDIN (DAC)/SDOUT (ADC)
0	0	0	0	16-bit, MSB first, right justified/left justified
1	0	0	1	20-bit, MSB first, right justified/left justified
2	0	1	0	24-bit, MSB first, right justified/left justified
3	0	1	1	16-bit IIS
4	1	0	0	20-bit IIS
5	1	0	1	24-bit IIS
6	1	1	0	16-bit MSB first, left justified/left justified
7	1	1	1	16-bit DSP frame (see Note 1)

NOTE 1: For the 16-bit DSP frame use SCLK = 64 f_S.

2.14.1 MSB First Right/Left Justified Format

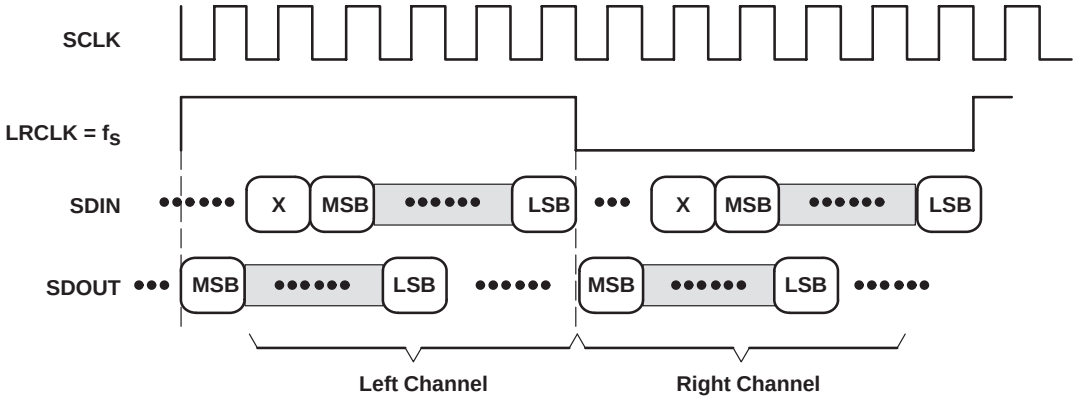


Figure 2–1. MSB First Right/Left Justified (for 16-, 20-, and 24-bits)

Note the following characteristics of this protocol.

- Left channel data is valid when LRCLK is high.
- The SDIN (recorded data) data is justified to the trailing edge of LRCLK
- The SDOUT MSB (playback data) is transmitted at the same time as the LRCLK edge, and captured at the very next rising edge of SCLK.
- If LRCLK phase changes by more than 10 MCLKs, then the device is automatically reset.

2.14.2 IIS-Compatible Serial Format

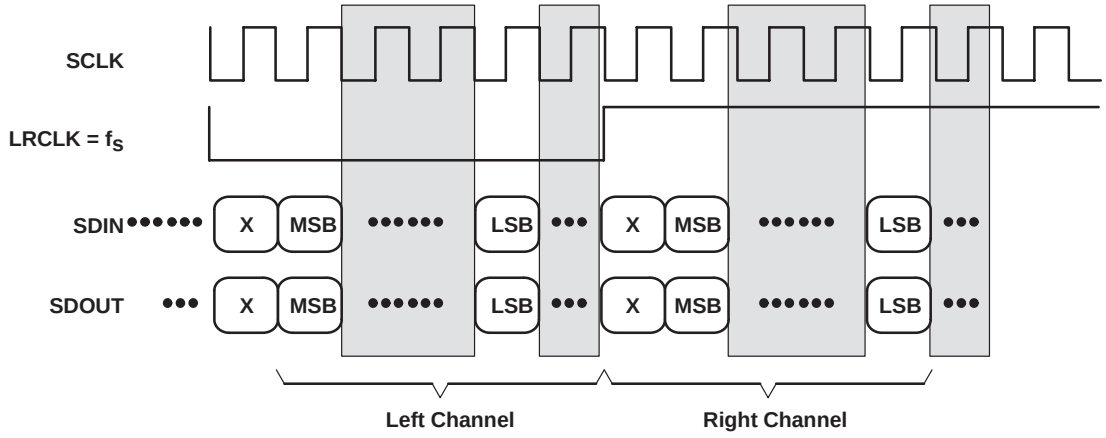


Figure 2–2. IIS-Compatible Serial Format (for 16-, 20-, and 24-bits)

Note the following characteristics of this protocol.

- Left channel data is valid when LRCLK is low.
- SDIN is sampled with the rising edge of SCLK.
- SDOUT is transmitted on the falling edge of SCLK.
- If LRCLK phase changes by more than 10 MCLKs, then the device is automatically reset.

2.14.3 MSB Left Justified Serial Interface Format

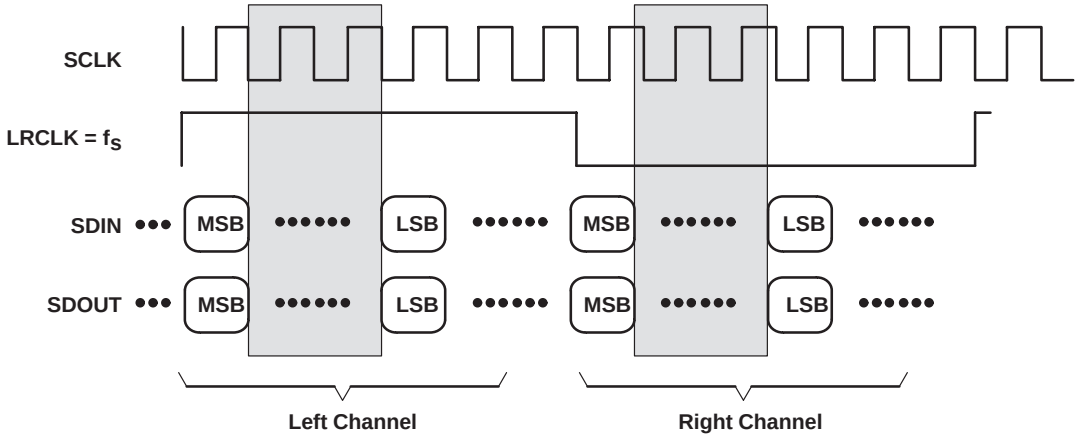


Figure 2–3. MSB Left Justified Serial Interface Format (for 16-bits)

Note the following characteristics of this protocol.

- Left channel data is valid when LRCLK is high.
- The SDIN data is justified to the leading edge of LRCLK.
- The MSBs are valid at the same time as the LRCLK edge for SDOUT, and captured at the very next rising edge of SCLK for SDIN.

2.14.4 DSP Compatible Serial Interface Format

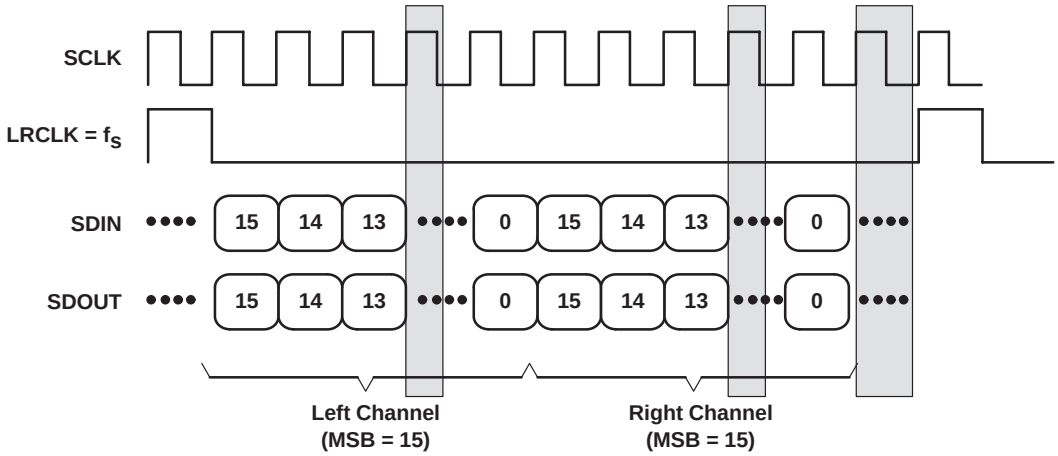


Figure 2–4. DSP Compatible Serial Interface Format (for 16-bits)

Note the following characteristics of this protocol.

- MCLK = 256 F_S only
- SCLK = 64 times the sampling frequency.
- Serial data is sampled with the falling edge of SCLK.
- Serial data is transmitted on the rising edge of SCLK.

2.15 Sampling Frequency Ranges

The TLC320AD77C supports two sampling frequency ranges.

- When in the normal option ranging from 16 kHz up to 48 kHz, SPDMOD = low is used.
- When in the fast option ranging from greater than 48 kHz up to 96 kHz, SPDMOD = high is used.

NOTE:
The high speed clocks should never be applied while SPDMOD is low in order to avoid glitches in the DAC and ADC outputs.

Table 2–1. Example Master Clock Frequency Rates

SAMPLING RATE FREQUENCY (kHz)	MCLK FREQUENCY		SPDMODE
	256 f_S	384 f_S	
32	8.192 MHz	12.2880 MHz	0
44.1	11.2896 MHz	16.9340 MHz	0
48	12.2880 MHz	18.432 MHz	0
64	16.384 MHz	24.576 MHz	1
88.2	22.579 MHz	33.868 MHz	1
96	24.576 MHz	36.864 MHz	1

2.16 Power Sequences

2.16.1 Initial Power Up

For initial power up, the ADC and DAC outputs are valid after the 150 ms settling time required for the analog stages. Holding the power down pin low while ramping up the power supplies is recommended to avoid glitches in the DAC output.

2.16.2 Power Down/Reset

The TLC320AD77C is capable of entering a stand-by mode at reduced power when no activity is required. To initiate the reset sequence, PDN_RSTB is held low for a minimum of 10 ns. As long as the pin is held low, the device is in the power-down state.

In order for the dynamic logic to be properly powered down, the clocks should not be stopped before the PDN_RSTB pin goes low. Otherwise, the device may drain additional supply current.

2.16.3 Reinitialization Sequence

When PDN_RSTB is returned to high, the device begins a reinitialization sequence after all clocks are active. The output data becomes valid after a minimum of 128 LRCLK cycles after the pin is pulled high. During the initialization sequence the outputs of the DAC and ADC are invalid.

Any change in the control lines (MOD0, MOD1, MOD2, DEM0, DEM1, SPDMOD, PDN_RST) or phase shift in LRCLK triggers the reinitialization sequence.

In order for the dynamic logic to be properly powered down, the clocks should not be stopped before the PDN_RSTB pin goes low. Otherwise, the device may drain additional supply current.

2.17 DAC De-Emphasis Filter

De-emphasis is only supported for three sampling rates (f_S): 32 kHz, 44.1 kHz, and 48 kHz in normal speed operation. The DEM0 and DEM1 pins select the filter coefficients and enable or disable the filter. Figure 2–5 illustrates the de-emphasis filtering characteristics.

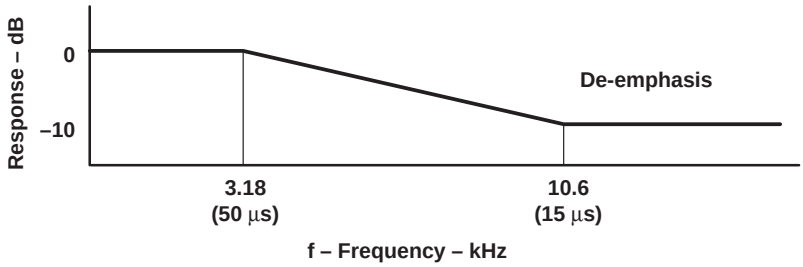


Figure 2–5. De-Emphasis Characteristics

2.17.1 De-Emphasis Selection

De-emphasis control is achieved using the DEM1 and DEM0 pins. The pin control is defined in the following table.

DEM 1	DEM 0	DE-EMPHASIS
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	Off

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Analog supply voltage range, AV_{DD} . . . . . –0.3 V to 4.2 V
Digital supply voltage range, DV_{DD} . . . . . –0.3 V to 4.2 V
Analog input voltage range . . . . . –0.3 V to AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%, f_S = 44.1 kHz

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD} (see Note 1)	3	3.3	3.6	V
Digital supply voltage, DV_{DD} (see Note 1)	3	3.3	3.6	V
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Voltages at analog inputs and outputs and AV_{DD} are with respect to ground.

3.3 Electrical Characteristics, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%, f_S = 44.1 kHz

PARAMETER		MIN	TYP	MAX	UNIT
Analog supply current	Operating		30		mA
	Power down (see Note 2)			150	µA
Digital supply current	Operating		20		mA
	Power down (see Note 2)			1	µA
Power dissipation	Operating		160		mW
	Power down			360	µW

NOTE 2: If clocks are turned off.

3.3.1 Static Digital Specifications, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%

PARAMETER		MIN	MAX	UNIT
V_{IH}	High-level input voltage	2	3.6	V
V_{IL}	Low-level input voltage	–0.3	0.8	V
V_{OH}	High-level output voltage (I_O = –1 mA)	2.4		V
V_{OL}	Low-level output voltage (I_O = 4 mA)		0.4	V
I_{lkg}	Input leakage current	–10	10	µA
C_L	Load capacitance, SDOUT		50	pF

3.3.2 ADC Digital Filter, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%, f_S = 44.1 kHz (see Notes 3 and 4)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filter (LPF)					
Pass band			20		kHz
Pass band ripple			±0.01		dB
Stop band			24.1		kHz
Stop band attenuation		80			dB
Group delay			720		µs
ADC High-Pass Filter (HPF)					
Pass band (–3 dB)			0.87		Hz
Deviation from linear phase	20 Hz to 20 kHz		1.23		degree

NOTES: 3. All the terms characterized by frequency, scale with the chosen sampling frequency, f_S.
4. See Figure 4–6 through Figure 4–9 for performance curves on the ADC digital filter.

3.3.3 Analog-to-Digital Converter, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V, f_S = 44.1 kHz (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (EIAJ)	A-weighted		100		dB
	Dynamic range	A-weighted, –60 dB, 1 kHz		100		dB
	Signal-to-noise + distortion ratio	20 Hz to 20 kHz		86		dB
	Power supply rejection ratio	1 kHz, See Note 5		50		dB
	Idle channel tone rejection			120		dB
	Intermodulation distortion			–80		dB
	ADC crosstalk			100		dB
	Overall ADC frequency response	20 Hz to 20 kHz	–0.1		0.1	dB
	Gain error				5%	
	Gain matching			±0.02		dB
	Full-scale differential input voltage			3.6		V_{pp}
CMRR	Common mode rejection ratio			100		dB

NOTES: 3. All the terms characterized by frequency, scale with the chosen sampling frequency, f_S.
5. Measured with a 50 mV peak sine wave.

3.3.4 DAC Interpolation Filter, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V + 10%, f_S = 44.1 kHz (see Notes 3 and 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass band		0		20	kHz
Pass band ripple			±0.005		dB
Stop band			24.1		kHz
Stop band attenuation	28.8 kHz to 3 MHz	75			dB
Group delay			700		µs

NOTES: 3. All the terms characterized by frequency, scale with the chosen sampling frequency, f_S.
6. See Figure 4–4 and Figure 4–5 for performance curves of the DAC digital filter.

3.3.5 Digital-to-Analog Converter, T_A = 25°C, AV_{DD} = 3.3 V, f_S = 44.1 kHz, Input = 1 V_{rms} Sine Wave at 1 kHz (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio (EIAJ)	A-weighted		100		dB
	Dynamic range	A-weighted, –60 dB, f = 1 kHz		100		dB
	Signal-to-noise + distortion ratio	0 dB, 1 kHz		80		dB
	Power supply rejection ratio	1 kHz		50		dB
	Idle tone rejection			120		dB
	Intermodulation distortion			–75		dB
	Frequency response		–0.5		0.5	dB
	Deviation from linear phase			±1.4		degree
	DAC crosstalk			100		dB
	Full-scale single-ended output voltage	AV_{DD} = 3.3 V		1.75		V_{PP}

NOTE 3: All the terms characterized by frequency, scale with the chosen sampling frequency, f_S.

3.3.6 Output Performance Data, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Driver Loading						
R_L	Output load resistance, (see Note 7)		10			kΩ
C_L	Output load capacitance				25	pF
$R_{L(COM)}$	Output load resistance, COM (see Note 8)			1		kΩ
$C_{L(COM)}$	Output load capacitance, COM (see Note 8)			50		pF
	RFILT internal resistance, RFILT (see Note 9)			1		kΩ

NOTES: 7. The output load resistance is coupled through an ac coupled capacitor.
8. COM may vary during power down.
9. RFILT should never be used as a voltage reference.

3.4 Serial Interface Switching Characteristics, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10%

PARAMETER		MIN	TYP	MAX	UNIT
$f_{(SCLK)}$	SCLK frequency			6.144	MHz
$t_{d(LRCLK)}$	Delay time, LRCLK edge to SCLK rising	20		$1/(128\times f_S)$	ns
$t_{d(SDOUT)}$	Delay time, SDOUT valid from SCLK falling (see Note 10)			$(1/(256\times f_S))+10$	ns
$t_{su(SDIN)}$	SDIN setup time before SCLK rising edge	20			ns
$t_{h(SDIN)}$	SDIN hold time from SCLK rising edge	10			ns
$f_{(LRCLK)}$	LRCLK frequency	16	44.1	96	kHz
	MCLK duty cycle		50%		
	SCLK duty cycle		50%		
	LRCLK duty cycle		50%		

NOTE 10: Maximum of 50-pF external load on SDOUT

3.5 DSP Serial Interface Switching Characteristics, T_A = 25°C, AV_{DD} = DV_{DD} = 3.3 V ± 10% (see Note 11)

PARAMETER		MIN	TYP	MAX	UNIT
$f_{(SCLK)}$	SCLK frequency			6.144	MHz
$t_{d(FS)}$	Delay time, SCLK rising to Fs			25	ns
$t_{w(FSHIGH)}$	Pulse duration, sync		$1/(64\times f_S)$		ns
$t_{d(SDOUT)}$	Delay time, SDOUT valid from SCLK rising (see Note 12)			$(1/(256\times f_S))+10$	ns
$t_{su(SDIN)}$	SDIN and LRCLK setup time before SCLK falling edge	20			ns
$t_{h(SDIN)}$	SDIN and LRCLK hold time from SCLK falling edge	10			ns
	SCLK duty cycle		50%		

NOTES: 11. Burst mode is not supported.
12. Timing parameters for DSP format which samples on the falling edge

4 Parameter Measurement Information

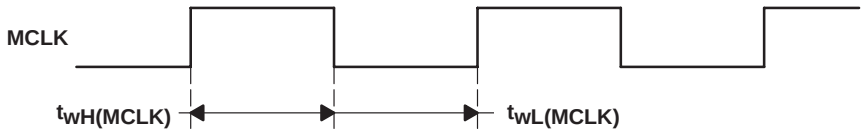


Figure 4–1. Master Clock Timing

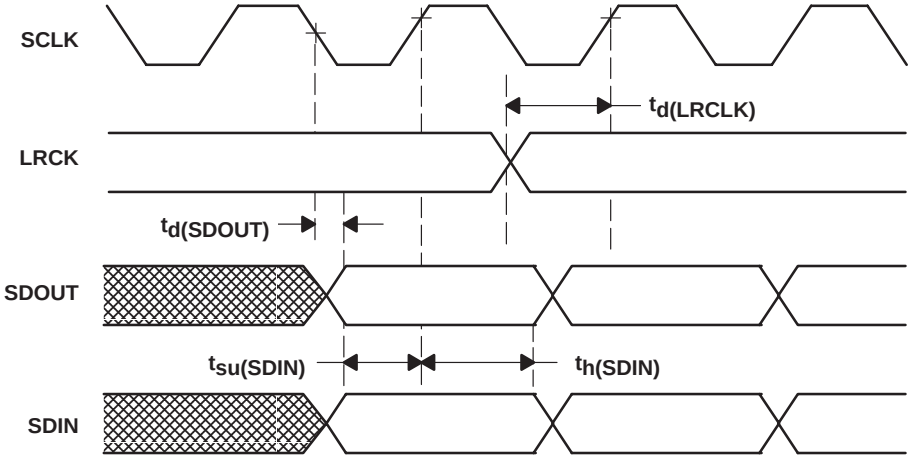


Figure 4–2. Right/Left Justified, IIS, Left/Left Justified Serial Protocol Timing

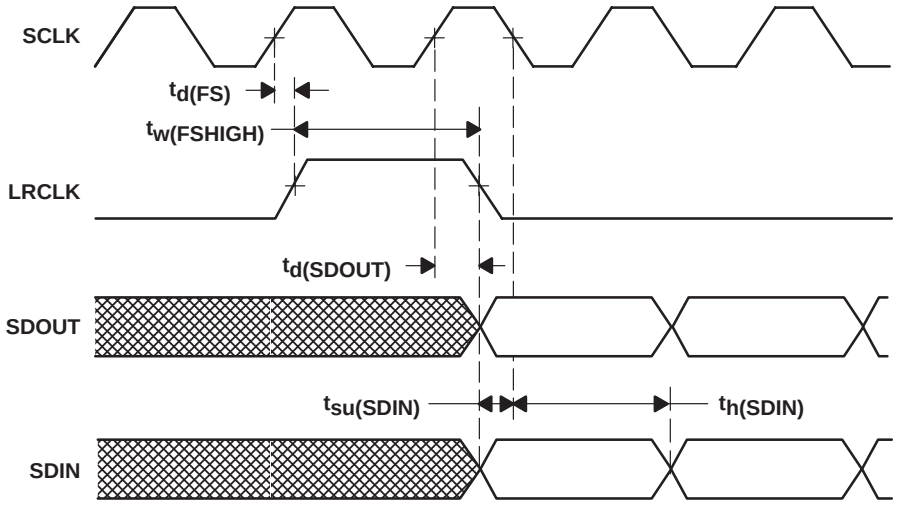


Figure 4–3. DSP Serial Port Timing

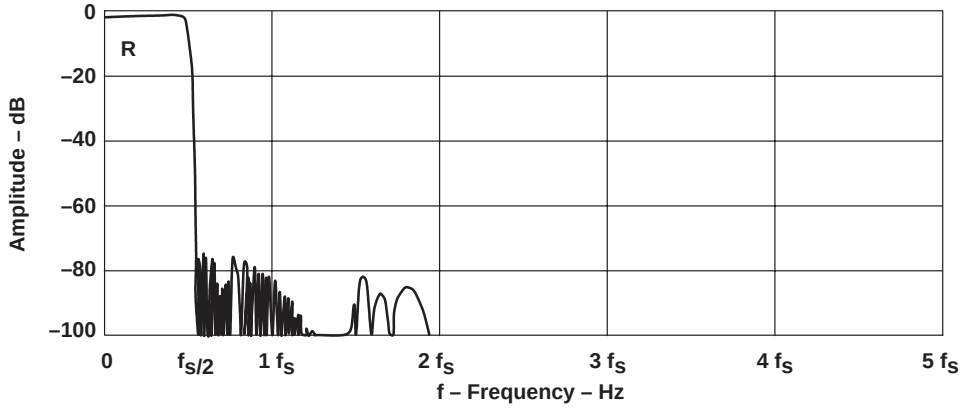


Figure 4–4. DAC Filter Overall Frequency Characteristics

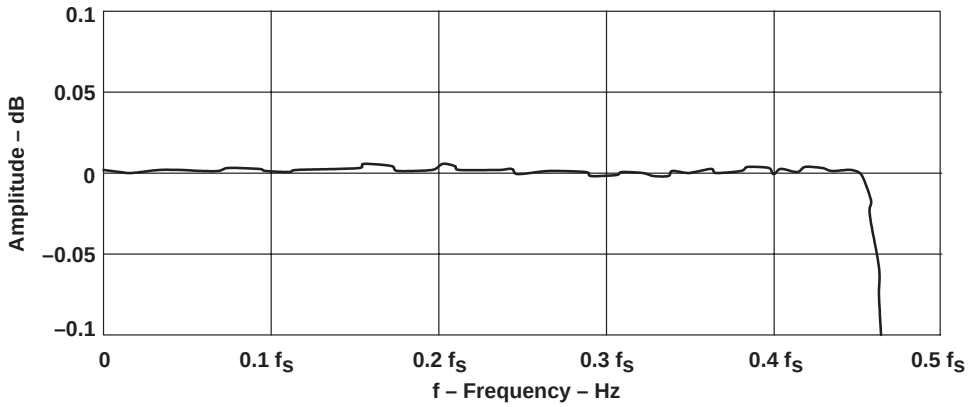


Figure 4–5. DAC Digital Filter Passband Ripple Characteristics

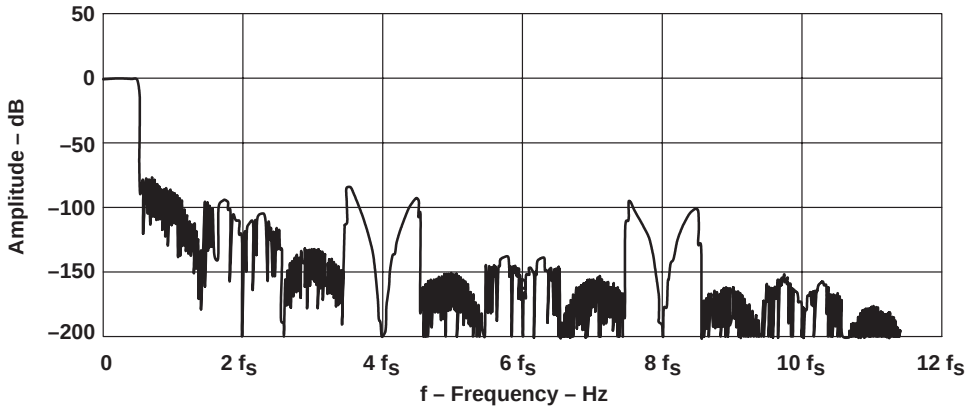


Figure 4–6. ADC Digital Filter Characteristics

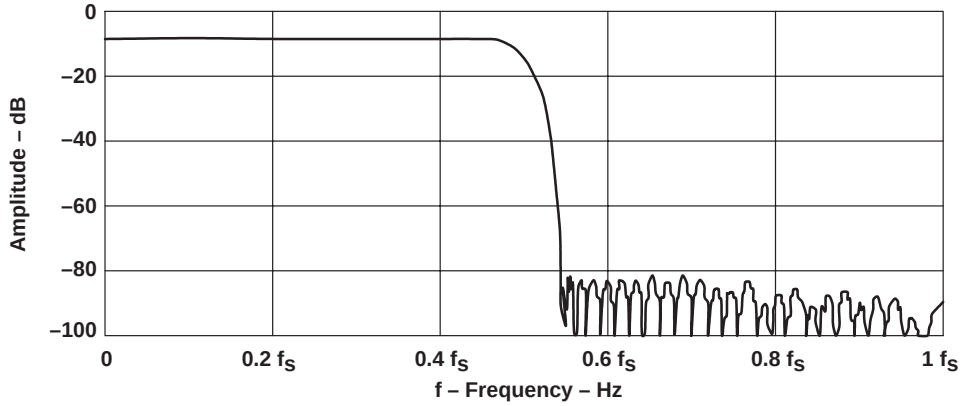


Figure 4–7. ADC Digital Filter Stopband Characteristics

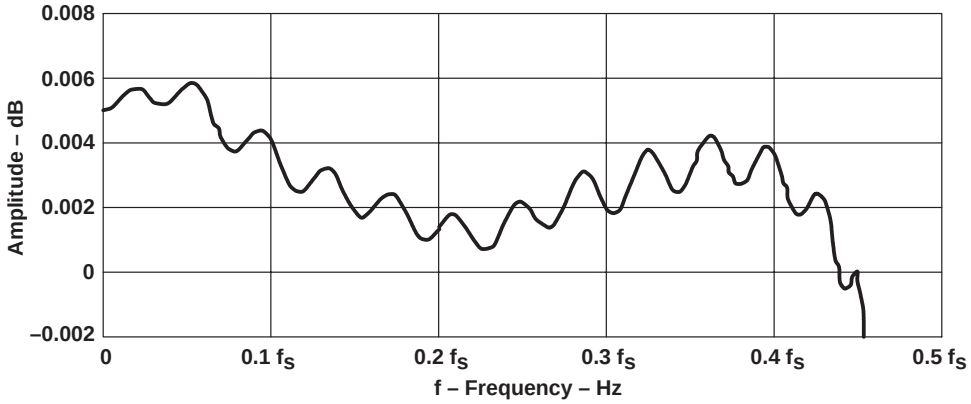


Figure 4–8. ADC Digital Filter Passband Characteristics

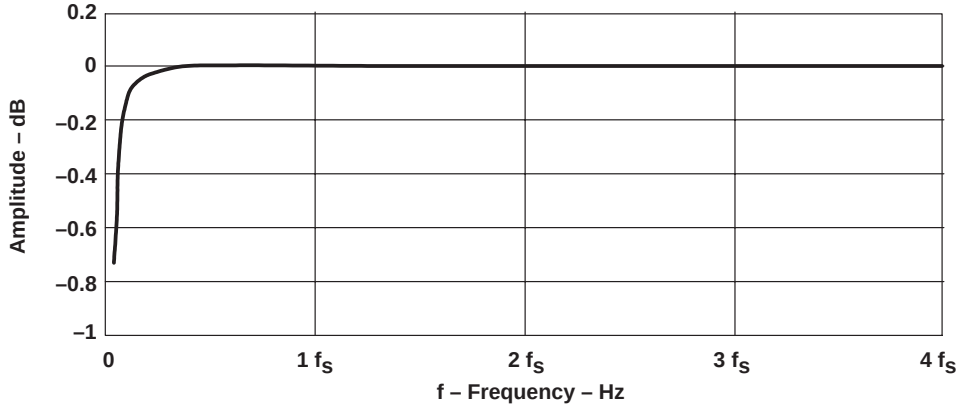


Figure 4–9. ADC High Pass Filter Characteristics

5 Application Information

5.1 Single-Ended to Differential External Analog Front-End Circuit (f_S = 44.1 kHz)

A single-ended to differential external analog front-end example circuit is shown in Figure 5–1. It biases the input signal around $AV_{DD}/2$ and applies the maximum input signal of 0.7 Vrms. The device sees a full-scale differential input voltage of approximately 4 V_{pp}. For other maximum input signals, the ratio of R2/R1 can be scaled accordingly to ensure a max ADC input of approximately 4 V_{pp}. As required by the ADC, R5, C4, and R6 provide a single-pole low-pass antialiasing filter to attenuate unwanted frequencies. If the user chooses to supply a single-ended input directly to the device (2 V_{pp} max), performance will be significantly degraded.

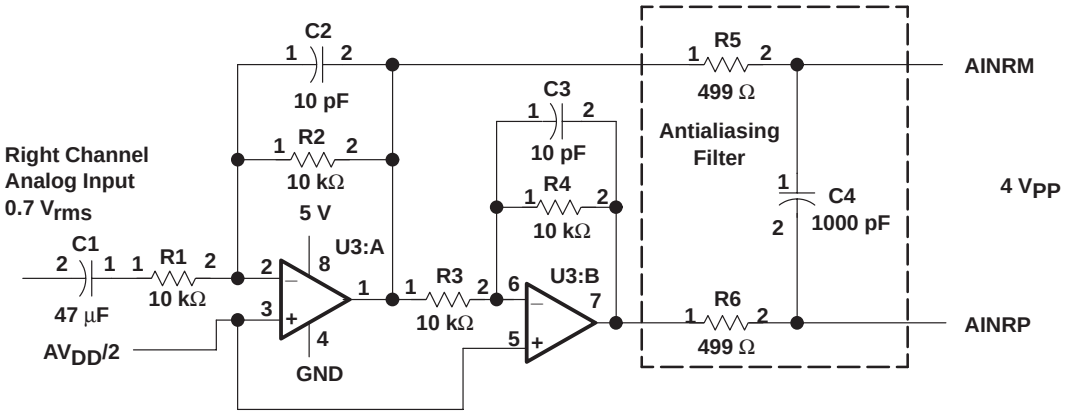


Figure 5–1. Analog Front End (right channel) for 0.7 Vrms Input

5.2 External Analog Back-End Circuit (f_S = 44.1 kHz)

For specified performance, the output should be taken between VCOM and AOUTR (or AOUTL). At pins AOUTR and AOUTL the output is an inverted analog representation of the digital input signal. It is advisable to add a low-pass filter to the output of the TLC320AD77C to eliminate high frequency noise >80 kHz. See Figure 5–2 for the recommended analog back-end circuit. The output of this circuit provides the user with a noninverted signal.

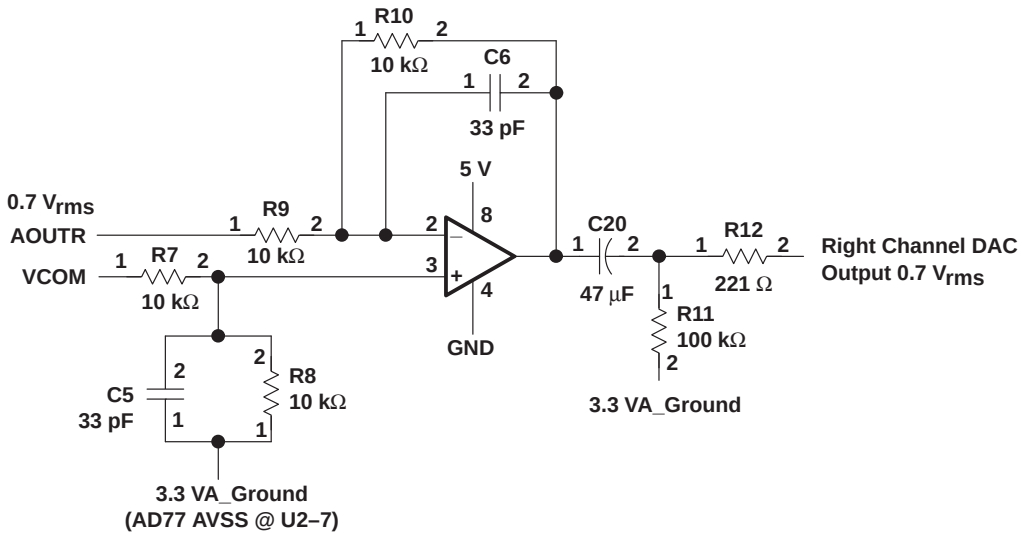


Figure 5–2. Analog Back End (right channel) for 0.7 Vrms Output

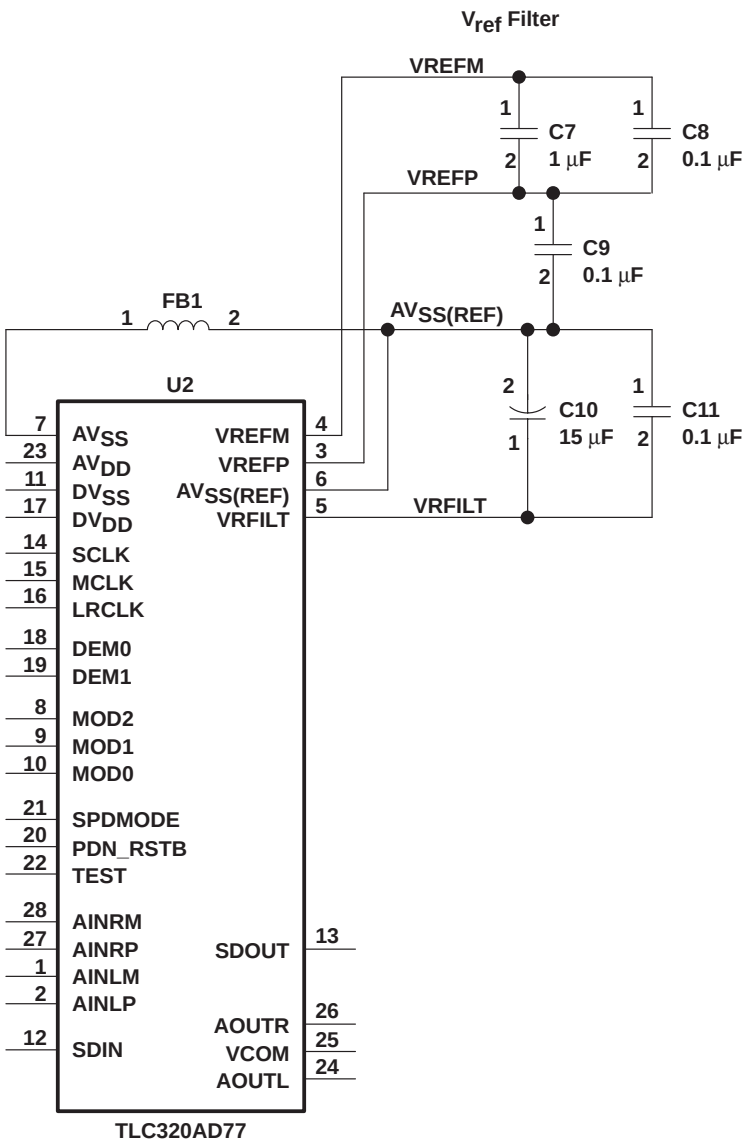
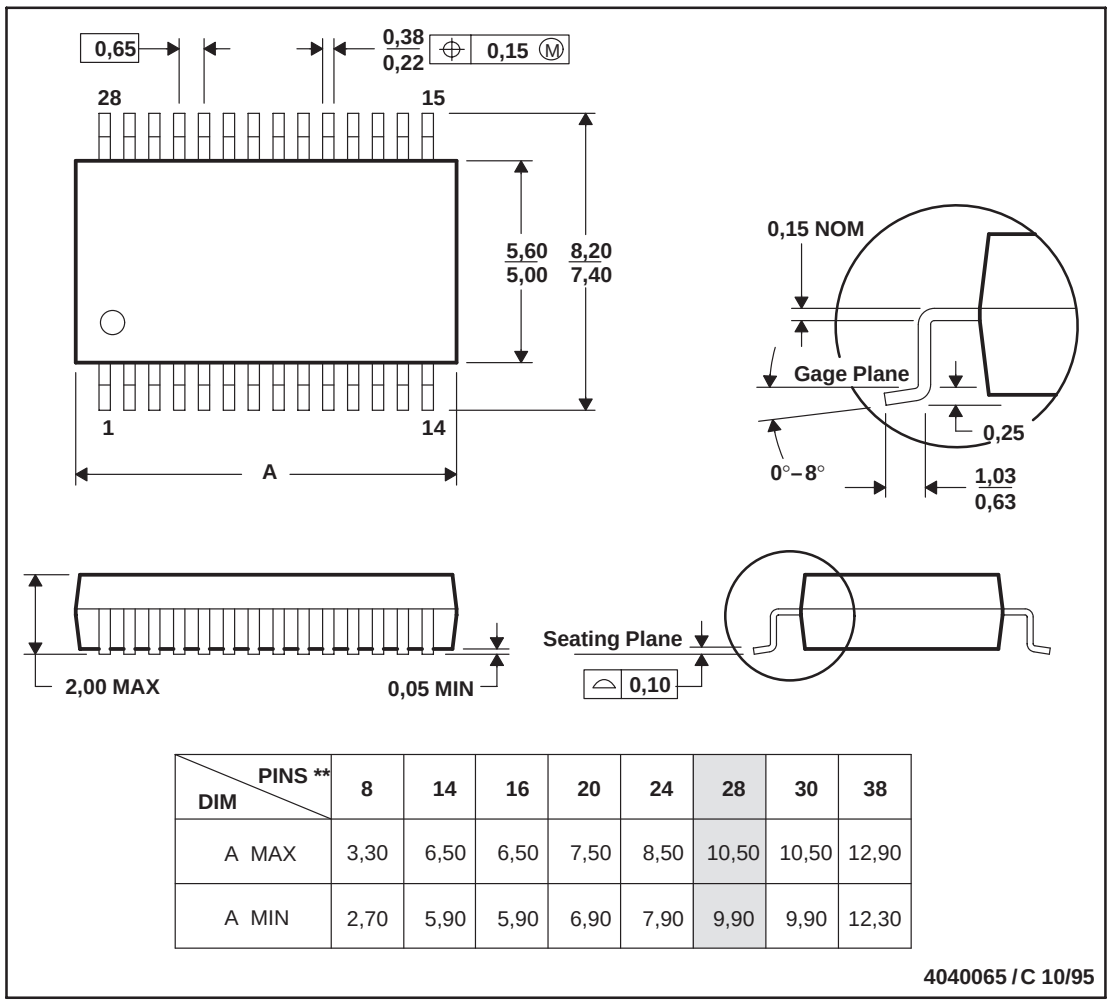


Figure 5–3. Voltage Reference Connections

Appendix A
Mechanical Data

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC320AD77CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC320AD77CDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC320AD77CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC320AD77CDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

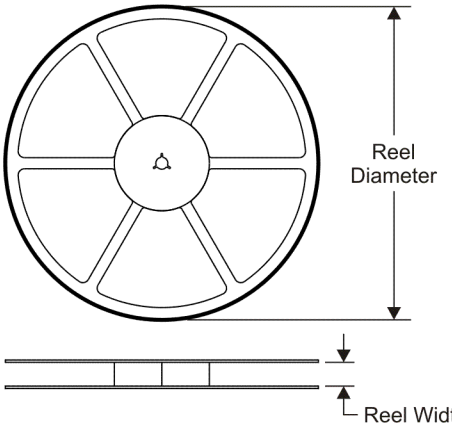
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

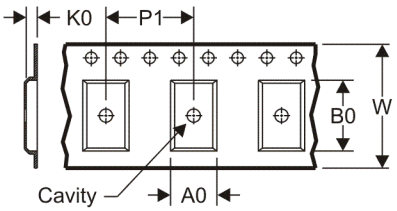
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

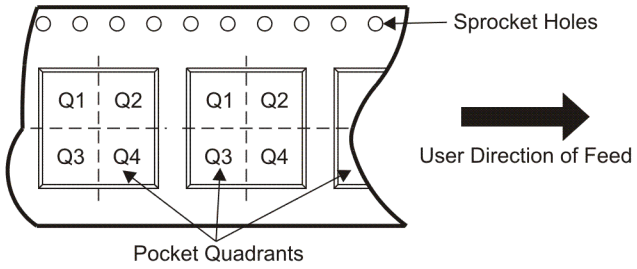


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

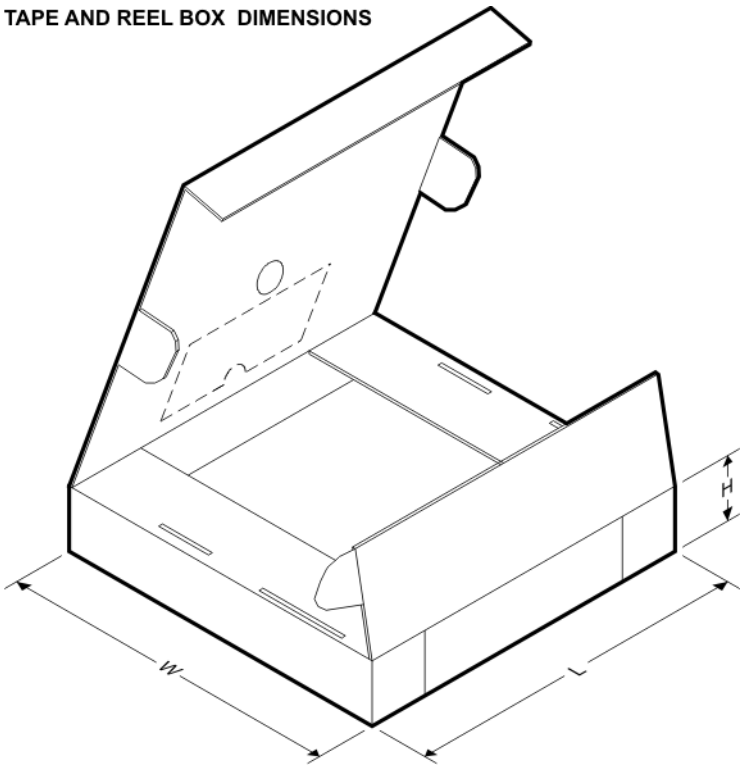
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC320AD77CDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC320AD77CDBR	SSOP	DB	28	2000	346.0	346.0	33.0